EECS 42 – Introduction to Electronics for Computer Science

Fall 2001, Prof. A. R. Neureuther
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Course Web Site http://www-inst.EECS.Berkeley.EDU/~ee42/

Final Examination December 14th, 2001

Closed Book, Closed Notes
You may use the equation sheet provided.
Write on the Exam paper

Print Your Name:_____

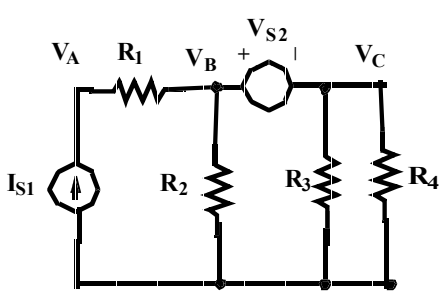
Sign Your Name:_____

Corrected: 12/18/01

Show your work so that the method as well as the answer can be graded for correctness and completeness. Correct answers alone are only worth 70% of full credit.

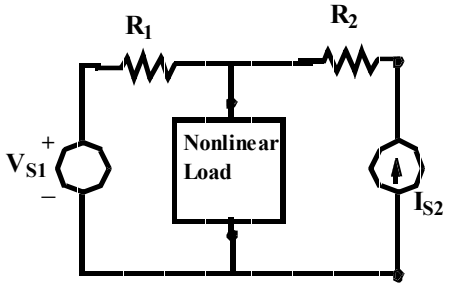
Problem	Possible	Score
I	42	
II	38	
III	40	
IV	38	
V	42	
Total	200	

I (42 Points) Basic Circuit Concepts

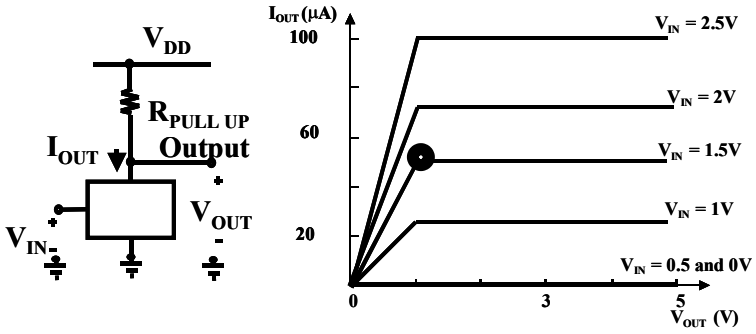


a) (10 Points) Find a single equation for V_C in terms of I_{S1}, V_{S2} and the resistors.

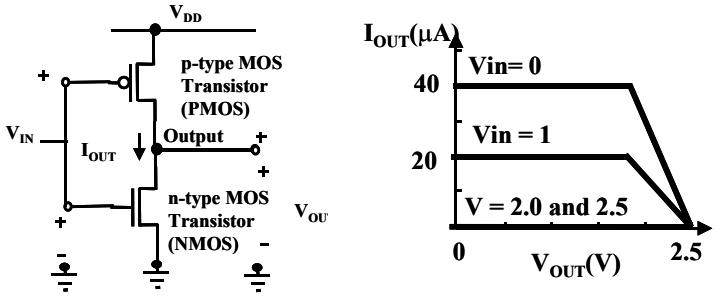
b) (10 Points) Find the Thevenin equivalent circuit seen looking outward from the nonlinear device.



c) (10 Points) Specify a value of R, V_{DD} and V_{IN} that makes the circuit operate at the point indicated on the I vs. V for an NMOS device.

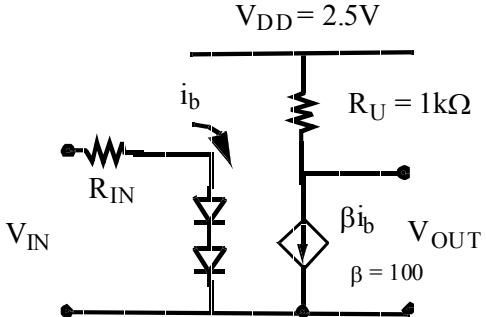


d) (12 Points) Graphically estimate V_M and the short circuit current when the PMOS with the I vs. V to the right and NMOS with I vs. V above are combined to create a CMOS inverter with V_{DD} = 2.5V.



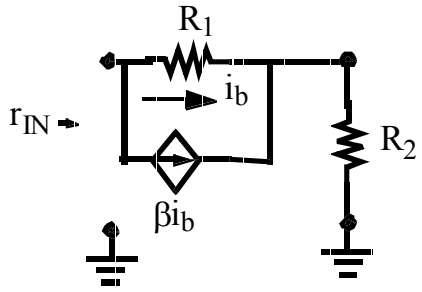
II (38 Points) Dependent Sources

a) (6 Points) Using the large signal diode model, find i_b when v_{IN} is 2V.



b) (12 Points) Find v_{IN} when v_{OUT} is 1.5V.

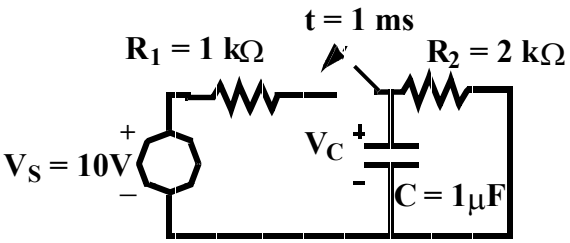
c) (14 Points) Find the input resistance for the circuit shown.



d) (6 Points) The input resistance in part c) above depends on R_1 and R_2. Does this circuit magnify, demagnify or not affect the contribution R_1?. Repeat for R_2 and briefly explain why the effects occur.

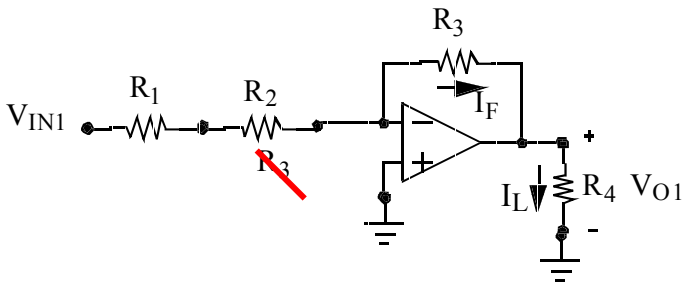
III (40 Points) Transients and Op-Amps

a) (9 Points) The switch in the circuit is closed at 1 ms. Just prior to closing the voltage on the capacitor is 3V. What was the voltage on the capacitor at t = 0?

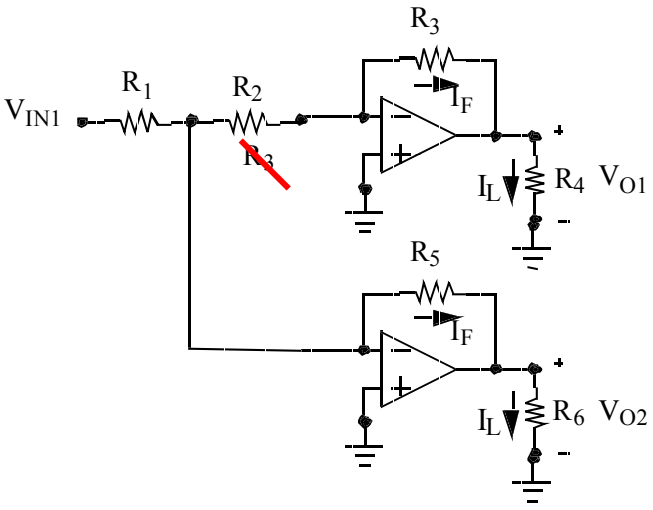


b) (6 Points) What is the time constant after the switch is closed?

c) (10 Points) For the Op-Amp circuit to the right find V_{OUT1} as a function of V_{IN1}.

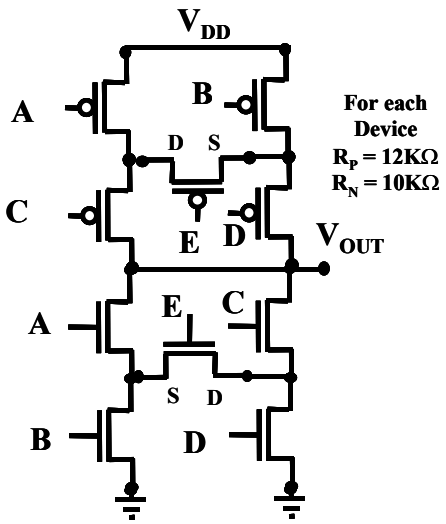


d) (15 Points) For the Op-Amp circuit to the right find V_{OUT1} and V_{OUT2} as a function of V_{IN1}. Be sure to show your fundamental assumptions. (Watch out this circuit may not be very useful.)



IV (38 Points) CMOS R, C and Carriers

a) (10 Points) Determine the worst-case resistance from the output to ground and give one example of inputs A-E for which this resistance will occur.



b) (15 Points) For the input state given to the right complete the table by specifying V_{DD}, GND or I (isolated) for each of the sources and drains in the circuit. For the vertical devices the NMOS source is toward the GND and the PMOS source is toward VDD. The horizontal devices are marked.

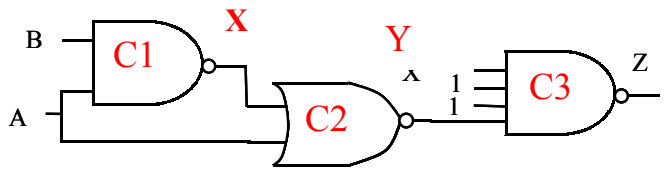
Input State: A = 0, B = 1, C = 1, D = 0, E = 0

	A	B	C	D	E
PMOS Source					
PMOS Drain					
NMOS Drain					
NMOS Source					

c) (13 Points) A 10 μm wide by 1 μm long NMOS transistor has carriers with a mobility of 200 cm^2/V-s and has a current of 10 μA when V_{DS} = 0.1V. Find the velocity of the carriers and the number of carriers per unit area under the gate. Hint: This problem requires only one very basic physical relationship and then some systematic reasoning. Several additional physical relationships have been added to the formula sheet to help you.

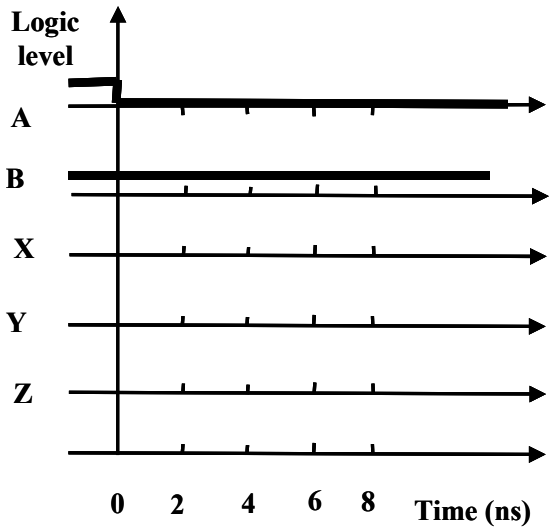
V (42 Points) CMOS Systems

a) (10 Points) Find the output logic levels of **X**, **Y**, and **Z** for the previous inputs when they have been applied for a long time and after the current inputs have been applied for a long time.



Previous A = 1, B = 1, X = , Y = , Z = .
Current A = 0, B = 1, X = , Y = , Z = .

b) (15 Points) Assuming each gate transition takes 2 ns, complete the timing diagram using the changes in the inputs given in the timing diagram.



The same logic function is implemented with latches as shown below. Each stage of the latch takes 100 ps. Circuits C1, C2 and C3 take 120ps, 150 ps and 250 ps respectively. The clock is high for 500 ps and low for 200 ps. Assume the previous logic state has been applied for many clock cycles at the labeled inputs and just before the clock goes low-high the input A on the left side of the circuit goes high-low.

c) (6 Points) Label all nodes with occurrences of signals **X**, **Y** and **Z** in the circuit below and indicate which of these nodes are **unsynchronized** (subject to additional data dependent delays in combinatorial logic) and which are **synchronized** (pass the correct and final value within a short constant delay) with the low-high transition of the clock.

d) (11 Points). Label as P1 and P2 the two critical points in the interior of this circuit where the final value must arrive before the clock high-low transition occurs. Determine the excess time that the clock is high, by finding the propagation delay to **both** of these two critical points and comparing them to the 500 ps high.