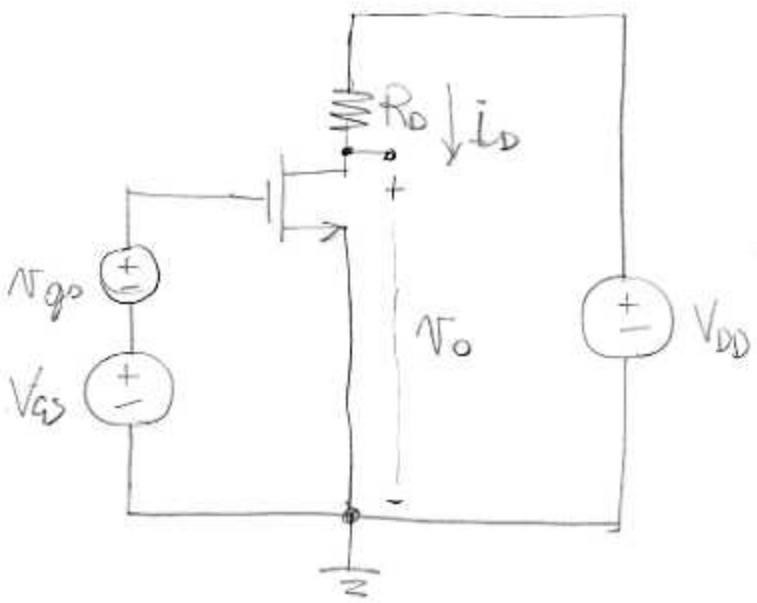
COMMON SOURCE CONFIGURATION

In this configuration the source is connected to ground:



We first consider $v_{gs}=0$, which means performing a DC analysis and computing the quiescent operating point.

We assume the transistor in saturation

$$I_{DQ} = \frac{K}{2}(V_{GS}-V_T)^2$$

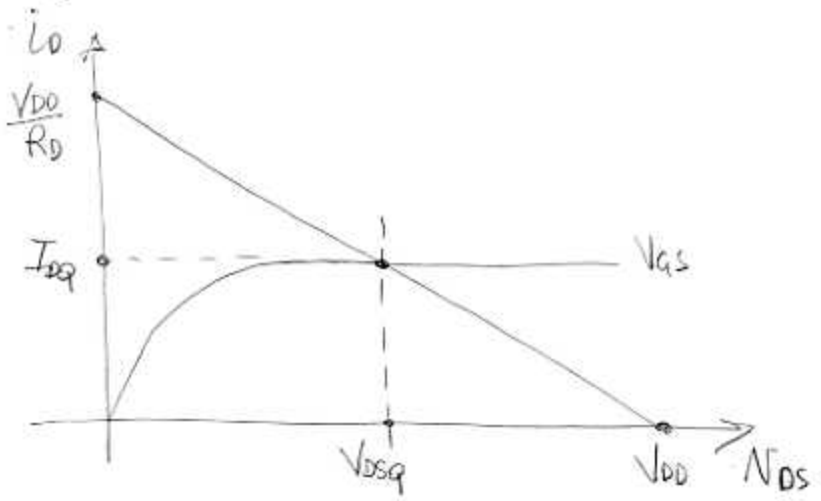
(V_{GS} is basically fixing the quiescent drain current)

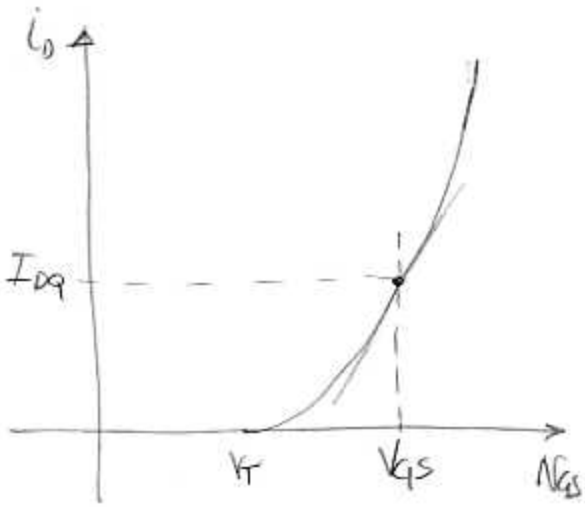
$$V_{DSQ} = V_{DD} - R_D I_{DQ} =$$

$$= V_{DD} - R_D \frac{K}{2}(V_{GS}-V_T)^2$$

In order for the transistor to be in saturation, it must be $V_{GS} > V_T$ and $V_{DSQ} \geq V_{GS}-V_T$

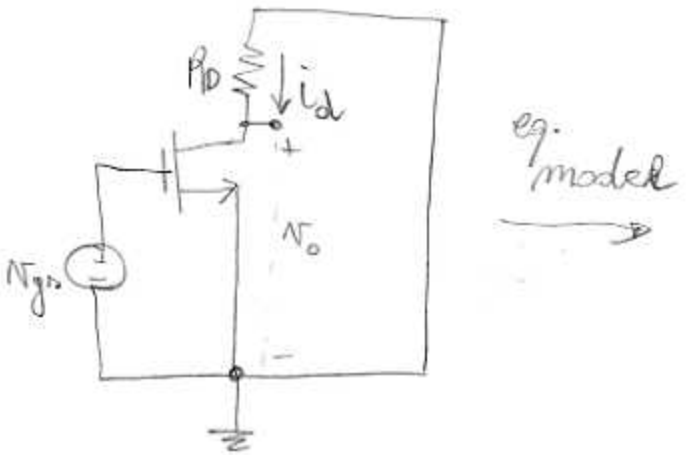
Using the load line:



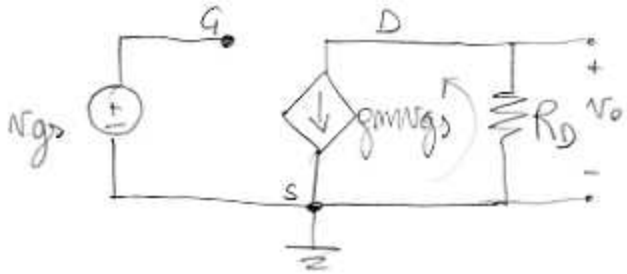


Now we compute $g_m = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{GS}} = K(V_{GS} - V_T)$

and we consider all DC sources equal zero:



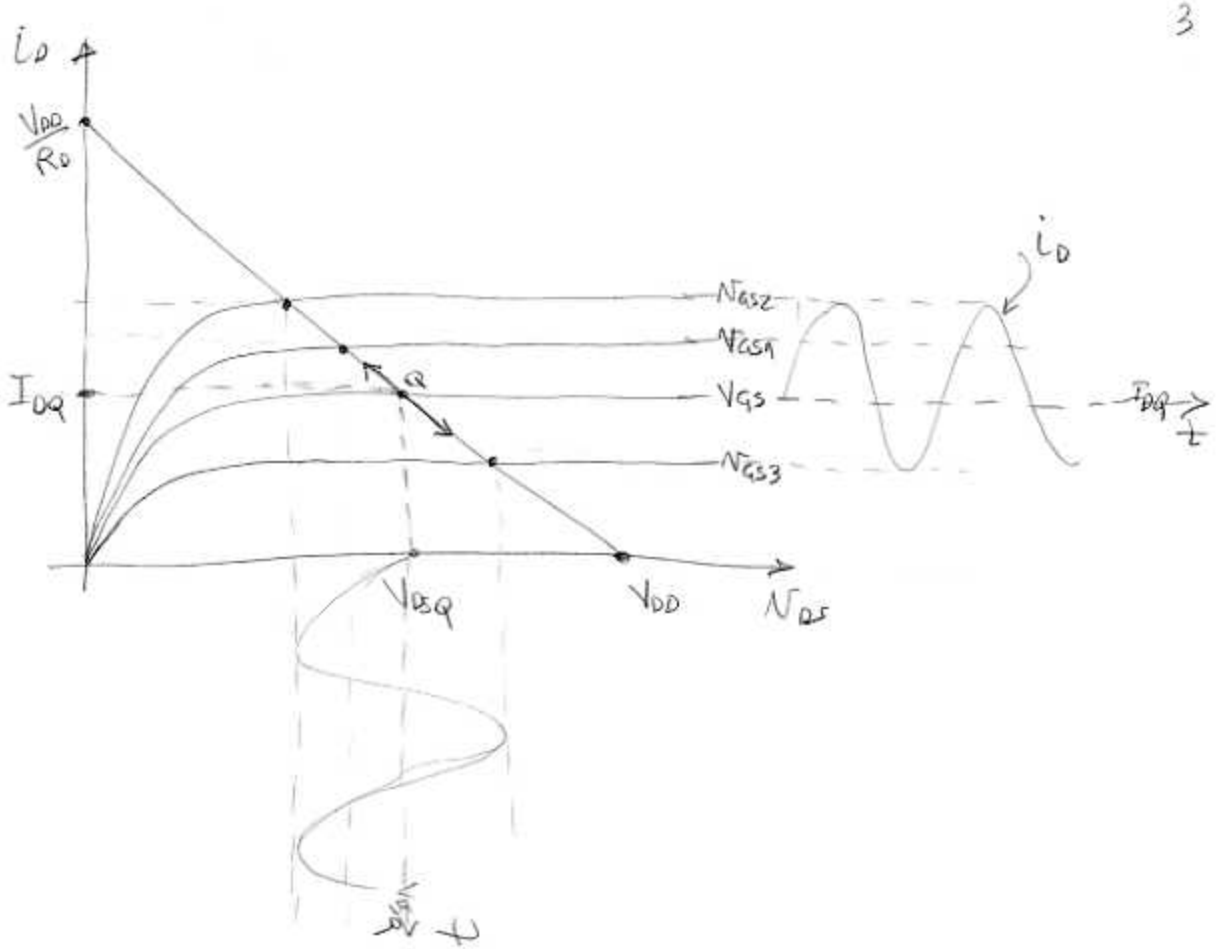
eq. model →

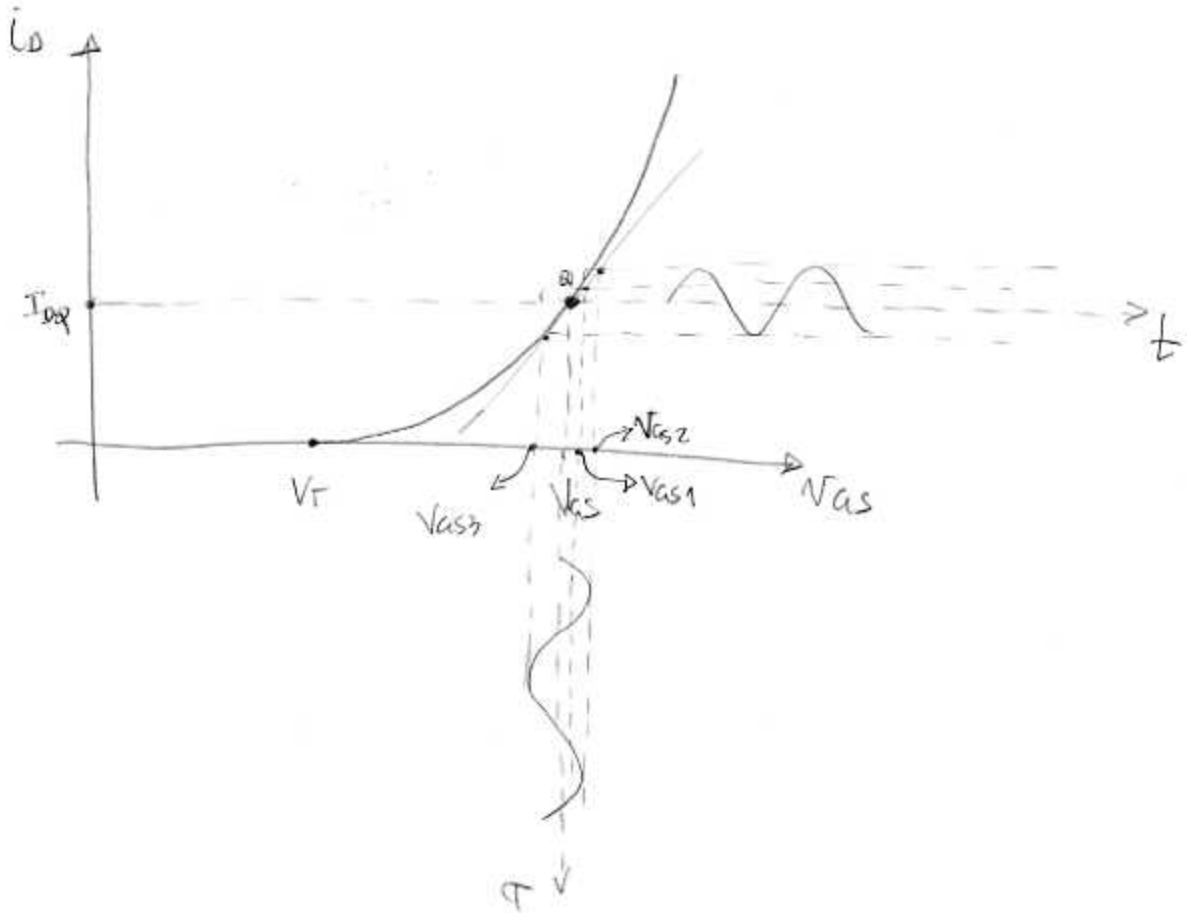


$$V_o = -g_m V_{gs} R_D \Rightarrow \quad \frac{V_o}{V_{gs}} = A_v = -g_m R_D$$

where A_v is the voltage gain.

Graphically the following thing is happening:


i_D
$\frac{V_{DD}}{R_D}$
I_{DQ}
Q
V_{GS2}
V_{GS1}
V_{GS}
V_{GS3}
V_{DSQ}
V_{DD}
V_{DS}
i_D
I_{DQ}
t
v_{gs}
t


i_D
I_{DQ}
Q
t
V_{GS2}
V_T
V_{GS3}
V_{GS}
V_{GS1}
V_{GS}
t