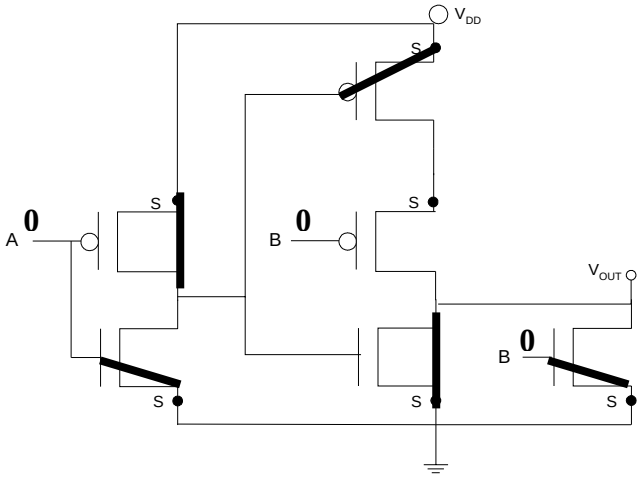
EE 40

Homework #6

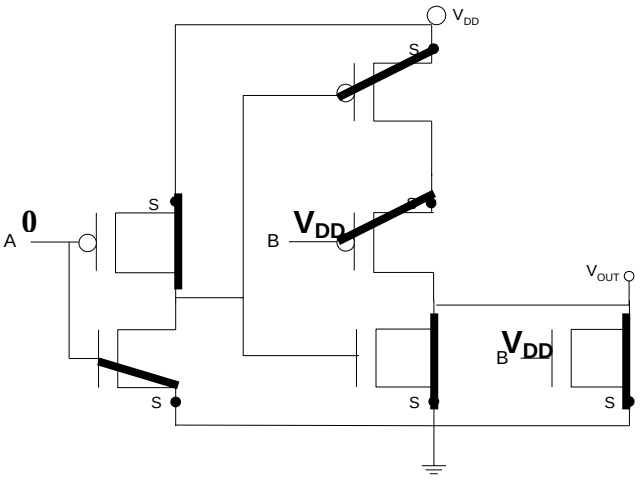
Solutions

Problem 1:

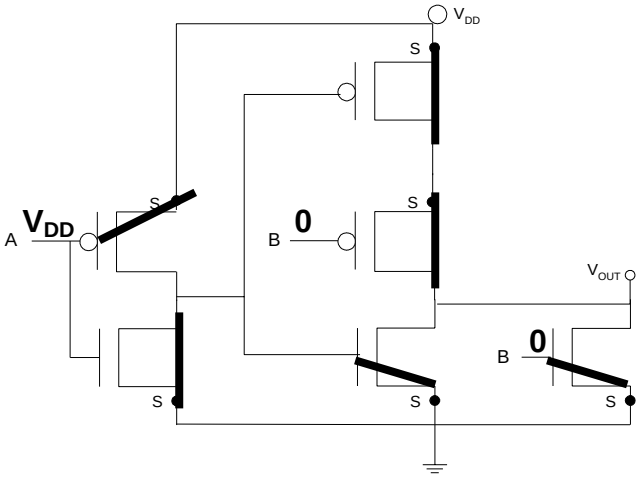
A = 0, B = 0: $V_{OUT} = 0$



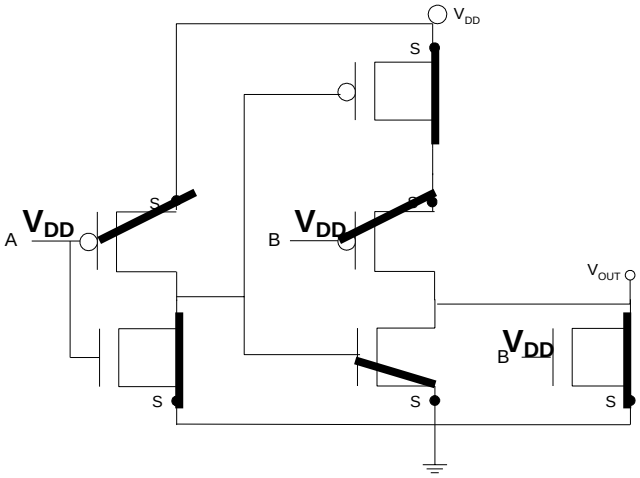
A = 0, B = V_{DD}: $V_{OUT} = 0$



A = V_{DD}, B = 0: $V_{OUT} = V_{DD}$

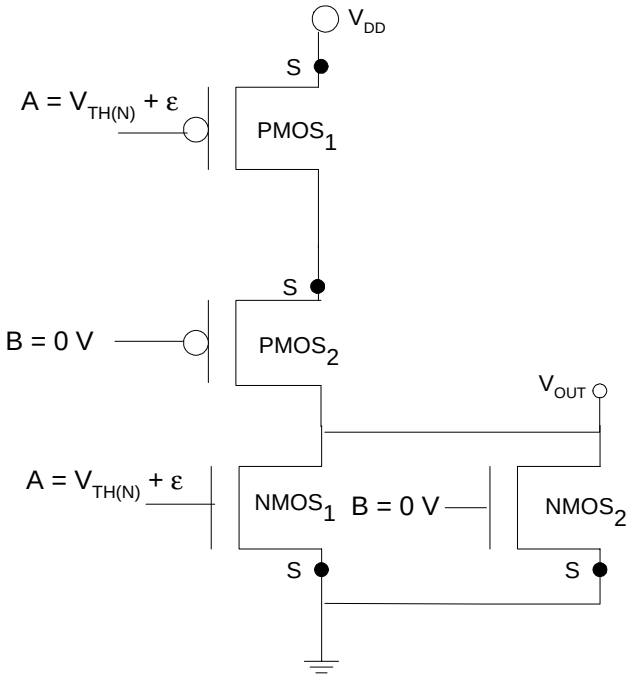


A = V_{DD}, B = V_{DD}: $V_{OUT} = 0$



Using sum-of-products, $V_{OUT} = A \overline{B}$.

Problem 2:



$NMOS_2$ is cutoff.

For $NMOS_1$, $V_{GS(N1)} = V_{TH(N)} + \varepsilon$.
$NMOS_1$ is therefore barely turned on, so I_D is small.

$PMOS_1$ and $PMOS_2$ have the same small current as $NMOS_1$ since no current goes through cutoff $NMOS_2$.

$PMOS_1$ has $V_{GS(P1)} = V_{TH(N)} + \varepsilon - V_{DD}$. By assumption stated in this problem, $PMOS_1$ is fully turned on.

Small I_D through a fully turned on transistor indicated **$PMOS_1$ is in triode mode.**

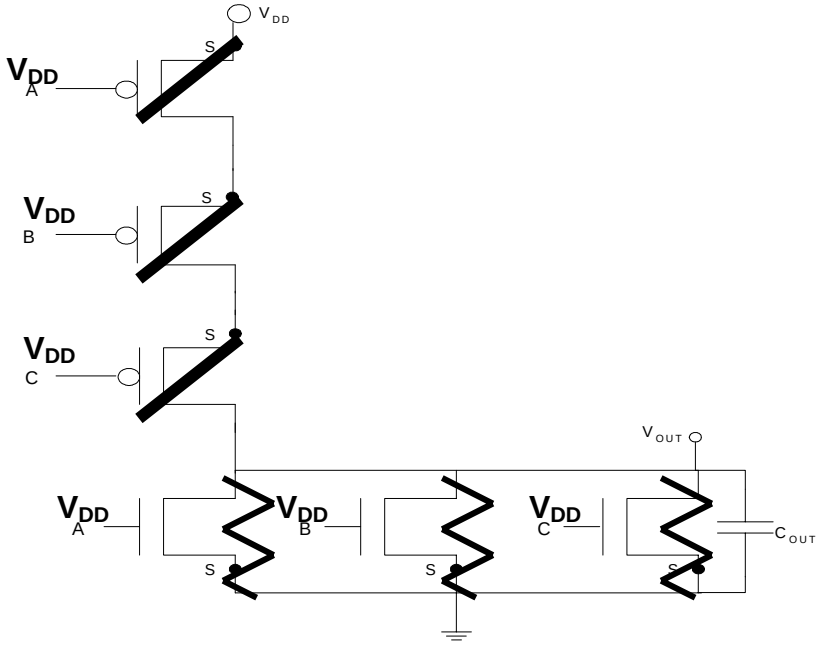
This also indicates that $V_{DS(P1)}$ for $PMOS_1$ will be small. So the source terminal of $PMOS_2$ is close to V_{DD} potential.

Therefore, $PMOS_2$ is fully turned on, and by the same argument, **$PMOS_2$ is in triode mode.**

Thus $PMOS_2$ will also have a small $V_{DS(P2)}$. This indicates $V_{DS(N1)}$ for $NMOS_1$ is close to V_{DD}, since $V_{DS(N1)}$, $V_{DS(P1)}$ (small), and $V_{DS(P2)}$ (small) must sum to V_{DD}. So **$NMOS_1$ is in saturation mode.**

Problem 3:

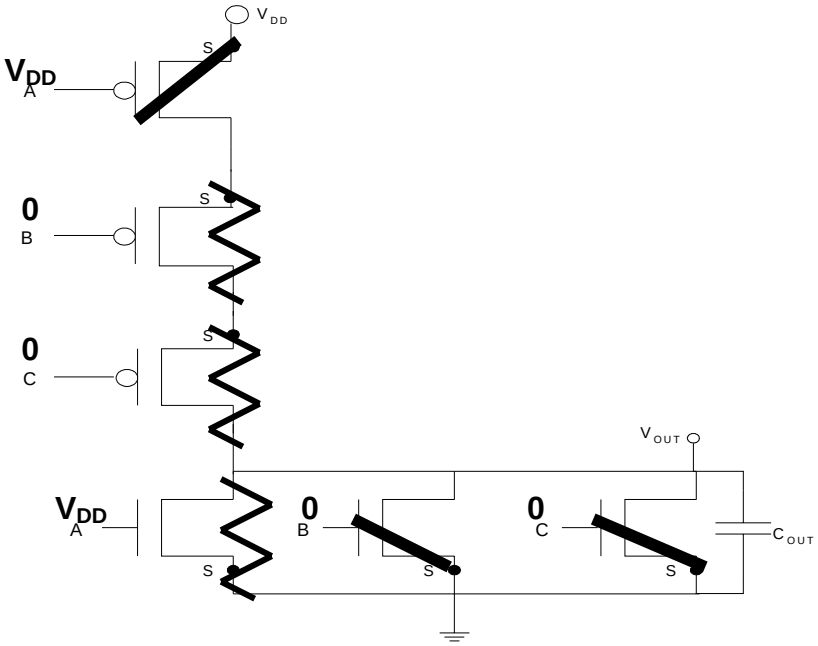
a) The shortest pull-down delay will occur when the NMOS resistances combine to form the smallest possible resistance. This will occur when all three NMOS transistors are active, so the resistances combine in parallel. To activate all three transistors, set $A = B = C = V_{DD}$. The previous input should make the output high so we can pull it down; previous input should be $A = B = C = 0$.



$R_{EQ} = R_N \,||\, R_N \,||\, R_N = 3.33\ k\Omega$

$t_p = 0.69\ R_{EQ}\ C_{OUT} = 115$ ps

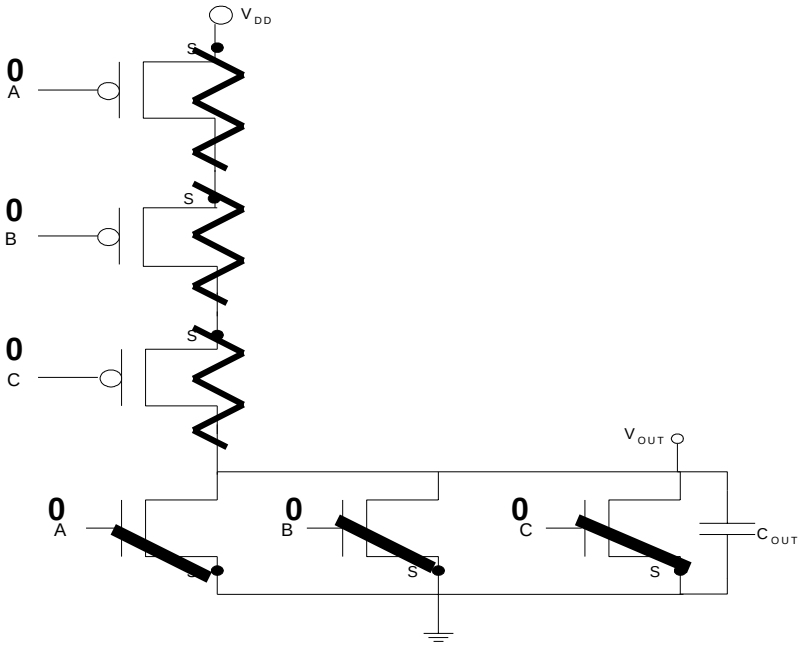
b) The longest pull down time occurs when the NMOS equivalent resistance is largest; when only one NMOS is on. This occurs when only one input is high, e. g. A = V_{DD}, B = C = 0, with previous inputs as in a).



$R_{EQ} = R_N = 10\ k\Omega$

$t_p = 0.69\ R_{EQ}\ C_{OUT} = 345$ ps

c) and d) There is only one way to pull up the output: set A = B = C = 0. Any other previous input will result in pull up with new input A = B = C = 0.



$R_{EQ} = 3\ R_P = 30\ k\Omega$

$t_p = 0.69\ R_{EQ}\ C_{OUT} = 1035$ ps

Problem 4:

$V_{DD} = 5$ V
$V_{TH(N)} = -V_{TH(P)} = 1$ V
$C_{OX} = 5$ fF/μm^2 for both transistors
L = 1 μm for both transistors
W = 2 μm for both transistors
λ = 0 for both transistors
$\mu_N = 50000$ mm^2 / (V s)
$\mu_P = 25000$ mm^2 / (V s)

a) When the previous input to the inverter is 0, and the new input is V_{DD}, then the output voltage will be pulled down. The NMOS transistor is active when the new input is V_{DD}, so it conducts the current discharging the capacitor.

$t_p = 0.69\ R_N\ C_{OUT}$

$R_N = ¾\ V_{DD} / I_{DSAT(N)}$

$I_{DSAT(N)} = ½\ W/L\ \mu_N\ C_{OX}\ (V_{GS(N)} - V_{TH(N)})^2 = ½(2\mu m / 1\ \mu m)(50000\ mm^2/Vs)(5\ fF/\mu m^2)(5\ V - 1\ V)^2$
$= 4$ mA

$R_N = 937.5\ \Omega$

There are 4 transistors per NAND or NOR gate. With one NAND and one NOR attached to the output, 8 transistors are attached to the inverter output. Thus, 8 C_G capacitances are contributed.

$C_G = W\ L\ C_{OX} = (2\ \mu A)(1\ \mu A)(5\ fF/\mu m) = 10$ fF

Since we are not including interconnect capacitance,

$C_{OUT} = 8\ C_G = 80$ fF

$t_p = 0.69\ (937.5\ \Omega)\ (80\ fF) = 51.75$ ps

When the previous input to the inverter is V_{DD} and tine new input is 0, the output voltage will be pulled down. The PMOS transistor is active when the new input is 0, so it conducts the current charging the capacitor.

$t_p = 0.69\ R_P\ C_{OUT}$

$R_P = -¾\ V_{DD} / I_{DSAT(P)}$

$I_{DSAT(P)} = -½\ W/L\ \mu_P\ C_{OX}\ (V_{GS(P)} - V_{TH(P)})^2 = -½(2\mu m / 1\ \mu m)(25000\ mm^2/Vs)(5\ fF/\mu m^2)(-5\ V - -1\ V)^2$
$= -2$ mA

$R_P = 1.875\ k\Omega$

$t_p = 0.69\ (1.875\ k\Omega)\ (80\ fF) = 103.5$ ps

b) Each NAND or NOR contributes 4 C_G, so we need $t_p = 0.69\ (1.875\ k\Omega)\ (4\ N \bullet 10fF) \leq 2$ ns where N is the number of NAND or NOR. (Using R_P is worst-case.) $N \leq 38$