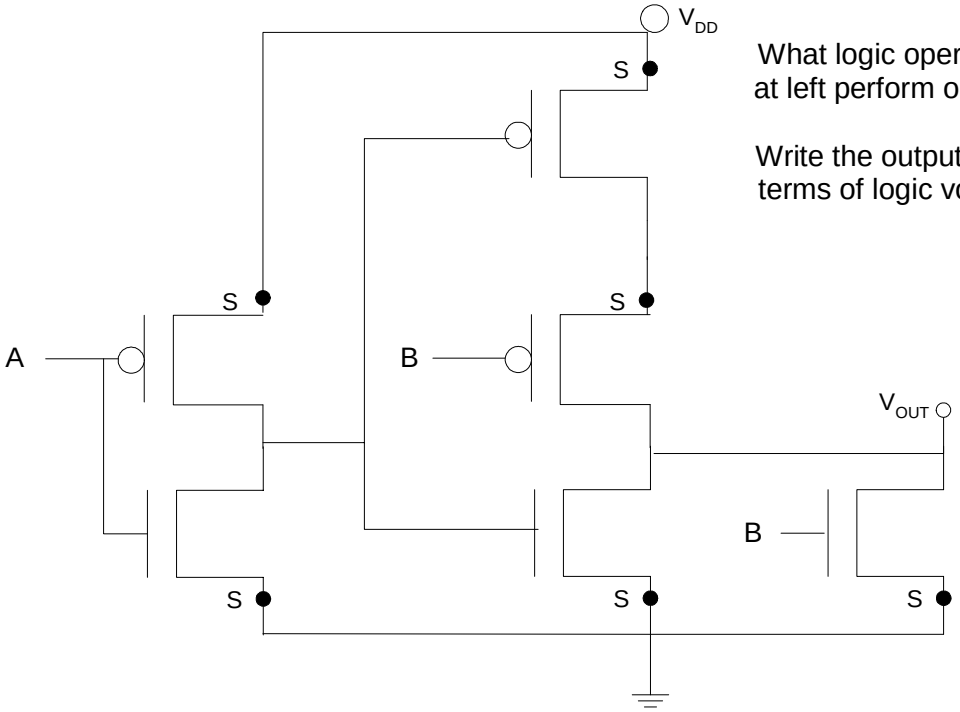
EE 40

Homework #6

Due Tuesday, April 22, 2003, 3:30 PM

40 Total Points Possible

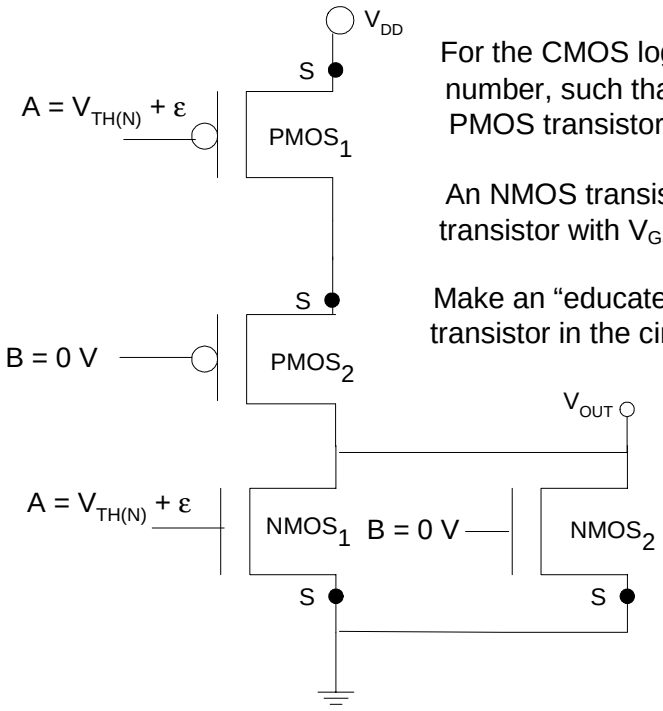
Problem 1: 10 Points Possible



What logic operation does the CMOS circuit at left perform on the binary inputs A and B?

Write the output as a Boolean function in terms of logic voltages A and B.

Problem 2: 8 Points Possible

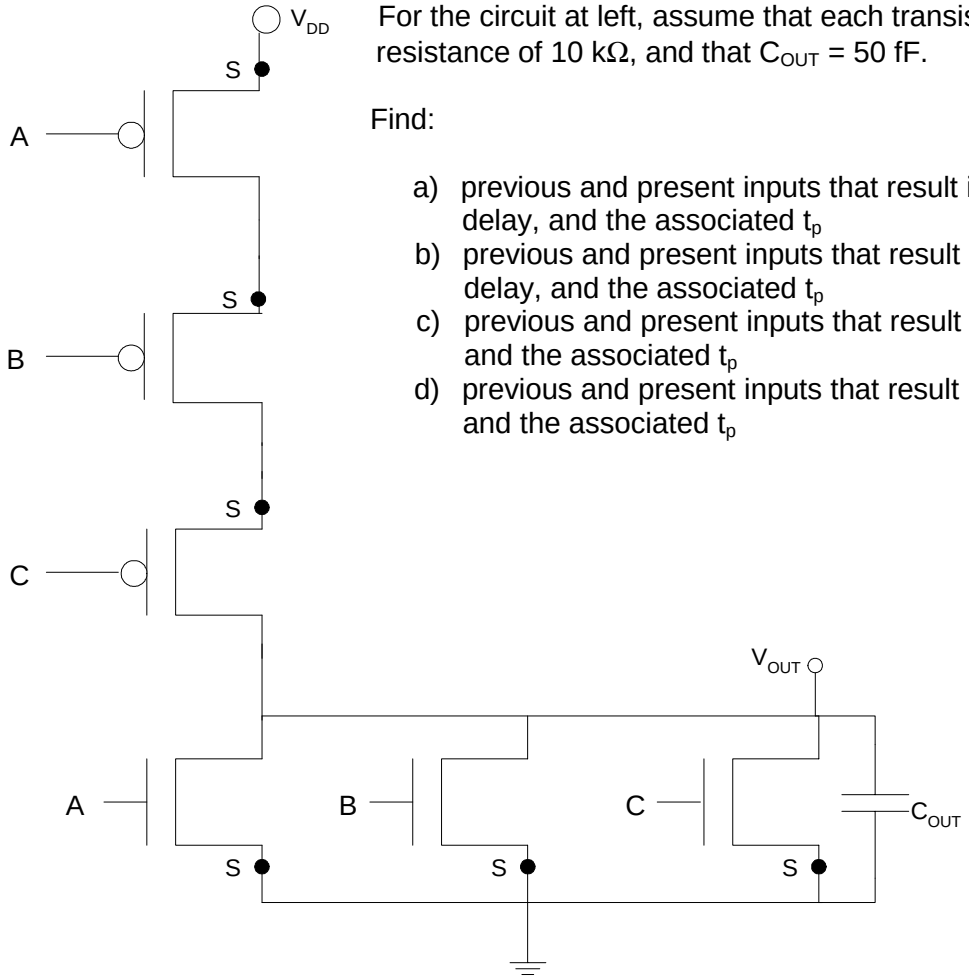


For the CMOS logic circuit at left, assume that ε is a small positive number, such that an NMOS transistor with $V_{GS(N)} = V_{TH(N)} + \varepsilon$ (or PMOS transistor with $V_{GS(P)} = V_{TH(P)} - \varepsilon$) would be "barely" turned on.

An NMOS transistor with $V_{GS(N)} = V_{DD} - (V_{TH(N)} + \varepsilon)$ (or PMOS transistor with $V_{GS(P)} = -V_{DD} - (V_{TH(P)} - \varepsilon)$) would be "fully" turned on.

Make an "educated guess" for the mode of operation of each transistor in the circuit at left. Assume $V_{TH(N)} \approx -V_{TH(P)}$.

Problem 3: 12 Points Possible



For the circuit at left, assume that each transistor has a pull-up/pull-down resistance of 10 kΩ, and that C_{OUT} = 50 fF.

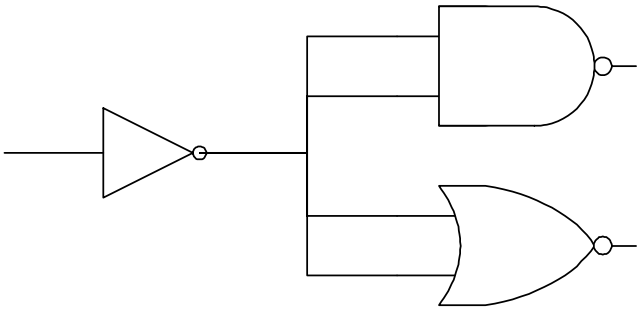
Find:

a) previous and present inputs that result in the shortest pull-down delay, and the associated t_p
b) previous and present inputs that result in the longest pull-down delay, and the associated t_p
c) previous and present inputs that result in the shortest pull-up delay, and the associated t_p
d) previous and present inputs that result in the longest pull-up delay, and the associated t_p

Problem 4: 10 Points Possible

Consider the logic circuit below. Each logic gate is constructed using the appropriate CMOS circuit given in lecture. With

V_{DD} = 5 V
$V_{TH(N)} = -V_{TH(P)}$ = 1 V
C_{OX} = 5 fF/μm^2 for both transistors
L = 1 μm for both transistors
W = 2 μm for both transistors
λ = 0 for both transistors
μ_N= 50000 mm^2 / (V s)
μ_P= 25000 mm^2 / (V s)



a) Find the low-to-high and high-to-low propagation delays t_p for the inverter in the circuit as shown. Take into account the pull-up and pull-down resistances of the transistors (which you must calculate here), as well as the gate capacitances of the attached gates (calculate also).

b) Suppose I require that the maximum propagation delay through the inverter is 2 ns. Determine the maximum fan-out: the maximum number of NAND or NOR gates that can be attached to the inverter output if the propagation delay through the inverter is to be 2 ns maximum.