EE 40

Homework #4

Due March 13, 2003

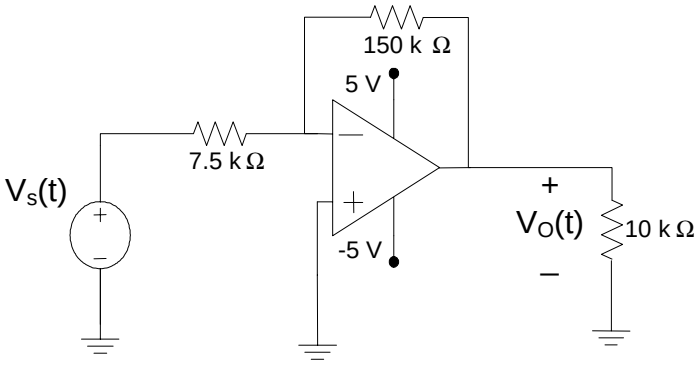
60 Points Possible

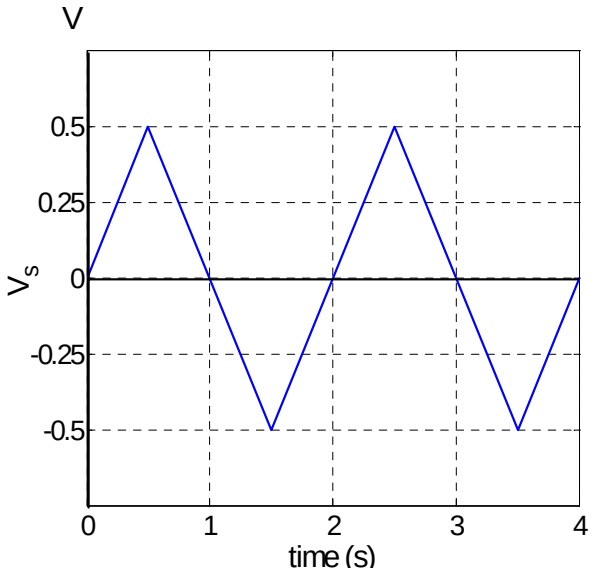
Nearly all problems taken from *Electric Circuits* by Nilsson and Riedel

Notation: The extra connections coming out of the amplifier indicate the "rails".

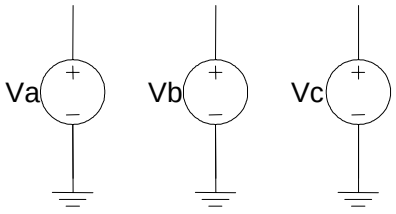
Problem 1: 10 Points Possible

For the input voltage $V_s(t)$ and ideal operational amplifier circuit below, sketch $V_O(t)$.



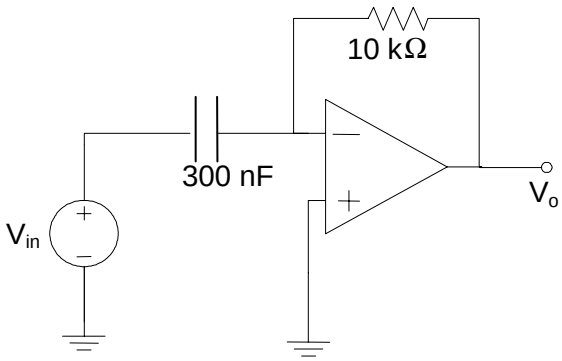


Problem 2: 8 Points Possible



Given three input voltages Va, Vb, and Vc, which cannot be detached from ground, design an ideal operational amplifier circuit which has the average of Va, Vb, and Vc as its output voltage. This output voltage must be maintained regardless of the resistance connected at the output. Ignore the effect of the rail voltages.

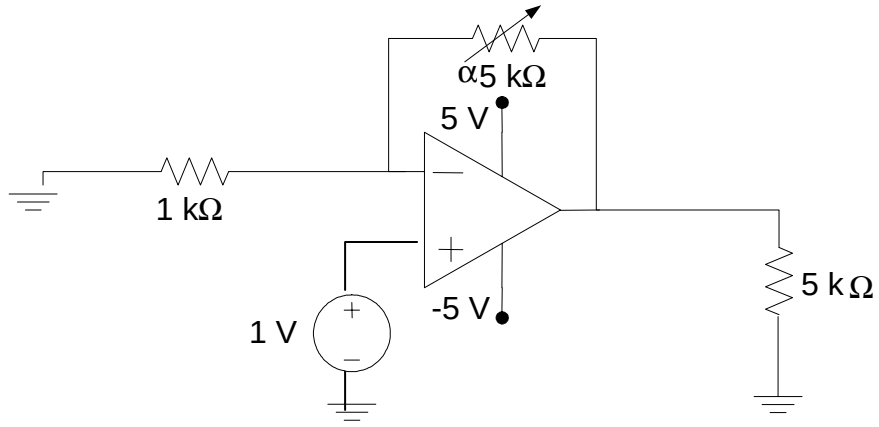
Problem 3: 12 Points Possible



a) Find V_o as a function of V_{in}. Ignore the effect of the rails.

b) Let $V_{in}(t) = \sin(120\pi t) + 10^{-6}\sin(10^6 \cdot 120\pi t)$. Consider $V_{in}(t)$ to be a 1 V amplitude, 60 Hz signal corrupted by 1 μV of VHF TV channel 2 (FOX). Find Vo(t), and make **rough** sketches of Vo(t) over 1/60 μs and Vo(t) over 1/60 s.

Problem 4: 10 Points Possible



The resistor labeled $\alpha 5\ k\Omega$ is simply a variable resistance, where α is some positive parameter. What is the maximum value that α may take if the amplifier is to operate linearly (i.e., not hit a rail)?

Problem 5: 12 Points Possible

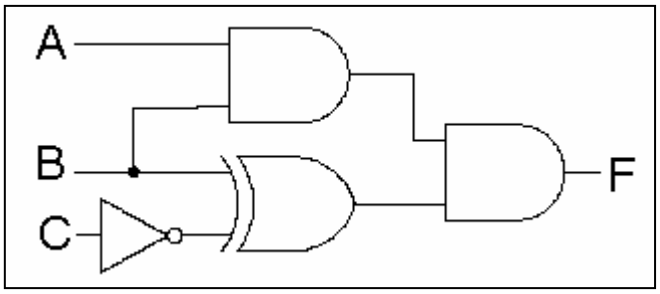
Inputs			Output
A	B	C	S_1
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

a) Use the sum-of-products method to write a Boolean function for S_1 in the variables A, B and C for the truth table at left.

b) Draw a NAND-NAND implementation for this circuit.

c) Simplify the implementation of this circuit to use the fewest total number of logic gates. You may use any of the gates covered in lecture, with any number of inputs.

Problem 6: 8 Points Possible



Consider the logic circuit at left. Assume that inputs A, B, and C have been at logic zero for a long time, and then instantaneously change to logic 1 at time t=0. Assume also that each logic gate has propagation delay τ. Draw a timing diagram showing the logic transitions of output F.