

- H<br>W #5 changes
- H<br>N #6
- **–**  $\geqq$ ල<br>ග 등  $\stackrel{\sigma}{\leq}$ tonight, গে problems
- **–** D<br>G<br>0 next Wednesday (08/06)
- **–**  $\geqq$ ල<br>ග a good review for the<br>O midterm
- Return H<br>Ms 4 and<br>D ಊ o<br>J Monday (08/04)
- Return 工<br>W ω and<br>D corrected HWs  $\overline{\phantom{0}}$ and<br>D  $\overline{\bm{\mathsf{c}}}$ o<br>J Friday (08/01)
- Midterm  $\equiv$ next Wednesday, 08/06/03!
- Practice problems 등  $\stackrel{\sigma}{\leq}$ tonight
- Review session? session?



- CMOS voltage transfer characteristic
- **–** SUGGESTION: Go over lecture  $\vec{\circ}$ STEP-BY-STEP
- **–** Ask questions <u>in</u> discussion and<br>D office hours!



- CMOS inverter propogation delay analysis
- **–** Complete our propogation delay model
- **–** Understand M<br>CSS capacitances
- **–** Switch-RC model <u>ር</u> the<br>O CMOS inverter
- **–** Understand and<br>D 77
- CMOS layouts and<br>D fabrication steps
- Extract capacitances,  $\leq$ and<br>D  $\overline{\phantom{a}}$ from layout/crossection
- References: Lectures  $\overset{\rightharpoonup }{\infty }$ and<br>D د<br>ص (Fall 1999) and<br>D Lecture  $\geq$ (Spring 2003)

#### MOSFET Capacitances MOSFET Capacitances

### Node connected to the gate: **Node connected to the gate:**



# **Node connected to the drain (or source):** Node connected to the drain (or source):

- providence between drain and bulk is C · pn junction capacitance between drain and bulk is C<sub>DB</sub>
- capacitance CSB is shorted out since  $\,<\,$  $\frac{\infty}{\mathsf{I}}$  $\gtrsim$ in digital circuits

#### The CMOS Inverter The CMOS Inverter



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## First Order CMOS Inverter Model First Order CMOS Inverter Model

**voltages The switches are "ganged" (move together) since they have the same trip**  The switches are "ganged" (move together) since they have the same trip

**NMOS is closed when** *vin* **>** *VTh* **; PMOS is open PMOS is closed when** *vin*  $\Lambda$  $\sum_{\tau}$ **; NMOS is open**

Reduce to a single switch (Fig. 2.10, R&R) **Reduce to a single switch (Fig. 2.10, R&R)**



### «Leareded" CMD Suverters "Cascaded" CMOS Inverters

**What's connected to the** *vout* **node?**

Representative "load" ... possibly another CMOS inverter **Representative "load" … possibly another CMOS inverter**



# Cascaded Identical CMOS Inverter Circuit Model Cascaded Identical CMOS Inverter Circuit Model



### Simpler Representation Simpler Representation

**operate in a complementary fashion NMOS and PMOS transistors have the same logic thresholds, but**  NMOS and PMOS transistors have the same logic thresholds, but operate in a complementary fashion  $\Rightarrow$  reduce to a single switch per **reduce to a single switch per inverter**



**Transitions of interest:** Transitions of interest:

**1.** *vin***1 increases above**  $\leq$ *Th*  **: switch for inverter 1 moves to "D" position from previous "U" position**

previous "D. bosition **previous "D" position2.** *vin***1 decreases below**  $\leq$ *Tl* **: switch for inverter 1 moves to "U" position from** 



#### Output Propagation Delay High to Low **Output Propagation Delay High to Low Version Date 04/03/03** Version Date 04/03/03



When  $V_{IN}$  goes High  $V_{OUT}$  starts decreases with time **goes High VOUT starts decreases with time** 

downstream gate to begin to switch is V<sub>pp</sub>/2 or 2.5V. Assume that the necessary voltage swing to cause the next **downstream gate to begin to switch is V Assume that the necessary voltage swing to cause the next DD/2 or 2.5V.** 

high to low is the time to go from  $V_{\text{DD}} = 5V$  to to  $V_{\text{DD}}/2 = 2.5V$ high to low is the time to go from  $\rm V_{\rm DD}$ **That is the propagation delay** τ**HL for the output to go from**  = 5V to to  $\rm V_{\rm DD}/2$  =2.5V

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#### Output Propagation Delay High to Low (Cont.) **Output Propagation Delay High to Low (Cont.)** Version Date 04/03/03 **Version Date 04/03/03**



When  $V_{OUT} > V_{OUT-SAT-D}$  the available current is  $I_{OUT-SAT-D}$ **When VOUT > VOUT-SAT-D the available current is IOUT-SAT-D**

is constant at  $I_{\text{OUT-SAT-D}}$  and the capacitor discharges. For this circuit when  $V_{OUT} > V_{OUT-SAT-D}$  the available current **is constant at IOUT-SAT-D and the capacitor discharges. For this circuit when VOUT > VOUT-SAT-D the available current** 

#### **The propagation delay** The propagation delay is thus

$$
M = \frac{C_{OUT}\Delta V}{I_{OUT-SAT-D}} = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = \frac{50\sqrt{F \cdot 2.5V}}{100\mu A} = 1.25ms
$$

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 $\Gamma$ ecreament  $\sim 1000$  X.R. Neurenher **Lecture 18: 04/0703 A.R. Neureuther**

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# **Switched Equivalent Resistance Model Switched Equivalent Resistance Model**

The above model assumes the device is an ideal constant current source. **The above model assumes the device is an ideal constant current source.**

1) This is not true below  $V_{\text{OUT-SAT-D}}$  and leads to in accuracies. **1) This is not true below VOUT-SAT-D and leads to in accuracies.**

and parallel connections is problematic. 2) Combining ideal current sources in networks with series **2) Combining ideal current sources in networks with series rallel connections is problematic.**

equal to the ∆t found above Instead define an equivalent resistance for the device by setting  $0.69\rm R_\odot C$ **equal to the** Instead define an equivalent resistance for the device by setting  $0.69 \rm R_{\rm D}C$ **t found above**

$$
\Delta t = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = 0.69R_DC_{OUT} \qquad \qquad \begin{array}{c}\n\text{This gives} \\
\frac{V_{DD}}{V_{DD}} = 0.69R_DC_{OUT} \\
\text{if} \\
\frac{V_{DD}}{V_{DD}} = \frac{3}{2} \cdot \frac{5V}{2V_{DD}} = 37.5 \text{k}\Omega\n\end{array}
$$

**This gives**

$$
R_D = \frac{V_{DD}}{2 \cdot (0.69) I_{OUT-SAT-D}} \approx \frac{3}{4} \frac{V_{DD}}{4 I_{OUT-SAT-D}} = \frac{3}{4} \frac{5V}{100 \mu A} = 37.5 k\Omega
$$

 $\frac{1}{2}$ 

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**Each device can now be replaced by this equivalent resistor.**

Each device can now be replaced by this equivalent resistor.

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from  $(0,0)$  to  $( I_{\text{OUT-SAT-D}}$ , <sup>3</sup>/<sub>4</sub>  $V_{\text{DD}}$  ). Approximate the NMOS device curve by a straight line **from (0,0) to (I Approximate the NMOS device curve by a straight line OUT-SAT-D, ¾ VDD**

Interpret the straight line as a resistor with **Interpret the straight line as a resistor with**

 $1/({\rm slog}) = {\rm R}$ 

 $=\frac{3}{\Lambda}$   $\sqrt{\frac{1}{\text{D}}}$   $\sqrt{\frac{1}{\text{N}}\text{N}}$   $\frac{1}{\text{N}}$ 

 $1/(slop) = R = \frac{3}{4} V_D V_{SAT}$ 

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Version Date 04/03/03 **Version Date 04/03/03**

# Switched Equivalent Resistance Values **Switched Equivalent Resistance Values**

geometrical layout, design style and technology node. **geometrical layout, design style and technology node.** The resistor values depend on the properties of silicon,  **resistor values depend on the properties of silicon,** 

higher than p-type. n-type silicon has a carrier mobility that is 2 to 3 times **higher than p-type. n-type silicon has a carrier mobility that is 2 to 3 times** 

width/length in the geometrical layout. **width/length in the g** The resistance is inversely proportion to the gate **The resistance is inversely proportion to the gate eometrical layout.**

predetermined fixed size **predetermined fixed size. Design styles may restrict all NMOS and PMOS to be of a**  Design styles may restrict all NMOS and PMOS to be of a

inversely with the linewidth. **inversely with the line** The current per unit width of the gate increases nearly **The current per unit width of the gate increases nearly** 

#### **For convenience in EE 42 we assume R<sub>D</sub> = RU = 10 k** $\bf C$





 $\circ$ 

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#### Additional Steps for CMOS Additional Steps for CMOS

#### **Well Formation Well Formation**



Process (before transistor fabrication) **Process (before transistor fabrication)**

- **1. start with p-type wafer; grow 250 nm oxide** 1. start with p-type wafer; grow 250 nm oxide
- 2. pattern oxide with n-well mask **2. pattern oxide with n-well mask**
- 3. implant with phosphorus and anneal to form a 3 **3. implant with phosphorus and anneal to form a 3** hm-deep n-type region μ**m-deep n-type region**

 $\overline{\phantom{0}}$ 



## **AND ONE MORE COMPLICATION: AND ONE MORE COMPLICATION:**

We need contacts to "vell and body" or well and body of p-region We need contacts to "body" or well and body of p-region

Easy to do - just modify "select" masks and oxide masks, i.e., Easy to do – just modify "select" masks and oxide masks, i.e.,

① Create thin oxide spots for contact in original oxide mask, and Create thin oxide spots for contact in original oxide mask, and

2 Allow openings in select masks to dope these regions Allow openings in select masks to dope these regions



p implant area in substrate is to make electrical contact by Al wire easier p implant area in substrate is to make electrical contact by Al wire easier

How to get n-regions implanted selectively with arsenic? How to get n-regions implanted selectively with arsenic?

Could simply invert polarity of select mask at contacts. Could simply invert polarity of select mask at contacts.

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Basic CMOS Process **Basic CMOS Process**

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# Well mask + select mask(s) + NMOS process **Well mask + select mask(s) + NMOS process**

W Oldham

#### Separate Masks Separate Masks

## Well, oxide, and polysilicon masks **Well, oxide, and polysilicon masks**





Separate Masks (cont.)

Separate Masks (cont.)

**Select masks, contact mask, and metal mask**

Select masks, contact mask, and metal mask

#### **CMOS Process Sequence CMOS Process Sequence**

- **1. p-type starting material; grow 500 nm of oxide** 1. p-type starting material; grow 500 nm of oxide
- **2. pattern oxide with well mask** 2. pattern oxide with well mask
- **3. implant phosphorus and anneal ("well drive in") to a depth** 3. implant phosphorus and anneal ("well drive in") to a depth **of 3** μ**m**
- **4. strip off oxide** 4. strip off oxide
- **5. grow 500 nm of oxide** 5. grow 500 nm of oxide
- **6. pattern with oxide mask** 6. pattern with oxide mask
- **7. grow 5 nm of oxide** 7. grow 5 nm of oxide
- **8. deposit 500 nm of n** 8. deposit 500 nm of n+ polysilicon  **polysilicon**
- **9. pattern with poly mask** 9. pattern with poly mask
- 10. spin on resist **10. spin on resist**
- 11. pattern with the select mask (dark field) **11. pattern with the select mask (dark field)**
- 12. implant boron; strip off resist **12. implant boron; strip off resist**
- 13. spin on resist **13. spin on resist**
- **14. pattern with the select mask (clear field)** 14. pattern with the select mask (clear field)

and substrate except for well contacts Same pattern and substrate except for well Same pattern

### **CMOS Process Sequence (cont.) CMOS Process Sequence (cont.)**

- 15. implant arealimplants to dist and anneal implants to from **15. implant arsenic; strip off resist and anneal implants to form** source and drain regions **source and drain regions**
- 16. deposit 500 nm of oxide **16. deposit 500 nm of oxide**
- 17. pattern using contact mask (dark field) **17. pattern using contact mask (dark field)**
- 18. deposit 1 um of aluminum **18. deposit 1**  μ**m of aluminum**
- 19. pattern using metal mask (clear field) **19. pattern using metal mask (clear field)**

# CMOS Cross Sections CMOS Cross Sections





- Completed our propogation delay model
- Switch-RC model <u>ር</u> the<br>O CMOS inverter
- and calculations
- CMOS layouts and<br>D fabrication steps
- References: Lectures  $\overset{\rightharpoonup }{\infty }$ and<br>D د<br>ت (Fall 1999) and<br>D Lecture  $\geq$ (Spring 2003)



- Barring unforseen circumstances: GUEST LECTURE —<br>ズ **PROF.** TSU JAE-KING
- H<br>N #5 due!
- START PREPARING T<br>R<br>R MIDTER<br>MIDTER