Pipeline Practice and Making Resistors

Lecture 34, 11/23/05

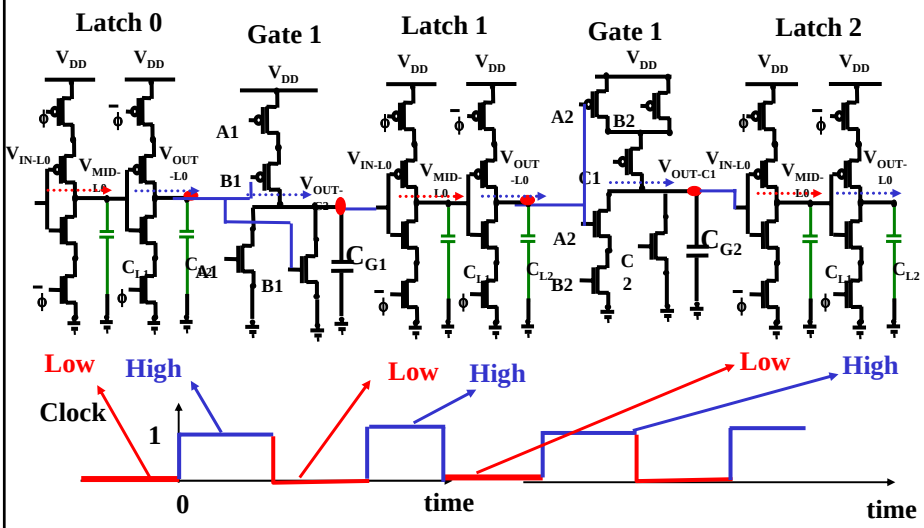
OUTLINE

- Pipelining Practice
- Resistance and Sheet Resistance
- Implant Sheet Resistance
- Layout definition of resistance values

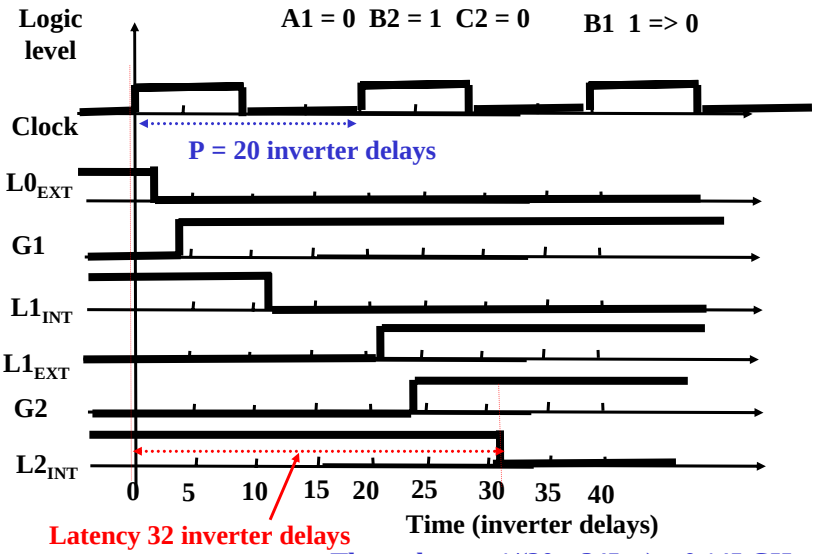
Reading

These presentation slides only

Latch Operation: Pipelined

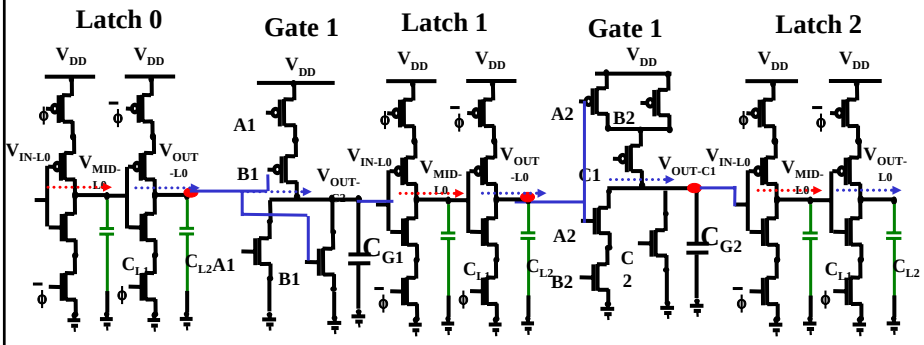


Latch Timing Diagram



Throughput = 1/(20 x 345ps) = 0.145 GHz

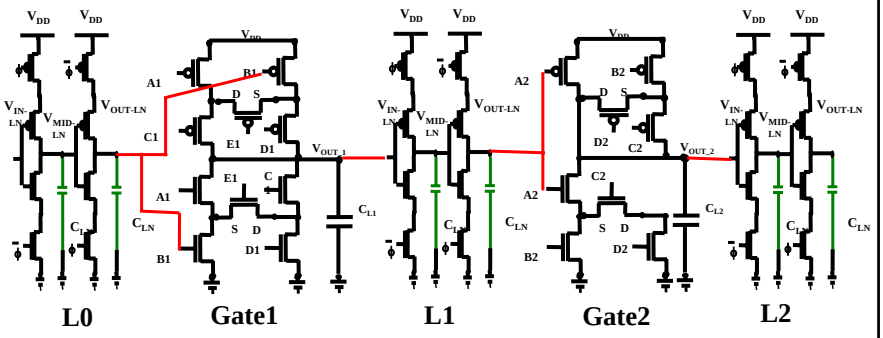
Clock Optimization: Pipelined



$\tau_{HIGH} = \tau_{L_EXT} + \max(\tau_{GATE1}, \tau_{GATE2})$

$\tau_{LOW} = \tau_{L_INT}$

Logic Pipeline: Example #2



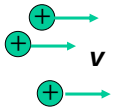
$\tau_{HIGH} = \tau_{L_EXT} + \max(\tau_{GATE1}, \tau_{GATE2})$

$\tau_{LOW} = \tau_{L_INT}$

Current Density

The current density ***J*** is the current per unit area (***J*** = ***I*** / ***A*** ; ***A*** is the cross-sectional area of the conductor)

If we have ***N*** positive charges per unit volume moving with average speed ***v*** in the +***x*** direction, then the current density in the +***x*** direction is just ***J*** = ***qNv***

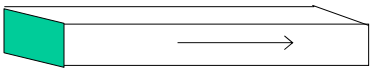


Example:

2×10^{16} holes/cm^3 moving to the right at 2×10^4 cm/sec

$J = 1.6 \times 10^{-19} \times 2 \times 10^{16} \times 2 \times 10^4 = 64$ A/cm^2

Suppose this occurs in a conductor 2 μm wide and 1 μm thick:



$I = J \times A = 64 \times (2 \times 10^{-4} \times 1 \times 10^{-4})$

$= 1.28$ μA

Electrical Conductivity σ

When an electric field is applied, current flows due to drift of mobile electrons and holes:

electron current density: $J_n = (-q)nv_n = qn\mu_n E$

hole current density: $J_p = (+q)pv_p = qp\mu_p E$

total current density: $J = J_n + J_p = (qn\mu_n + qp\mu_p)E$

$$J = \sigma E$$

conductivity $\sigma \equiv qn\mu_n + qp\mu_p$ (Units: Ω-cm^{-1})

Electrical Resistivity ρ

$$\rho \equiv \frac{1}{\sigma} = \frac{1}{qn\mu_n + qp\mu_p}$$

$\rho \cong \frac{1}{qn\mu_n}$ **for n-type mat'l**

$\rho \cong \frac{1}{qp\mu_p}$ **for p-type mat'l**

(Units: ohm-cm)

Example Calculation of Resistivity

Consider a Si sample doped with 10^{16}/cm^3 Boron. What is its resistivity?

Answer:

$N_A = 10^{16}/\text{cm}^3$, $N_D = 0$ ($N_A >> N_D$ → p-type)

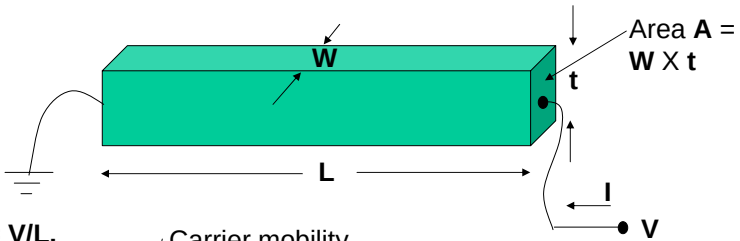
→ $p \approx 10^{16}/\text{cm}^3$ and $n \approx 10^4/\text{cm}^3$

$$\rho = \frac{1}{qn\mu_n + qp\mu_p} \cong \frac{1}{qp\mu_p}$$

$$= \left[(1.6\times10^{-19})(10^{16})(450)\right]^{-1} = 1.4\,\Omega - \text{cm}$$

From μ vs. ($N_A + N_D$) plot

Physics of Current Flow, Resistance, Resistivity



E = V/L.

I = V/R

R = ρL/A **=(1/q μN) L/W t = (L/W) /μ(qNt)**

Carrier mobility

Carriers per unit volume

But **q N t** has the dimensions of charge per unit area and represents the charge per unit area in a film of thickness **t** when the film has **N** carriers/cm^3 and is **t** units thick. Thus we call **q N t** the "**Q**" and

R = (L/W)/ μQ = L/W $R_{\square}$

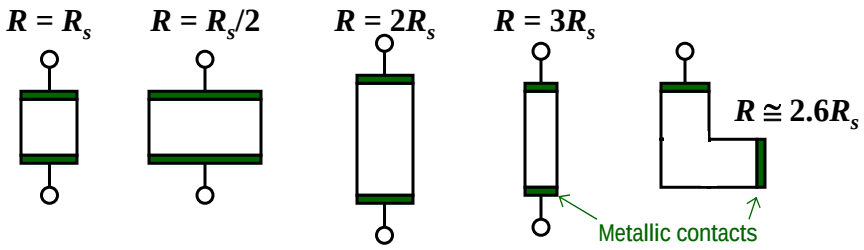
Where $R_{\square}$ is the resistance of a "square" of the film. Clearly if L is four times W, then R = 4 $R_{\square}$.

Sheet Resistance R_s

$$R = \rho\frac{L}{Wt} = R_s\frac{L}{W} \quad \Rightarrow \quad \boxed{R_s \equiv \frac{\rho}{t}}$$ **(Unit: ohms/square)**

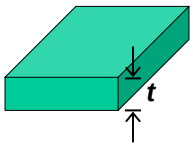
(L, W, t = length, width, thickness) R_s is the resistance when $W = L$

- The R_s value for a given layer in an IC technology is used
  - for design and layout of resistors
  - for estimating values of parasitic resistance in a circuit



Integrated-Circuit Resistors

The resistivity ρ and thickness ***t*** are fixed for each layer in a given manufacturing process



A circuit designer specifies the length ***L*** and width ***W***, to achieve a desired resistance ***R***

$$R = R_s\left(\frac{L}{W}\right)$$

fixed designable

Example: Suppose we want to design a 5 kΩ resistor using a layer of material with R_s = 200 Ω/☐

Resistor layout (top view)

Space-efficient layout

Resistance of Silicon Films (at low E fields)

at low fields $\sigma = q\,N\,\mu$ **where N = n or p and** $\mu = \mu_n$ **or** μ_p

So $\sigma = q\,n\,\mu_n$ for electrons in n-type Si

and $\sigma = q\,p\,\mu_p$ for holes in p-type Si

In other words $R_{\square} = 1/\,\mu_N(qN_Dt) = 1/\,\mu_N(Q_D)$ in N-type Silicon

Where (N_D t) is the number of donors implanted per unit area, and multiplying by **q**, we have the donor charge implanted per unit area. (μ_N is the mobility of the electrons).

Similarly $R_{\square} = 1/\,\mu_P(qN_At) = 1/\,\mu_P(Q_A)$ in P-type Silicon

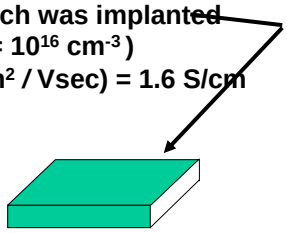
Where (N_A t) is the number of acceptors implanted per unit area, and multiplying by **q**, we have the acceptor charge implanted per unit area.

We do not need uniformly doping versus depth!

Silicon Resistor by Ion Implantation

***Example*: 1 μm thick n-type silicon layer which was implanted with 10^{12} donors cm^{-2}. (Thus $N_d = 10^{12} / 10^{-4} = 10^{16}$ cm^{-3})**

$\sigma = q\,n\,\mu_n = (1.6 \times 10^{-19}$ C) (10^{16} cm^{-3}) (1000 cm^2 / Vsec) = 1.6 S/cm



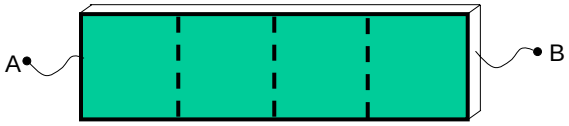
$\rho = 1 / \sigma = 0.625\ \Omega$ cm

Sheet resistivity, $R_{\square}$ given by:

$R_{\square} = [1/(\sigma\,t)] = 6.25$ K Ω/square

But this can be obtained directly from the implant "**Q**" of $1.6 \times 10^{-19} \times 10^{12} = 1.6 \times 10^{-7}$ thus

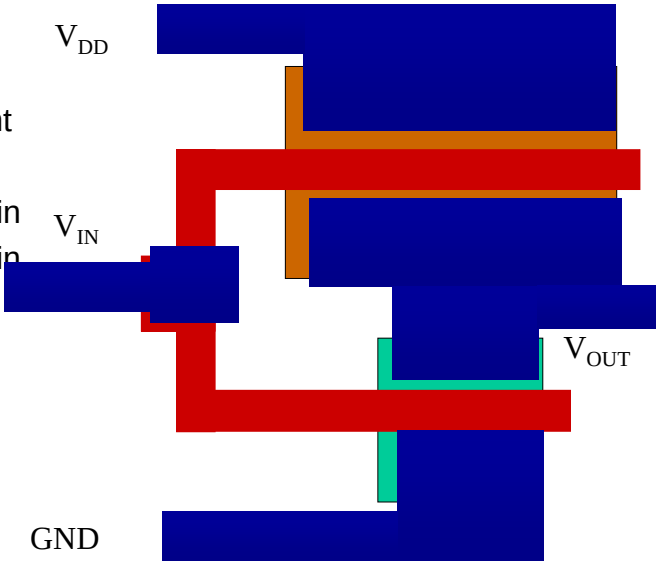
$R_{\square} = [1/(Q\,\mu)] = 6.25$ K Ω/square



R_{AB} = ?

R_{AB} = 4 X 6.25
= 25 KΩ

Device Layout and Process

Process Flow

- Active Area
- n-Well Implant
- Poly
- n Source/Drain
- p Source/Drain
- Insulator
- Contacts
- Metal