CMOS Static Summary and Layout

Lecture 30, 11/14/05

OUTLINE

• Midterm #2 Results
• Overview of EE40 Lab Project
• Summary of CMOS Static Analysis
• CMOS Layout Example

Reading
These presentation slides only

Midterm #2 Results

<table>
<thead>
<tr>
<th>A-F Front Left</th>
<th>G-L Front Right</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rough Scale</td>
<td>Rough Scale</td>
</tr>
<tr>
<td>P1</td>
<td>P2</td>
</tr>
<tr>
<td>45</td>
<td>32</td>
</tr>
<tr>
<td>MEAN</td>
<td></td>
</tr>
<tr>
<td>41.2</td>
<td>26.2</td>
</tr>
<tr>
<td>4.8</td>
<td>7.7</td>
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<tr>
<td>0.91</td>
<td>0.65</td>
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<tr>
<td>0.12</td>
<td>0.30</td>
</tr>
<tr>
<td>Standard deviation</td>
<td>Standard deviation/AVE</td>
</tr>
<tr>
<td>82.1</td>
<td>14.7</td>
</tr>
<tr>
<td>55</td>
<td>61</td>
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</tbody>
</table>
| Re-grade only for 4 or more points: Write specific request on cover and return to Prof. Neureuther by end of class 11/14/05.

EE40 Lab Project: Scope

Objective

• The student will understand and make design trade-offs in a computerized electronic measurement system for investigating an exploratory electronic Circuit Under Test.

Overview

• The emphasis is on developing an integrated environment for automatically testing, evaluating and controlling an electronic circuit.
• The project is based on the use of LABVIEW for automation, SPICE or MultiSim for circuit simulation, Op-Amp buffer circuits for extracting measurements and MOSFET circuits for implementing controls that interact with the Circuit Under Test.

EE40 Lab Project: Circuit Under Test

• A good candidate is cross-coupled Op-Amps with capacitors in the feedback circuits.
• This circuit produces a pair of coupled rate equations with damping.
• These equations might correspond to the difference from equilibrium of concentrations in a chemical reaction or even populations of species in an environmental system.
• The coefficients of the rate equations can be set by adjusting the resistor values.
• By pre-charging the capacitors to various voltages and switching them into the circuit various initial conditions can be applied.

CMOS Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.

Voltage Transfer Function for the CMOS Inverter Circuit

Load only affects transient
Find Points That Satisfies Both Devices for Each $V_{IN}$

![Graph showing the intersection of different lines for $V_{IN}$ values of 0, 3, and 5, indicating solution points.]

CMOS Static Behavior is Nearly Ideal

- Voltage Transfer Function (VTC) nearly Ideal
  - Transition is near $V_{DD}/2$ => good noise margins
  - Very high slope => regenerate signals
- Pull-up and Pull-Down devices are off when input is within a threshold voltage of 0 or $V_{DD}$ => No short-circuit current
- Leakage orders of magnitude lower than on current => low static power

MOSFET Models

1. $I_D$ is reduced by the voltage drop along the channel
2. $I_D$ is reduced when carriers reach the velocity limit

![Graphs illustrating MOSFET models with curves for velocity saturation and pinch-off.]

CMOS Device and Process Flow

Start with p-type wafer
- Create N-Well
- Grow oxide
- Remove it in transistor areas
- Grow gate oxide
- Grow and pattern polysilicon for gates
- Dope n-channel source and drains
- Dope p-channel source and drains
- Deposit oxide over gates
- Pattern contacts
- Deposit and Pattern Metal
- Need to protect p-mos areas
- Need to protect n-mos areas

It looks like we need three more masks than in NMOS

Device Layout and Process

Process Flow:
- Active Area
- n-Well Implant
- Poly
- n Source/Drain
- p Source/Drain
- Insulator
- Contacts
- Metal

![Diagram of device layout and process flow with symbols for VDD, GND, VIN, VOUT, VDD, and VGND.]

Device Layout Compensates Mobility Diff.

- The desired device current drive can be changed by adjusting the W/L of the device layout.
- For better balance the lower mobility PMOS ($200 \text{ cm}^2/\text{Vs}$) pull-up device can be made larger than the higher mobility ($500 \text{ cm}^2/\text{Vs}$) NMOS pull-down device.