CMOS Static Summary and Layout

Lecture 30, 11/14/05

OUTLINE

- Midterm #2 Results
- Overview of EE40 Lab Project
- Summary of CMOS Static Analysis
- CMOS Layout Example

Reading

These presentation slides only

Midterm #2 Results

A-F Front Left **G-L Front Right**

	P1	P2	P3	TOT
	45	32	33	110
MEAN	41.2	26.2	14.7	82.1
standard deviation	4.8	7.7	7.5	15.7
MEAN/Value	0.91	0.65	0.42	0.75
Standard deviation/AVE	0.12	0.30	0.51	0.19

Rough Scale

A = 94
A- = 89
B+ = 84
B = 78
B- = 73
C+ = 67
C = 61
C- = 55
D+ = 48

Re-grade only for 4 or more points: Write specific request on cover and return to Prof. Neureuther by end of class 11/14/05.

M-S Rear Left **T-Z Rear Right**

EE40 Lab Project: Scope

Objective

- The student will understand and make design trade-offs in a computerized electronic measurement system for investigating an exploratory electronic Circuit Under Test.

Overview

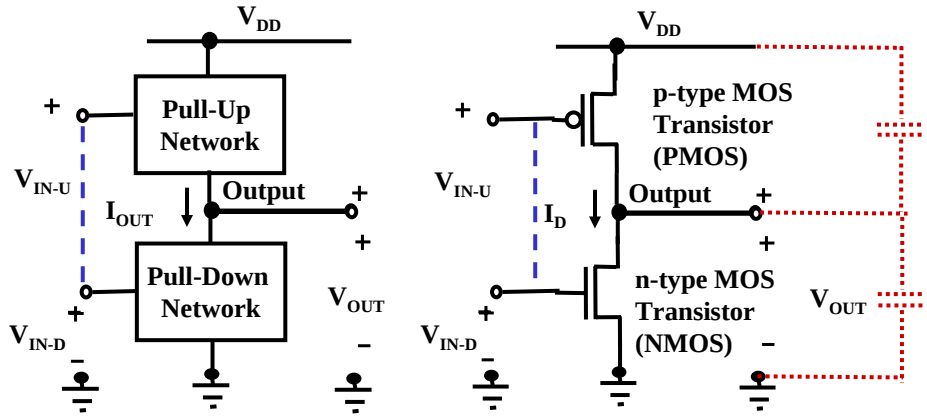
- The emphasis is on developing an integrated environment for automatically testing, evaluating and controlling an electronic circuit.
- The project is based on the use of LABVIEW for automation, SPICE or MultiSim for circuit simulation, Op-Amp buffer circuits for extracting measurements and MOSFET circuits for implementing controls that interact with the Circuit Under Test.

EE40 Lab Project: Circuit Under Test

- A good candidate is cross-coupled Op-Amps with capacitors in the feedback circuits.
- This circuit produces a pair of coupled rate equations with damping.
- These equations might correspond to the difference from equilibrium of concentrations in a chemical reaction or even populations of species in an environmental system.
- The coefficients of the rate equations can be set by adjusting the resistor values.
- By pre-charging the capacitors to various voltages and switching them into the circuit various initial conditions can be applied.

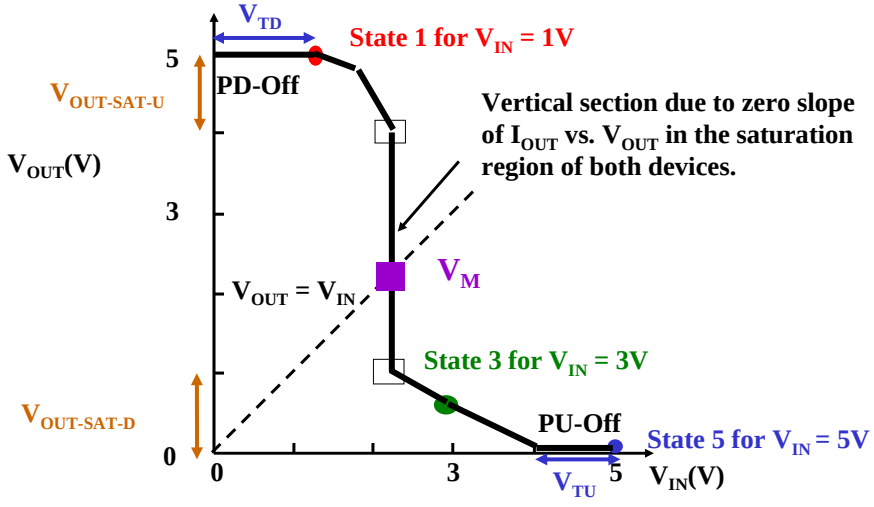
CMOS Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.

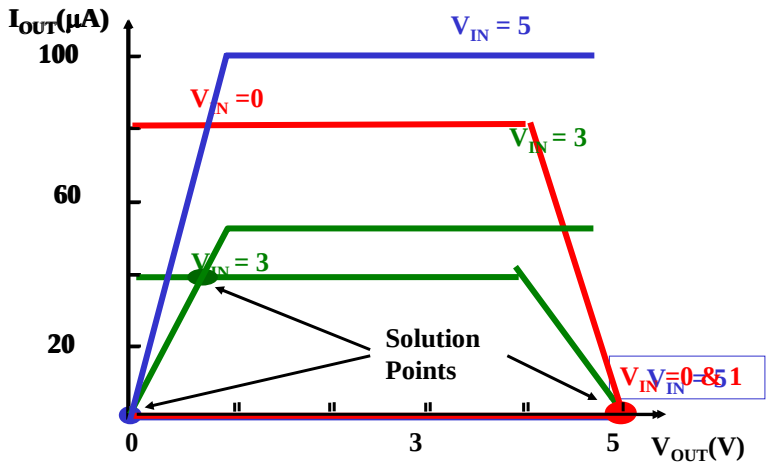


Load only affects transient

Voltage Transfer Function for the CMOS Inverter Circuit



Find Points That Satisfies Both Devices for Each V_{IN}

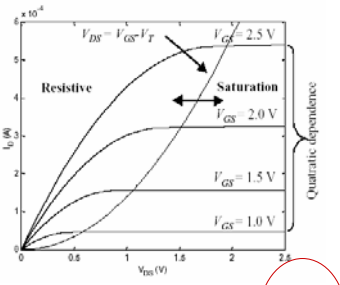


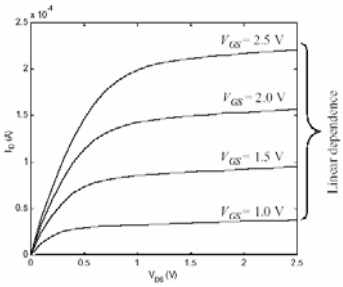
CMOS Static Behavior is Nearly Ideal

- Voltage Transfer Function (VTC) nearly Ideal
  - Transition is near $V_{DD}/2$ => good noise margins
  - Very high slope => regenerate signals
- Pull-up and Pull-Down devices are off when input is within a threshold voltage of 0 or V_{DD} => No short-circuit current
- Leakage orders of magnitude lower than on current => low static power

MOSFET Models

1. I_D is reduced by the voltage drop along the channel
2. I_D is reduced when carriers reach the velocity limit





$$I_D = k_n' \frac{W}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

where $k_n' = \mu_n C_{ox}$

$$I_{DSAT} = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

where $k_n' = \mu_n C_{ox}$

Pinch-Off

$$I_{DSAT} = WC_{ox}\left[V_{GS} - V_T - \frac{V_{DSAT}}{2}\right]v_{sat}$$

where $V_{DSAT} = \frac{L}{\mu_n}v_{sat}$

Velocity Saturation

CMOS Device and Process FLow

Start with p-type wafer

Create N-Well

Grow thick oxide

Remove it in transistor areas

Grow gate oxide

Grow and pattern polysilicon for gates

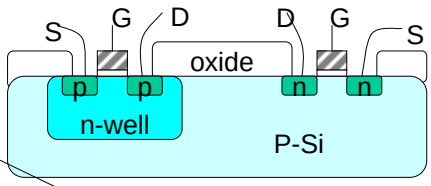
Dope n channel source and drains

Dope p-channel source and drains

Deposit oxide over gates

Pattern contacts

Deposit and Pattern Metal



New for CMOS

Need to protect p-mos areas

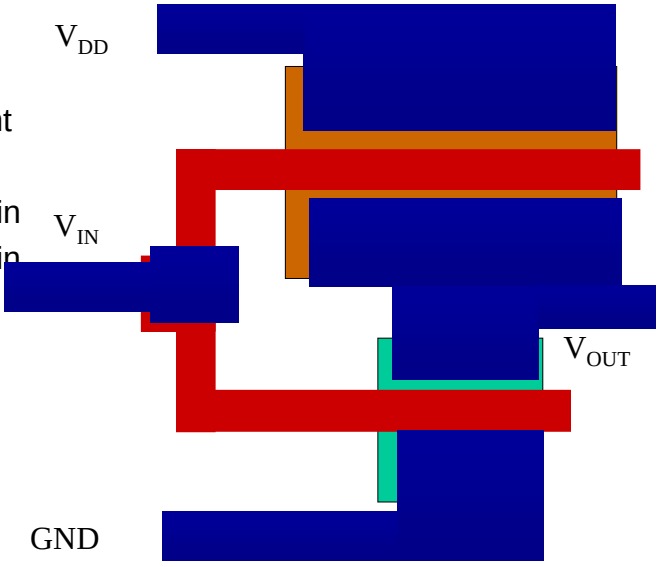
Need to protect n-mos areas

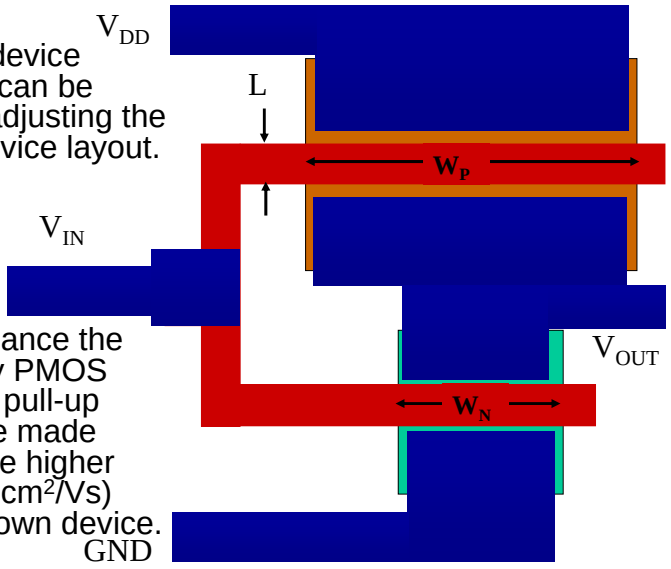
It looks like we need three more masks than in NMOS

Device Layout and Process

Process Flow

- Active Area
- n-Well Implant
- Poly
- n Source/Drain
- p Source/Drain
- Insulator
- Contacts
- Metal



Device Layout Compensates Mobility Diff.

- The desired device current drive can be changed by adjusting the W/L of the device layout.
- For better balance the lower mobility PMOS (200 cm^2/Vs) pull-up device can be made larger than the higher mobility (500 cm^2/Vs) NMOS pull-down device.