CMOS Inverter Analysis

Lecture 28, 11/04/05

OUTLINE
• Need for Input Controlled Pull-Up
• Trial and Error Investigation of Devices
• Velocity Saturation PMOS_40VS
• CMOS Inverter Analysis
• CMOS Voltage Transfer Characteristic

Reading
Not covered in Hambley
=> Mainly these Presentation Slides

Velocity Saturation MOSFET Model NMOS_4XVS

Current $I_{OUT}$ only flows when $V_{IN}$ is larger than the threshold value $V_{TD}$ and the current is proportional to $V_{OUT}$ up to $V_{OUT-SAT-D}$ where it reaches the saturation current

$$I_{OUT-SAT-D} = k_D(V_{IN} - V_{TD})$$

Note that we have added an extra parameter to distinguish between threshold ($V_{TH}$) and saturation ($V_{OUT-SAT-D}$).

Example:

- $k_D = 25 \, \mu A/V^2$
- $V_{TD} = 1V$
- $V_{OUT-SAT-D} = 1V$

Use these values in the homework.

Composite Current Plot for an NMOS Inverter

$V_{IN} = 0$ & $1$

$I_{OUT}$

$V_{OUT}$

$V_{TH}$

$V_{DD}$

$R_{PULL-UP}$

$V_{HEVENS}$

$R_{LOAD}$

Composite Current of NMOS Inverter with 200kΩ Load

$V_{IN} = 0$ & $1$

$I_{OUT}$

$V_{OUT}$

$V_{DD}$

$R_{PULL-UP}$

$V_{HEVENS}$

$R_{LOAD}$
Voltage Transfer Function NMOS Inverter w/wo Load

Complete a VTC like this for the device in the Homework

Problems in the NMOS Inverter

Problem #1: Current when VOUT is low
Problem #2: High value of VOUT is adversely affected by a load resistor.
Missed Opportunity: The value of the input control signal is not used to adjust the state of the pull-up device.

What if: If the pull-up device could be a state-dependent device what kind of device would we want?

Problems and Opportunities in Logic Circuit Design

Problem #1: Significant wasted current and power when VOUT is low.
Problem #2: High value of VOUT is adversely affected by a load resistor.

Missed Opportunity: The value of the input control signal is not used to adjust the state of the pull-up device.

What if: If the pull-up device could be a state-dependent device what kind of device would we want?

Pull-Up Device Design: Trial 1

Problem #1 is worse! There is even more wasted current and power than before when VOUT is low.

Look for a more Complementary approach.

Note that in the pull-down case the current decreases.

Pull-Down and Pull-Up Must Complement Rather Than Fight Each Other

Reduce the Short-Circuit Current by making either one or the other device off.
Desirable Complementary Device Characteristics

- **VDD**
- **VOUT**
- **IOUT**
- **VIN**

We desire characteristics that are complementary for the pull-down and pull-up state-dependent devices.

<table>
<thead>
<tr>
<th></th>
<th>Low</th>
<th>High</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pull-Down</td>
<td>Low not leak</td>
<td>High Discharge Output</td>
</tr>
<tr>
<td>Pull-Up</td>
<td>High Charge Output</td>
<td>Low not leak</td>
</tr>
</tbody>
</table>

Designing the Complementary Device

The curve sets are very similar but have two key changes.

- The creation of current with input State (VIN) is reverse ordered (and also shifted).
- The dependence on VOUT in reverse ordered and shifted by VDD.

Velocity Saturation PMOS_4XVS

Current I_{OUT} only flows when VIN is smaller than VDD minus the threshold value V_{TU} and the current is proportional to (V_{DD}V_{OUT}) up to (V_{DD}V_{OUT-SAT-U}) where it reaches the saturation current

\[ I_{OUT-SAT-U} = k_U(V_{DD} - V_{IN} - V_{TU}) \]

Example:

- k_u = 20 \mu A/V^2
- V_{TU} = 1V
- V_{OUT-SAT-U} = 1V

\[ I_{OUT} = \frac{20 \mu A}{V^2} \]

PMOS_40VS Pull-UP I_{OUT} vs. V_{OUT}

Evaluating the point where V_{OUT} = V_{DD} - V_{TU} for a given VIN allows the entire curve to be sketched.

CMOS Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.

<table>
<thead>
<tr>
<th>Push-Up Network</th>
<th>Output</th>
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<tbody>
<tr>
<td>VIN</td>
<td>V_{OUT}</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pull-Down Network</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN_D</td>
<td>V_{IN-D}</td>
</tr>
</tbody>
</table>

p-type MOS Transistor (PMOS)

n-type MOS Transistor (NMOS)
Case #1: \( V_{\text{IN}} = V_{\text{DD}} = 5\text{V} \Rightarrow \text{Output Low} \)

The PMOS transistor is OFF when \( V_{\text{IN}} > V_{\text{DD}} - V_{\text{TU}} \)

The NMOS transistor is ON when \( V_{\text{IN}} > V_{\text{T}} \)

\[
\begin{align*}
V_{\text{OUT}}(V) & = 0 \quad \text{when} \quad V_{\text{IN}} = V_{\text{DD}} = 5\text{V} \\
I_{\text{OUT}}(\mu \text{A}) & = 100 \quad \text{at} \quad V_{\text{OUT}} = 0
\end{align*}
\]

Case #2: \( V_{\text{IN}} = 0 \Rightarrow \text{Output High} \)

The PMOS transistor is ON when \( V_{\text{IN}} < V_{\text{DD}} - V_{\text{TU}} \)

The NMOS transistor is OFF when \( V_{\text{IN}} < V_{\text{T}} \)

\[
\begin{align*}
V_{\text{OUT}}(V) & = 5 \quad \text{when} \quad V_{\text{IN}} = 0 \\
I_{\text{OUT}}(\mu \text{A}) & = 100 \quad \text{at} \quad V_{\text{OUT}} = 5
\end{align*}
\]

Composite \( I_{\text{OUT}} \) vs. \( V_{\text{OUT}} \) for CMOS_4XVS

Find Points That Satisfies Both Devices for Each \( V_{\text{IN}} \)

Voltage Transfer Function for the CMOS_4XVS

Method for Finding \( V_{\text{M}} \)

At \( V_{\text{M}} \):
1) By definition \( V_{\text{OUT}} = V_{\text{IN}} = V_{\text{M}} \)
2) Both devices are in saturation
3) \( I_{\text{OUT-SAT-D}} = I_{\text{OUT-SAT-U}} \)

\[
\begin{align*}
I_{\text{OUT-SAT-D}} & = k_D (V_{\text{IN}} - V_{\text{T}}) V_{\text{OUT-SAT-D}} \\
I_{\text{OUT-SAT-U}} & = k_U (V_{\text{DD}} - V_{\text{OUT}} - V_{\text{T}}) V_{\text{OUT-SAT-U}}
\end{align*}
\]

Substitute \( V_{\text{M}} \)

Solve for \( V_{\text{M}} \)

Example Result: When \( k_D = k_U \), \( V_{\text{OUT-SAT-D}} = V_{\text{OUT-SAT-U}} \)
and \( V_{\text{TD}} = V_{\text{T}} \), then \( V_{\text{M}} = V_{\text{DD}}/2 \)