MOSFET Physical Parameters

OUTLINE
• Midterm #2 Coverage
• Midterm #2 Review
• MOSFET I-V for Pinch-Off
• MOSFET I-V for Velocity Saturation
• MOSFET Load Line

Reading
Hambley 12.1-12.2
And these presentation slides

Midterm #2 Coverage
Three Main Topics: (likely 3 questions)
• Phasors (V, I, and Z) and Bode Plot (Mag and phase of Vout/Vin versus ω). Hambley 5.1-5.6 and 6.1-6.6
• Ideal Op-Amp Circuits Hambley 14.1-14.5 and 14.9-14.10 light
• Diode Circuits (Logic and General) Hambley 10.1-10.7
Use material from Midterm #1 as tools:
• Loop and node analysis
• Dependent sources, equivalent circuits
• Simple transients (not too likely)

Phasors
Homework example of a 1000 ohm load at an angle of 30 degrees driven by a 120V rms cos(ωt), where ω = 2π/60.

All V and I values in rms.

Bode Plot of Magnitude and Phase

Phasor equation:

Cascade Op-Amp Circuit Analysis

Digital Logic: Diodes with Dependent Sources

• EE40 TTL (Transistor-Transistor Logic

In case you are interested: True TTL has at least three dependent sources that are associated with the three bipolar transistors on which it is based.
Signal Shaping Diode Circuits

Level Shift  Peak Detect
The final output is the peak to peak voltage of the input.

Finding Physical Parameters for MOSFETs
Revisit where these models come from via the next few slides.

Pure Si: intrinsic Carriers
Covariant (shared e⁻) bonds exists between Si atoms in a crystal. Since the e⁻ are loosely bound, some will be free at any t, creating holes.

\[ \eta_i = 3.9 \times 10^{16} \text{ cm}^{-3} \]
\[ n_i \approx 10^{10} \text{ cm}^{-3} \text{ at room temperature} \]

Drift Velocity and Carrier Mobility
Mobile charge-carrier drift velocity is proportional to applied E-field:

\[ |v| = \mu E \]
\[ \mu \text{ is the mobility} \]
(Units: cm²/V·s)

Note: Carrier mobility depends on total dopant concentration \((N_D + N_A)\)!

Charge Control Experiment – “The Field Effect”
Above some "threshold" voltage \(V_t\), the number of electrons per square cm under the gate is proportional to \(v_{sa} - V_t\), i.e., the charge \(Q_o\) is proportional to \(v_{sa} - V_t\).

\[ Q_o = \eta_{ox} (v_{gs} - V_t) \]
\[ \text{charge for unit area} \]
\[ \text{onset of charge formation by field effect} \]

These charge carriers can carry current from D to S, so we can make low resistance \(R_{DS} \) by making \(v_{sa} - V_t\) very large.

N-MOS I-V Characteristics
At low \(V_{GS}\) we have:

\[ i_D = \frac{W}{L} v_{gs} \quad \frac{V_{gs}}{V_{TH}} < 1 \]
\[ i_D \approx \frac{W}{L} \mu C_V (V_{gs} - V_t) \]
At high drain voltage \(V_{DS}\) the current stops rising (saturates) due to:
- Voltage increase by \(V_{DS}\) along channel reduces local excess gate voltage even to zero (Pinch-Off).
- Electrons reach their velocity saturation limit
MOSFET at High V_{DS}

DEVICE IN CROSS-SECTION

“Metal” “Oxide” “Semiconductor”

• Above a certain gate to source voltage V_t (the “threshold”), electrons are induced at the surface beneath the oxide. (Think of it as a capacitor.)

• These electrons can carry current between S and D if a voltage is applied.

• At high V_{DS}, a voltage drop appears along the channel and Pinches Off the current when V_{DS} = V_{GS} - V_t.

• At this maximum current the average channel voltage is V_{DS}/2

Charge Drift in Silicon: Low Field

At low electric fields, the average speed of carriers is proportional to the field with proportionality constant \( \mu \). In fact drift velocity = \( \mu E \) for holes = \( -\mu_n E \) for electrons:

\[
\mu \approx \frac{\text{Charge Drift in Silicon: Low Field}}{10^2 \text{cm}^2/\text{v-sec}}, \quad (\text{or} \ 10^3 \text{Km}^2/\text{v-sec})
\]

\[
\mu = 500 \text{ cm}^2/\text{v-sec}
\]

Charge Drift in Silicon: High Field

But at high electric fields, the average speed of carriers is NOT proportional to the field; that is the mobility concept fails. In fact velocity saturates at \( 10^7 \text{ cm/sec} \) for both electrons and holes:

\[
\text{Velocity Saturation}
\]

Digital Logic from State-Dependent Three-Terminal Devices

Three-terminal devices such as MOS transistors have output characteristics (such as I_{OUT} vs. V_{OUT} curves) on the output side that can be programmed by changing signals on the input side (such as the input voltage).

The input voltage V_{IN} can thus be viewed as changing or programming the ‘State’ of the output of the device.

Three-terminal devices whose input voltage V_{IN} or ‘State’ can be programmed can be used to make digital logic devices for computers whose outputs respond to input signals.
State-Dependent Device $I_{OUT}$ vs. $V_{OUT}$

Depending on the state the output $I_{OUT}$ vs. $V_{OUT}$ is constrained to be on one of these curves by the three-terminal device.

Terminology for a Logic Circuit

- **$V_{IN}$** = Power supply voltage (D is from Drain) we do not draw the symbol.
- **Pull-Up Network** = Set of devices used to carry current from the power supply to the output node to charge the output node to the power supply voltage.
- **Pull-Down Network** = Set of devices used to carry current from the output node to ground to discharge the output node to ground.
- **$V_{TH}$** = Threshold Voltage value of $V_{IN}$ at which the Pull-Down (NMOS transistor) begins to conduct.
- **$I_{OUT-SAT-D}$** = Value of $I_{OUT}$ beyond which the current $I_{OUT-D}$ saturates at the (drain) current saturation value $I_{OUT-SAT-D}$. 

Thevenin Model For Pull-Up Device

For the given state only one point satisfies both the external circuit and the three-terminal device.

Load Line For Pull-Up Device

For a given state only one point satisfies both the external circuit and the three-terminal device.

Voltage Transfer Function for the Logic Circuit

Sketch the curve