MOSFET Physical Parameters

OUTLINE

• Midterm #2 Coverage
• Midterm #2 Review
• MOSFET I-V for Pinch-Off
• MOSFET I-V for Velocity Saturation
• MOSFET Load Line

Reading
Hambley 12.1-12.2
And these presentation slides

Midterm #2 Coverage

Three Main Topics: (likely 3 questions)
• Phasors (V, I, and Z) and Bode Plot (Mag and phase of Vout/Vin versus $\omega$). Hambley 5.1-5.6 and 6.1-6.6
• Ideal Op-Amp Circuits Hambley 14.1-14.5 and 14.9-14.10 light
• Diode Circuits (Logic and General) Hambley 10.1-10.7

Use material from Midterm #1 as tools:
• Loop and node analysis
• Dependent sources, equivalent circuits
• Simple transients (no too likely)
Phasors

Homework example of a 1000 ohm load at an angle of 30 degrees driven by a 120V rms \(\cos(\omega t)\), where \(\omega = 2\pi f\).

All V and I values in rms.

\[
\begin{align*}
Z &= 1000\angle 30^\circ = 866 + j500 \\
V_{rms} &= 120\angle 0 \\
I_{rms} &= \frac{V_{rms}}{Z} \\
KVA &= |V_{rms}| |I_{rms}| = |120\angle 0||0.12\angle -30^\circ| = 14.4\text{ watts} \\
Power &= |I_{rms}|^2 R = |0.12\angle -30^\circ|^2 866 = 12.47\text{ watts}
\end{align*}
\]

Add series capacitor to cancel reactance (Match)

\[
\begin{align*}
Z_{MATCH} &= \frac{1}{j\omega C} + 866 + j500 = 866 \\
I_{rms} &= \frac{V_{rms}}{Z_{MATCH}} = 120\angle 0 \\
\text{Power} &= |I_{rms}|^2 R = |0.1386\angle 0|^2 866 = 16.63\text{ watts}
\end{align*}
\]

Higher local voltage \(V^{R+j\omega L}\) is \(I^{MATCH}(R+j\omega L) = 0.1386[866 + j500] = 138.6\angle 30^\circ\)

Bode Plot of Magnitude and Phase

\[
\begin{align*}
V_{OUT} &= \frac{R_2 + j\omega C_2}{R_1 + j\omega C_1} \\
V_{IN} &= \frac{C_1}{C_2} \left(1 + j\omega R_2 C_2\right) \\
\frac{V_{OUT}}{V_{IN}} &= \frac{R_2 + j\omega C_2}{R_1 + j\omega C_1} \left(1 + j\omega R_2 C_2\right) \\
&= \left(1 + j\omega 100-100^{-4}\right) \\
&= 44.7\angle -63.4^\circ = 33.0\text{dB} \angle -63.4^\circ
\end{align*}
\]

\(\omega \rightarrow 0\) ratio=100
\(\omega \rightarrow \infty\) ratio= 0.1

\(\omega = 1/(R_2 C_2) = 10\)

\(\omega = 1/(R_1 C_1) = 10000\)
Cascade Op-Amp Circuit Analysis

How do you get started on finding $V_O$?

**Hint: Identify Stages**

Hint: $I_{IN2}$ does not affect $V_{O1}$

Digital Logic: Diodes with Dependent Sources

- EE40 TTL (Transistor-Transistor Logic)

In case you are interested: True TTL has at least three dependent sources that are associated with the three bipolar transistors on which it is based.
Signal Shaping Diode Circuits

The final output is the peak to peak voltage of the input.

Finding Physical Parameters for MOSFETs

Revisit where these models come from via the next few slides.
Covalent (shared $e^-$) bonds exist between Si atoms in a crystal. Since the $e^-$ are loosely bound, some will be free at any $T$, creating hole electron pairs.

$n_i = 3.9 \times 10^{16} T^{-3/2} e^{-0.605 eV \over k T} / \text{cm}^3$

$n_i \approx 10^{10} \text{ cm}^{-3} \text{ at room temperature}$

Drift Velocity and Carrier Mobility

Mobile charge-carrier drift velocity is proportional to applied $E$-field:

$$|v| = \mu E$$

$\mu$ is the mobility (Units: cm$^2$/V$\cdot$s)

Note: Carrier mobility depends on total dopant concentration ($N_D + N_A$)!
Charge Control Experiment – “The Field Effect”

Above some “threshold” voltage $V_T$, the number of electrons per square cm under the gate is proportional to $V_{GS} - V_T$, i.e., the charge $Q_N$ is proportional to $V_{GS} - V_T$.

$$Q_N = C_{ox}(V_{GS} - V_T)$$

$C_{ox} = \frac{e_{ox}}{t_{ox}}$

These charge carriers can carry current from D to S, so we can make low resistance ($R_{DS}$) by making $V_{GS} - V_T$ very large.

N-MOS I-V Characteristics

At low $V_{DS}$ we have:

$$I_D = \frac{W}{L} \frac{V_{DS}}{R} = \frac{W}{L} QV = \frac{W}{L} Q \mu V_{DS}$$

$$I_D = \frac{W}{L} \mu C_{ox} (V_{GS} - V_T) \cdot V_{DS}$$

Here $\mu = \mu n V_{DS}$ and $Q = C_{ox} (V_{GS} - V_T)$

$I_D \sim$ product of two voltages

$I_D \sim (V_{GS} - V_T) V_{DS}$

At high drain voltage $V_{DS}$ the current stops rising (saturates) due to:

- Voltage increase by $V_{DS}$ along channel reduces local excess gate voltage even to zero (Pinch-Off).
- Electrons reach their velocity saturation limit.
MOSFET at High $V_{DS}$

- Above a certain gate to source voltage $V_t$ (the “threshold”), electrons are induced at the surface beneath the oxide. (Think of it as a capacitor.)
- These electrons can carry current between S and D if a voltage is applied.
- At high $V_{DS}$ a voltage drop appears along the channel and Pinches Off the current when $V_{DS} = V_{GS} - V_T$.
- At this maximum current the average channel voltage is $V_{DS}/2$

Charge Drift in Silicon: Low Field

At low electric fields, the average speed of carriers is proportional to the field with proportionality constant $\mu$; In fact drift velocity $= \mu E$ for holes $= - \mu_n E$ for electrons:

Example: $\mu_n = 1000 \text{ cm}^2/\text{v-sec}$, (or 10Km$^2$/KV-sec) $\mu_p = 500 \text{ cm}^2/\text{v-sec}$
Charge Drift in Silicon: High Field

But at high electric fields, the average speed of carriers is NOT proportional to the field; that is the mobility concept fails. In fact velocity saturates at $10^7 \text{cm/sec} = 100 \text{ km/sec}$ for both electrons and holes:

This saturation is observable directly in the “resistance” of a silicon resistor at high fields (10KV/cm = 1V/µm)

MOSFET Models

1. $I_D$ is reduced by the voltage drop along the channel
2. $I_D$ is reduced when carriers reach the velocity limit

\[
I_D = k' \frac{W}{L} \left[ V_{ds} - V_F - \frac{V_{gs} - V_T}{2} \right] V_{ds}
\]

where \( k' = \mu \cdot C_{ox} \)

\[
I_{max} = \frac{k' \mu}{2} (V_{gs} - V_T)^2
\]

where \( V_{max} = \frac{1}{\mu} \cdot V_T \)

Pinch-Off

Velocity Saturation
Digital Logic from State-Dependent Three-Terminal Devices

Three-terminal devices such as MOS transistors have output characteristics (such as $I_{\text{OUT}}$ vs. $V_{\text{OUT}}$ curves) on the output side that can be programmed by changing signals on the input side (such as the input voltage).

The input voltage $V_{\text{IN}}$ can thus be viewed as changing or programming the ‘State’ of the output of the device.

Three-terminal devices whose input voltage $V_{\text{IN}}$ or ‘State’ can be programmed can be used to make digital logic devices for computers whose outputs respond to input signals.

State-Dependent Three-Terminal Device Element
Only four states or input values are shown but typically there is a continuum of states.

Depending on the state the output \( I_{OUT} \) vs. \( V_{OUT} \) is constrained to be on one of these curves by the three-terminal device.

**Terminology for a Logic Circuit**

- **\( V_{DD} \)** = Power supply voltage (D is from Drain) we do not draw the symbol.
- **Pull-Up Network** = Set of devices used to carry current from the power supply to the output node to charge the output node to the power supply voltage.
- **Pull-Down Network** = Set of devices used to carry current from the output node to ground to discharge the output node to ground.
- **\( V_{TD} \)** = Threshold Voltage value of \( V_{IN} \) at which the Pull-Down (NMOS transistor) begins to conduct.
- \( V_{OUT-SAT-D} \) = Value of \( V_{OUT} \) beyond which the current \( I_{OUT-D} \) saturates at the (drain) current saturation value \( I_{OUT-SAT-D} \).
Thevenin Model For Pull-Up Device

\[ V_{\text{THEVENIN}} = V_{\text{DD}} \]

\[ I_{\text{OUT SHORT CIRCUIT}} = \left( \frac{V_{\text{DD}}}{R_{\text{PULL UP}}} \right) \]

Example:
\[ V_{\text{DD}} = 5V \text{ and } R_{\text{PULL UP}} = 100k\Omega \]
\[ V_{\text{THEVENIN}} = 5V \]
\[ I_{\text{OUT SHORT CIRCUIT}} = 50 \mu A \]

Load Line For Pull-Up Device

\[ I_{\text{OUT}} \text{ vs. } V_{\text{OUT}} \]
For the Pull-Up Resistor and \( V_{\text{DD}} \)

\[ I_{\text{OUT}} \text{ vs. } V_{\text{OUT}} \] is constrained to be on this line by the circuit external to the three-terminal device
Composite Current Plot for the Logic Circuit
Three-Terminal Device
Plus Load Line for the Pull-Up Device

For a given state only one point satisfies both the external circuit and the three-terminal device.

Note that when $V_{OUT}$ is low current flows and power is consumed.

$V_{IN} = 0 \& 1$

Voltage Transfer Function for the Logic Circuit

Sketch the curve.