Diodes: Rectifiers and Clamp Circuits

Lecture 25, 10/30/05

OUTLINE

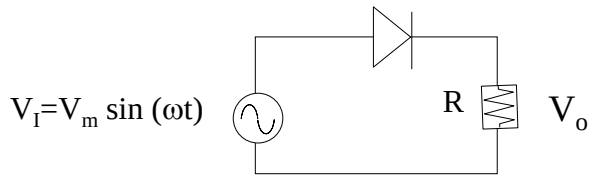
- Half-wave Rectifier
- Clamps and Voltage Doublers using Capacitors (the most challenging circuits in EE40)
- (EE 105 Small Signal Model)

Reading

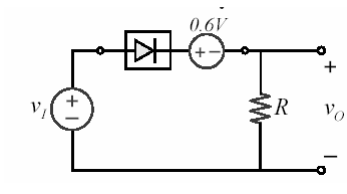
Hambley 10.5-10.8

Power Conversion Circuits

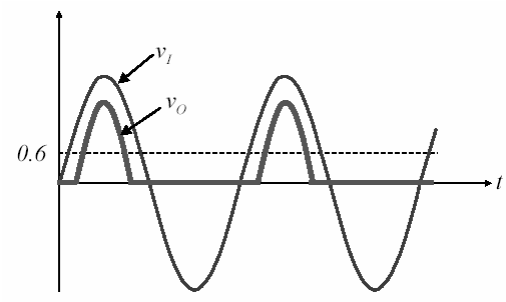
- Converting AC to DC
- Potential applications: Charging a battery



Rectifier Equivalent circuit

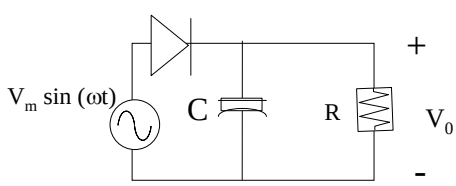


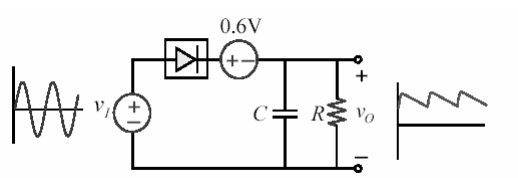
V>0.6V, diode = short circuit
→ $V_o=V_I-0.6$
V<0.6V, diode = open circuit
→ Vo=0



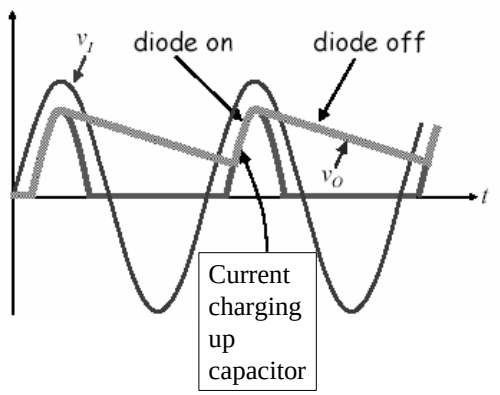
Half-wave Rectifier Circuits

- Adding a capacitor: what does it do?

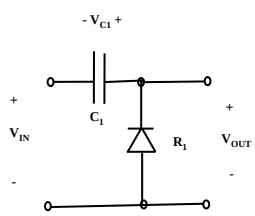


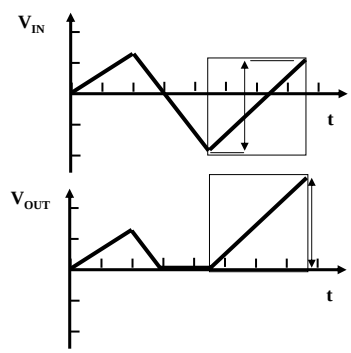


Half-Wave Rectifier



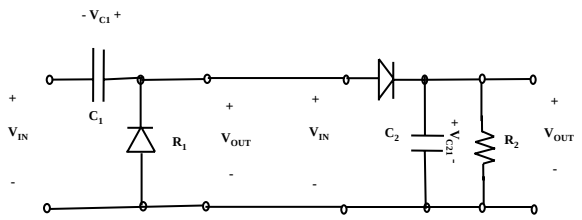
Level Shift Circuit





Once the capacitor is charged by the negative most voltage the rest of the signal is shifted up by that amount.

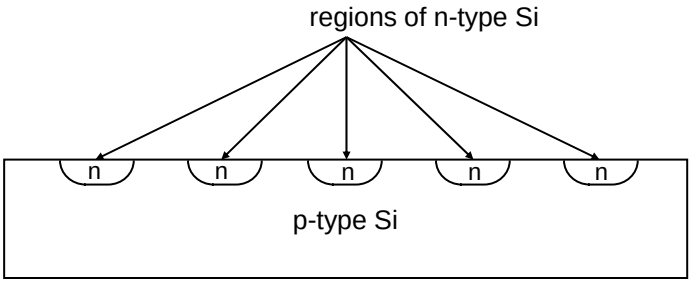
Voltage Doubler Circuit



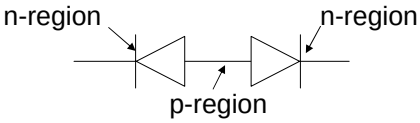
Level Shift Peak Detect

The final output is the peak to peak voltage of the input.

Device Isolation using pn Junctions



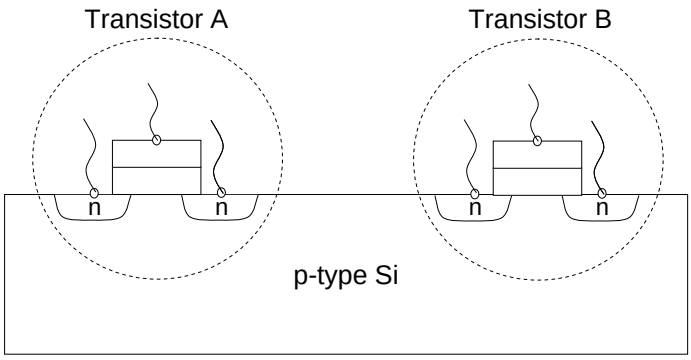
No current flows if voltages are applied between n-type regions, because two pn junctions are “back-to-back”



=> n-type regions **<u>isolated</u>** in p-type substrate and vice versa

Why are pn Junctions Important for ICs?

- The basic building block in digital ICs is the MOS transistor, whose structure contains reverse-biased diodes.
  - pn junctions are important for electrical isolation of transistors located next to each other at the surface of a Si wafer.
  - The junction capacitance of these diodes can limit the performance (operating speed) of digital circuits



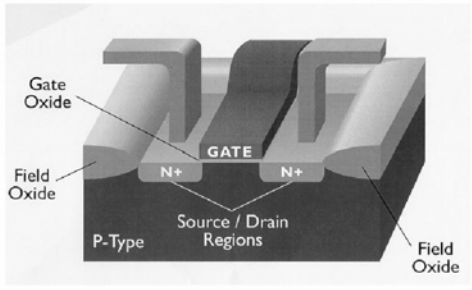
We can build large circuits consisting of many transistors without worrying about current flow between devices. The p-n junctions **isolate** the transistors because there is always at least one **reverse-biased** p-n junction in every potential current path.

Modern Field Effect Transistor (FET)

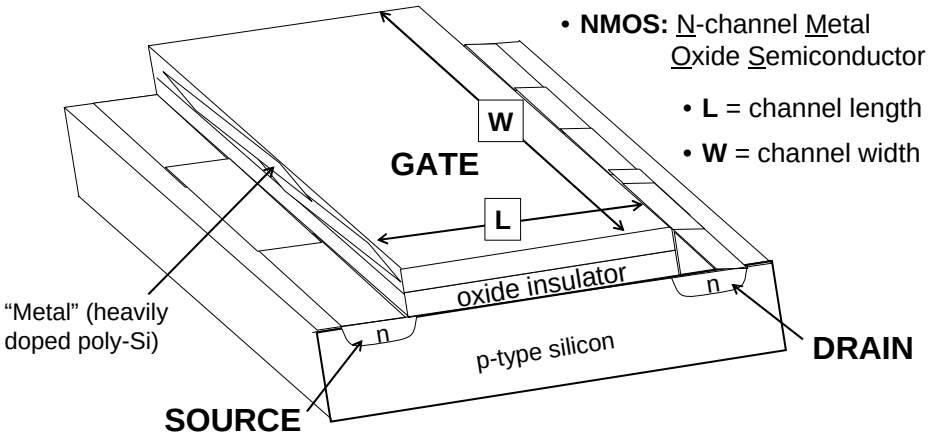
- An electric field is applied normal to the surface of the semiconductor (by applying a voltage to an overlying electrode), to modulate the conductance of the semiconductor

→ Modulate drift current flowing between 2 contacts ("source" and "drain") by varying the voltage on the "gate" electrode

→ Metal-oxide-semiconductor (MOS) FET



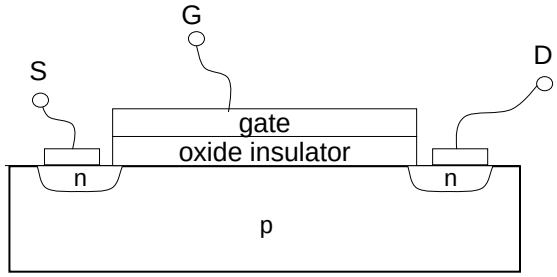
MOSFET



- **NMOS:** N-channel Metal Oxide Semiconductor
  - **L** = channel length
  - **W** = channel width

- A GATE electrode is placed above (electrically insulated from) the silicon surface, and is used to control the resistance between the SOURCE and DRAIN regions

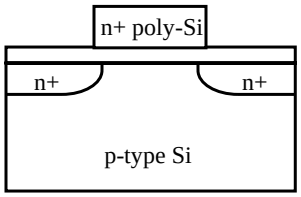
N-channel MOSFET



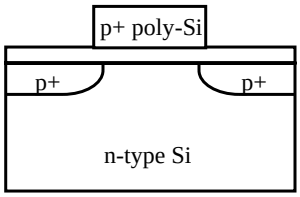
- Without a gate voltage applied, no current can flow between the source and drain regions.
- Above a certain gate-to-source voltage (***threshold voltage V_T***), a conducting layer of mobile electrons is formed at the Si surface beneath the oxide. These electrons can carry current between the source and drain.

N-channel *vs.* P-channel MOSFETs

NMOS



PMOS



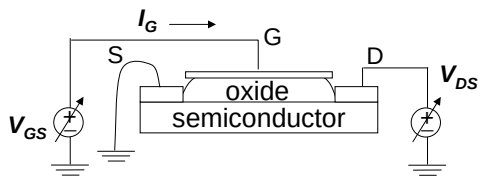
- For current to flow, $V_{GS} > V_T$
- Enhancement mode: $V_T > 0$
- Depletion mode: $V_T < 0$
  - Transistor is ON when V_G=0V

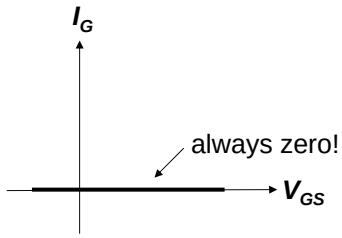
- For current to flow, $V_{GS} < V_T$
- Enhancement mode: $V_T < 0$
- Depletion mode: $V_T > 0$
  - Transistor is ON when V_G=0V

("n+" denotes very heavily doped n-type material; "p+" denotes very heavily doped n-type material)

NMOSFET I_G vs. V_{GS} Characteristic

Consider the current I_G (flowing into **G**) versus V_{GS}:

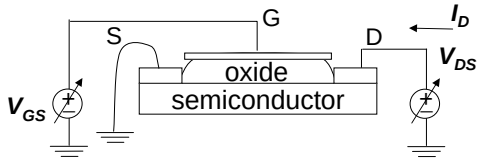


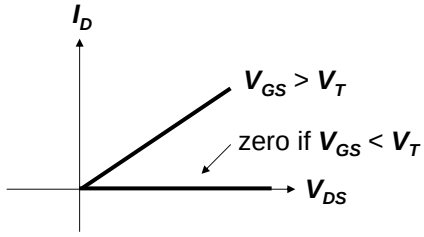


The gate is insulated from the semiconductor, so there is no significant gate current.

NMOSFET I_D vs. V_{DS} Characteristics

Next consider I_D (flowing into **D**) versus V_{DS}, as V_{GS} is varied:





Above threshold ($V_{GS} > V_T$): "inversion layer" of electrons appears, so conduction between **S** and **D** is possible

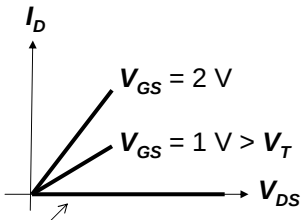
Below "threshold" ($V_{GS} < V_T$): no charge → no conduction

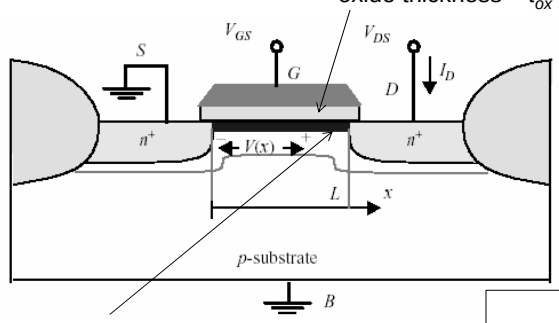
The MOSFET as a Controlled Resistor

- The MOSFET behaves as a resistor when V_{DS} is low:
  - Drain current I_D increases linearly with V_{DS}
  - Resistance R_{DS} between SOURCE & DRAIN depends on V_{GS}
    - R_{DS} is lowered as V_{GS} increases above V_T

oxide thickness ≡ t_{ox}

NMOSFET Example:



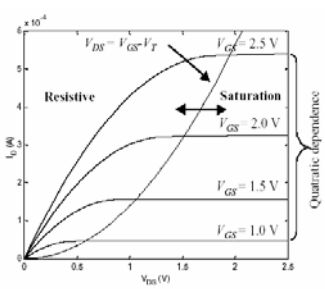


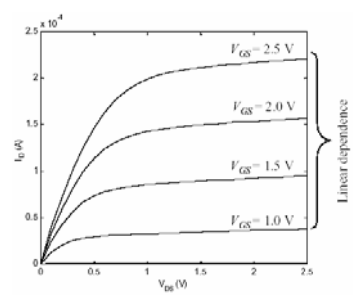
I_{DS} = 0 if $V_{GS} < V_T$

Inversion charge density $Q_i(x) = -C_{ox}[V_{GS}-V_T-V(x)]$
where $C_{ox} \equiv \varepsilon_{ox} / t_{ox}$

MOSFET Current Saturation

1. I_D is reduced by the voltage drop along the channel
2. I_D is reduced when carriers reach the velocity limit





$$I_D = k'_n \frac{W}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

where $k'_n = \mu_n C_{ox}$

$$I_{DSAT} = \frac{k'_n}{2}\frac{W}{L}(V_{GS}-V_T)^2$$

where $k'_n = \mu_n C_{ox}$

$$I_{DSAT} = WC_{ox}\left[V_{GS} - V_T - \frac{V_{DSAT}}{2}\right]v_{sat}$$

where $V_{DSAT} = \frac{L}{\mu_n} v_{sat}$