Diodes: Piecewise Models and Circuit Analysis

Lecture 24, 10/26/05
TTL Re-Updated 10/28/05

OUTLINE

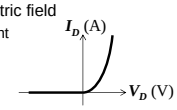
- Load Line Analysis
- Solar Cells, Detectors, Zener Diodes
- Piecewise Linear Models (Ideal and Large Signal)
- Circuit Analysis with Piecewise Linear
- Logic Circuits and IC Device Isolation

Reading

Hambley 10.2- 10.5

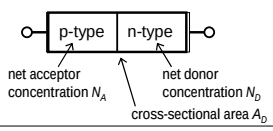
Summary: *pn*-Junction Diode *I-V*

- Under forward bias, the potential barrier is reduced, so that carriers flow (by diffusion) across the junction
  - Current increases exponentially with increasing forward bias
  - The carriers become minority carriers once they cross the junction; as they diffuse in the quasi-neutral regions, they recombine with majority carriers (supplied by the metal contacts)
    "injection" of minority carriers
- Under reverse bias, the potential barrier is increased, so that negligible carriers flow across the junction
  - If a minority carrier enters the depletion region (by thermal generation or diffusion from the quasi-neutral regions), it will be swept across the junction by the built-in electric field
    "collection" of minority carriers → reverse current

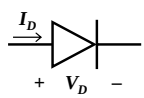


The *pn* Junction Diode

Schematic diagram

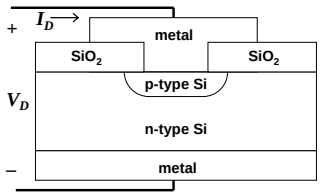


Circuit symbol



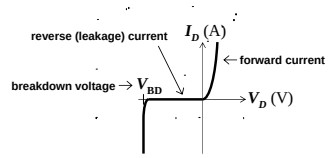
Physical structure: (an example)

For simplicity, assume that the doping profile changes abruptly at the junction.



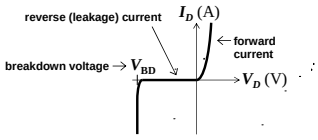
pn-Junction Reverse Breakdown

- As the reverse bias voltage increases, the peak electric field in the depletion region increases. When the electric field exceeds a critical value ($E_{crit} \cong 2\text{x}10^5$ V/cm), the reverse current shows a dramatic increase:

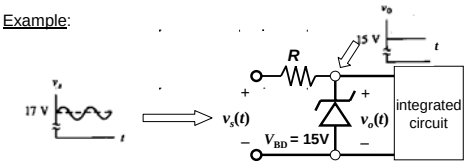


Zener Diode

A ***Zener diode*** is designed to operate in the breakdown mode.

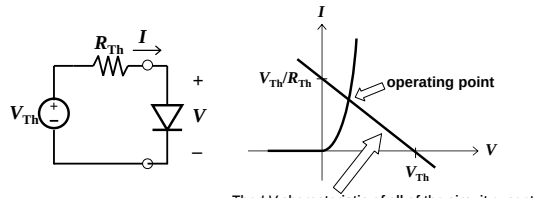


Example:



Load Line Analysis Method

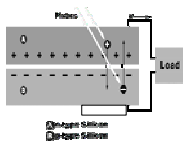
1. Graph the *I-V* relationships for the non-linear element and for the rest of the circuit
2. The operating point of the circuit is found from the intersection of these two curves.



The *I-V* characteristic of all of the circuit except the non-linear element is called the *load line*

Solar cell: Example of simple PN junction

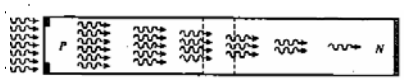
- What is a solar cell?
  - Device that converts sunlight into electricity
- How does it work?
  - In simple configuration, it is a diode made of PN junction
  - Incident light is absorbed by material
  - Creates electron-hole pairs that transport through the material through
    - Diffusion (concentration gradient)
    - Drift (due to electric field)



PN Junction Diode

Optoelectronic Diodes

- Light incident on a pn junction generates electron-hole pairs
- Carriers are generated in the depletion region as well as n-doped and p-doped quasi-neutral regions.
- The carriers that are generated in the quasi-neutral regions diffuse into the depletion region, together with the carriers generated in the depletion region, are swept across the junction by the electric field

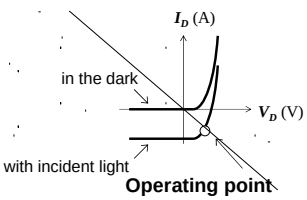


- This results in an additional component of current flowing in the diode: $I_D = I_S(e^{qV_D/kT} - 1) - I_{optical}$

  where $I_{optical}$ is proportional to the intensity of the light

Photovoltaic (Solar) Cell

$$I_D = I_S(e^{qV_D/kT} - 1) - I_{optical}$$



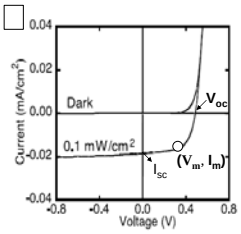
Operating point
The load line a simple resistor.

I-V characteristics of the device

- I-V characteristics of a PN junction is given by

$$I = I_S\left[\exp\left(\frac{eV}{kT}\right) - 1\right] - I_L$$

where I_S is the saturation intensity depending on band gap and doping of the material and I_L is the photocurrent generated due to light



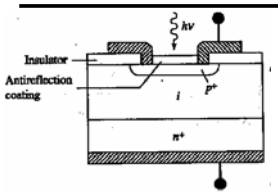
- Efficiency is defined as

$$\eta = \frac{I_m \cdot V_m}{Light\ Intensity} = \frac{FF * V_{oc} * I_{sc}}{Light\ Intensity}$$

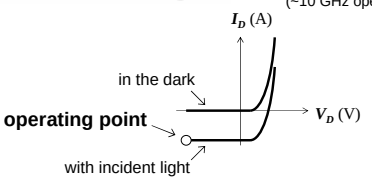
FF is the Fill Factor

V_{oc} - Open circuit voltage
I_{sc} - Short circuit current
I_{mp}, V_{mp} - Current and voltage at maximum power

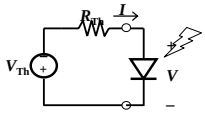
Example 2: Photodiode

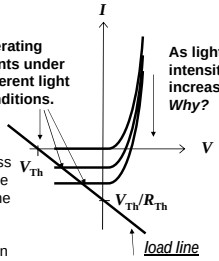


- An intrinsic region is placed between the p-type and n-type regions
  - $W_i \cong W_{i\text{-region}}$, so that most of the electron-hole pairs are generated in the depletion region
    - → faster response time (~10 GHz operation)



Photodetector Circuit Using Load Line





operating points under different light conditions.

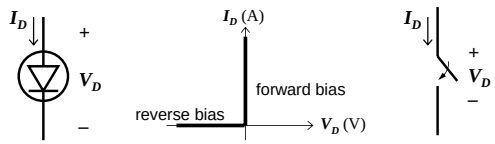
As light intensity increases. *Why?*

As light shines on the photodiode, carriers are generated by absorption. These excess carriers are swept by the electric field at the junction creating drift current, which is same direction as the reverse bias current and hence negative current. The current is proportional to light intensity and hence can provide a direct measurement of light intensity → photodetector.

- What happens when R_{th} is too large?
- Why use Vth?

Ideal Diode Model of PN Diode

Circuit symbol | ***I-V* characteristic** | **Switch model**

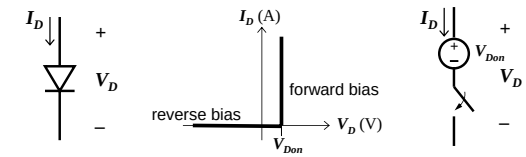


- An ideal diode passes current only in one direction.
- An ***ideal diode*** has the following properties:
  - when $I_D > 0$, $V_D = 0$
  - when $V_D < 0$, $I_D = 0$

  } Diode behaves like a switch:
  - closed in forward bias mode
  - open in reverse bias mode

Large-Signal Diode Model

Circuit symbol | ***I-V* characteristic** | **Switch model**



For a Si pn diode, $V_{Don} \cong 0.7$ V

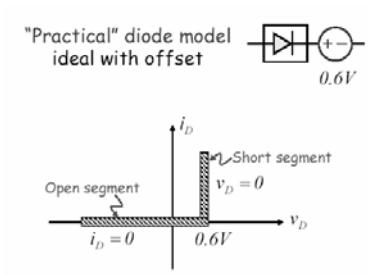
RULE 1: When $I_D > 0$, $V_D = V_{Don}$

RULE 2: When $V_D < V_{Don}$, $I_D = 0$

} Diode behaves like a voltage source in series with a switch:
- closed in forward bias mode
- open in reverse bias mode

Diode: Large Signal Model

- Use piece-wise linear model



How to Analyze Circuits with Diodes

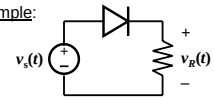
A diode has only two states:

- **forward biased:** $I_D > 0$, $V_D = 0$ V (or 0.7 V)
- **reverse biased:** $I_D = 0$, $V_D < 0$ V (or 0.7 V)

Procedure:

1. Guess the state(s) of the diode(s)
2. Check to see if KCL and KVL are obeyed.
3. If KCL and KVL are not obeyed, refine your guess
4. Repeat steps 1-3 until KCL and KVL are obeyed.

Example:



If $v_s(t) > 0$ V, diode is forward biased (else KVL is disobeyed – try it)

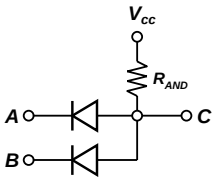
If $v_s(t) < 0$ V, diode is reverse biased (else KVL is disobeyed – try it)

Diode Logic: AND Gate

- Diodes can be used to perform logic functions:

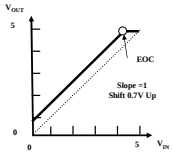
AND gate

output voltage is high only if both A and B are high



Inputs A and B vary between 0 Volts ("low") and V_{cc} ("high")

Between what voltage levels does C vary?



Diode Logic: OR Gate

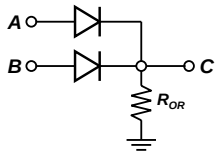
- Diodes can be used to perform logic functions:

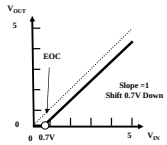
OR gate

output voltage is high if either (or both) A and B are high

Inputs A and B vary between 0 Volts ("low") and V_{cc} ("high")

Between what voltage levels does C vary?



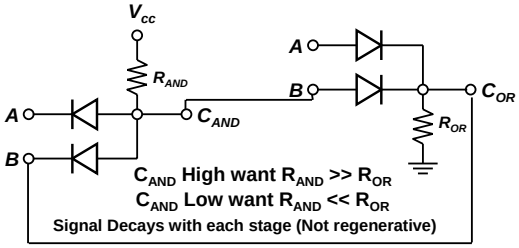


Diode Logic: Incompatibility and Decay

- Diode Only Gates are Basically Incompatible:

AND gate
output voltage is high only if both A and B are high

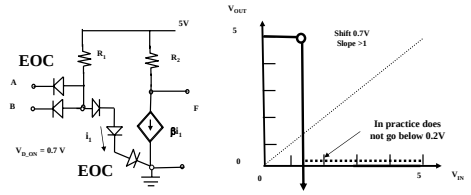
OR gate
output voltage is high if either (or both) A and B are high



C_{AND} High want R_{AND} >> R_{OR}
C_{AND} Low want R_{AND} << R_{OR}
Signal Decays with each stage (Not regenerative)

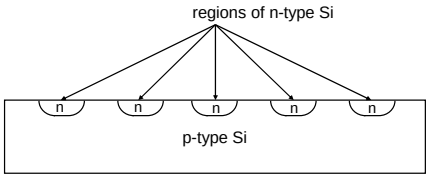
Digital Logic: Diodes with Dependent Sources

- EE40 TTL (Transistor-Transistor Logic

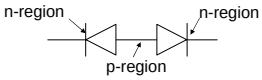


Incase you are interested: True TTL has at least three dependent sources that are associated with the three bipolar transistors on which it is based.

Device Isolation using pn Junctions



No current flows if voltages are applied between n-type regions, because two pn junctions are "back-to-back"



=> n-type regions **isolated** in p-type substrate and vice versa

Why are pn Junctions Important for ICs?

- The basic building block in digital ICs is the MOS transistor, whose structure contains reverse-biased diodes.
  - pn junctions are important for electrical isolation of transistors located next to each other at the surface of a Si wafer.
  - The junction capacitance of these diodes can limit the performance (operating speed) of digital circuits