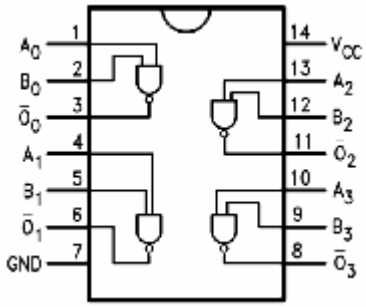
Experiment Guide: Digital Logic

Objective

In this introduction to CMOS digital logic, you will use commercially available "quad NAND gates" to breadboard the NOT gate and the XOR gate and measure their propagation delays on the oscilloscope.

Commercial NAND Gates

In this lab, you will construct logic circuits using a DIP-package NAND gate from a family of standard logic ICs. In particular, you will be using the 74HC00, a Quad NAND array (or the Quad NAND IC). You will need more than one IC to construct the XOR function.



NOTE : This is a **TOP VIEW**. A half-circle or small circle indicates where pin 1 is.

Figure 1. The 74HC00

There are 4 NAND gates in one package (see connection diagram above), hence it is named "Quad NAND". Two special symbols require attention. One is the Vcc (pin 14), which provides power to the chip and serves as the high logic level. Vcc can be from +2 to +6V. The other is GND (pin 7), which serves as power return ground as well as the low logic level. Please see the full data sheets for more details.

Normal Operation and Absolute Maximum Ratings

Please observe from the data sheets especially the Absolute Maximum Ratings.
In particular:

1) **V_{CC} CANNOT BE MADE NEGATIVE of ground**
2) **inputs A and B CANNOT BE MADE NEGATIVE of ground**
3) **inputs are NOT ALLOWED TO EXCEED V_{CC}**

The latter caution is somewhat subtle and particularly easy to violate (burning out the chip). For example if you are studying normal operation at 5V you may be tempted to use logic levels of 0 and 5 V at the inputs. Now if you turn down V_{CC} and you continue to drive the inputs with a 5V logic signals, you will violate rule 3!!!! THEREFORE BE CAREFUL TO NEVER DRIVE THE INPUTS WITH VOLTAGES EXCEEDING V_{CC}.

Another feature to note from the data sheets is the dependence of the gate delay performance on V_{CC}. "Nominal worst case" operation is at V_{CC} = 4.5V (because that is the lower end of the nominal power supply range of 5V +/- 10%). But these devices are

also designed to work at much lower values of V_{CC}, down to 2V. This provides a great opportunity to observe gate delays in a regime where they are very easy to measure.

Chain of inverters

Before studying an XOR gate constructed from NAND gates, we want you to first study a much simpler circuit: a chain of 4 inverters (NOT gates). We suggest making the inverters by wiring one of the NAND inputs to logic 1. This gives the input signal a load of only one gate input. On your lab report draw the breadboard diagram of the chain of 4 inverters constructed using one 74HC00. Include the top view of the 74HC00 plugged into your prototype board and the wiring used to complete the circuit. Whenever using IC's, all input pins should be defined, not floating. Here, we will be using every pin on the package. In this diagram you can show the internal wiring of the breadboard explicitly. Next, construct the inverter chain, using a wire to apply either VDD=5V=logic 1 or VSS=0V=logic 0 to the chain input. Using the multimeter, verify the logic states within the chain. Then setup the function generator to provide a 1kHz square wave to the input and verify the switching of all the inverters in the chain using the oscilloscope.

Propagation Delay of Inverter Chain

Measure the delay of 3 inverters and 1 inverter using the oscilloscope. (To do this you use the square wave generator to drive the input and to trigger the scope. Set the scope Main Delay time reference to left. You can use the cursors to measure the gate delay. For example to measure the gate delay through gate 3 you measure the time between when the input reaches 50% ($0.5*V_{CC}$) and the time the output reaches 50%.) Repeat for V_{CC} = 5V, 2V. Assuming that the probe disturbs the delay (by adding capacitance), you can estimate this disturbance from the measurements above. In particular, the difference between 1 gate and 3 gates represents two times the average gate delay.

$$\tau_{propagationdelay} = \frac{\tau_{low-to-high} + \tau_{high-to-low}}{2}$$

The XOR Function

In the prelab you showed the NAND realization of the XOR function. Although this may not be an "optimal" design it will work and it will have at most 3 gate delays (one inverter and two NAND delays). **A recommended layout on the breadboard for the XOR circuit can be found on the EECS 40 website**. You will need to use 5 NAND gates plus one more to act as the load on the output; short the inputs on the two unused NAND gates to ground and leave the outputs open. Construct the XOR circuit, and verify its static operation. Fill out the truth table on your lab report. Show the circuit to your TA and demonstrate proper static logic functionality**.**

Propagation Delay of the XOR

Now it's time to measure the dynamic performance of the XOR circuit. You have loaded the output with a spare NAND gate input so that in the following you are measuring the delay of an XOR gate with fanout of 1. Measure the XOR delay at 5V.

AGAIN: THE INPUT LOGIC VOLTAGE CANNOT EXCEED V_{CC} !!!

Use the same technique as in the inverter chain. The square wave generator is the pulse source and the scope as instrument to measure the 50% point that defines the logic delay.

Glitching (BONUS – Only do this if you have time!)

Construct the circuit shown below, using V_{CC} = 5V, and load the output with a spare NAND gate input (short all other unused NAND inputs to ground, leaving the outputs open). Verify its static operation and fill out the truth table on your lab report. Apply the inputs for A and B shown on the timing diagram on your lab report and draw the waveforms for X and Y. Measure the time interval and height of the glitch.

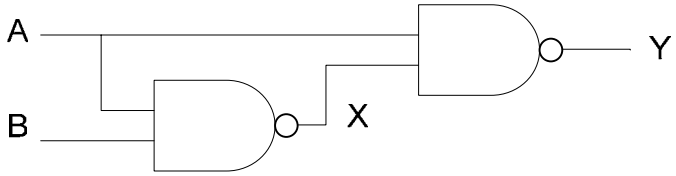


Figure 2. Glitching Circuit

More fun: Using LEDs to see digital logic states

To detect the logic level of a given circuit node one can of course use a voltmeter or scope. But for static measurements it is attractive to have a simple visual indicator. You can build such a logic probe using an LED in series with a resistor. Note that the LED is a diode with a polarity and is meant to conduct electrons and emit light in one direction. The amount of current you need (typically from 1 to 10 mA) to be able to clearly see the LED light depends on the LED efficiency. The high current end is limited by the source capability of the NAND gate output, which is about 10mA at 5V. Assuming a diode drop of about 1.6V to 1.8V, a resistor in the range of 300 ohms may be adequate for the full voltage range, but you must test your detector for correct operation and adequate LED brightness over the range 2V to 5V. WARNING: YOU CAN DAMAGE both the LED and the logic chip if you have too low a resistance. In no case use less than 200 ohms.