HW 7 Solutions - Isaac

7.1 Op-AM Types

Use figure 14.33 in the text on page 665 (it has 4 resistors).

a) Convert R2 to a capacitor with capacitance C and derive the expression for V_{out} as a function of V_{in1} and V_{in2} for sinusoidal inputs.

Given two sinusoidal inputs, we know that our circuit satisfies negative feedback. So, we can use the summing point constraint. From the circuit, the positive input results from voltage division of Vin1 across R4 and R3. This regulates the negative input voltage.

Thus, the current into the device is given by the following, given two inputs $V_{in1} = M_1(\cos\omega t + \phi_1)$ and $V_{in2} = M_2(\cos\omega t + \phi_2)$:

$I_{in} = (V_{in1} - R_4/(R_3 + R_4)V_{in2})/R_1$

By stepping through voltages,

$M_{out}\angle\phi_{out} = R_4/(R_3 + R_4) M_2\angle\phi_2$ - $(M_1\angle\phi_1 - R_4/(R_3 + R_4) M_2\angle\phi_2)/(j\omega R_1C)$

This can be simplified to give the following:

$R_4/(R_3 + R_4) M_2\angle\phi_2 + j(M_1\angle\phi_1 - R_4/(R_3 + R_4) M_2\angle\phi_2)/(\omega R_1C)$

$R_4/(R_3 + R_4) M_2\angle\phi_2 + (M_1\angle\phi_1+\pi/2 - R_4/(R_3 + R_4) M_2\angle\phi_2+\pi/2)/(\omega R_1C)$

This gives you an expression in the time domain of a sine and two cosines.

d) Go back to your circuit from part a) (Remove R5). Ground V_{in1}. Perform an analysis for a DC input V_{in2}. Find V_{out} in terms of V_{in2} and time, assume the capacitor initially is fully discharged at t = 0. What does this circuit do?

By the inverter analysis using the summing point constraint, $I = V_{in2}/R$

This current runs across the capacitor, charging it. By $I = C(dv/dt)$, we obtain that, given the capacitor is discharged at t = 0, V(t) is the integral from 0 to t of (V_{in2}/R). The circuit is thus termed an integrator (it looks similar to the integrator in lecture).

7.2 Cascade Op-Amp Analysis and Output Currents

Use figure 14.9 in the text on page 641. Use symbolic values for all resistors.

a) Discuss how and why the given circuit can be separated into two independent stages for analysis.

The circuit can be separated into two at the output of the first amplifier. The ideal characteristics of the amplifiers serve to buffer the output voltage at the output of the first amplifier no matter what load is connected.

b) Find the currents at the input to each amplifier stage, and through the load (at the input means current through the node at the input terminal, not current into the input terminal).

Using the summing point constraints, the current at the input to the first stage is:

$I_1 = V_1/R_1$

Using summing point constraints again and that $V_{out1} = -(R_2/R_1)V_1$, the current at the input to the second stage is: $I_2 = V_2/R_4 - (R_2/(R_1*R_3))V_1$

Using Ohm's Law, the current through the load is V_{out2}/R_L, where we obtain:

$V_{out2} = R_5(V_2/R_4 - (R_2/(R_1*R_3)) V_1)$

c) Find the current provided by the op-amp output for each stage.

By KCL, we obtain that the current out of the first stage is:

$(R_2/R_3 – 1)(V_1/R_1)$

By KCL, we obtain that the current out of the second stage is:

$(R_5/R_L - 1)(V_2/R_4 – (R_2/(R_1*R_3))V_1)$

d) Find an expression for V_{out} in terms of the two inputs. What does this circuit do?

From before, $V_{out2} = (R_5/R_4)V_2 – (R_2/(R_1*R_3))V_1$

The circuit is a summing circuit that inverts one input, and scales both inputs.

7.3 Building Op-Amps from Amplifiers

Assume that the contents of an op-amp are a two-port amplifier with infinite input impedance, a gain of 100,000 and a 10Ω Thevenin output impedance. Use figure 14.2 in the text on page 634, with a 10Ω resistor R_{out} in series with the dependent source on the + side. Assume input resistance is infinite.

a) Using the ideal op-amp framework, design an inverting amplifier. It should have a gain of –10, with the + terminal grounded. Give values for your components. Connect your components at the corresponding nodes in the non-ideal framework. When you work with the non-ideal model, how does your gain change? Find $V_–$ and V_{out} when V_{in} = 0.4V. For an inverting amplifier, V_+ should be grounded.

In order to design an inverting amplifier with a gain of –10, by the methods in lecture we need two resistors whose ratio is 10, the smaller one for the input path and the larger one for the feedback path. Any set is fine as long as this ratio holds.

Suppose two resistors rated at 1kΩ and 10kΩ. Connecting them to the nonideal circuit with R_{in} infinite, A = 100,000 and Rout = 10Ω, this circuit must be solved using any of the methods of circuit analysis learned in the first half of the course.

Using KVL analysis the following circuit results, and the following equations are obtained.

$-Vin + (I*1k\Omega) + (I*10k\Omega) + (I*10\Omega) + 100000(V+ - V-) = 0$

$-(V+ - V-) = Vin – I*1k\Omega$

This results in: $-Vin + I*(11010) + 100000(I*1k\Omega) – 100000Vin = 0$

Also, $Vout = Vin – I(1k\Omega + 10k\Omega)$

From the former equation, $I = Vin(9.999*10^{-4})$

Substituting into the Vout expression, the result Vout = -9.999Vin is obtained.

The nonideality, because it is so close to the ideal form, does not significantly degrade the gain of the amplifier.

Note that anyone could use different values for the two resistors. As long as the result obtained is close to Vout = -10Vin, that result is acceptable.

Then, when Vin = 0.4V, by the above analysis Vout ≈ -4V, V- ≈ 0V

b) Assume that A is frequency dependent 1/(1+f/100MHz)). Find the frequency at which the overall response drops by about 3 dB.

The first step in this problem is to calculate the result when f = 0. When this is true, A = 1.

Working back through our equations, we can obtain that

Vout = Vin – Vin(11kΩ*(1 + 1)/(10kΩ + 1kΩ + 10 + A*1kΩ)

Vout = -0.832Vin

Notice that when A is relatively low, far from the ideal, the output is far from the ideal op-amp calculations.

If we want a 3dB reduction in Vout/Vin, this calls for a multiplicative factor of $2^{-1/2}$.

This gives the relation Vout = -0.588Vin

Solving back through the equation,

-0.588 = 1 – 11kΩ(1+A)/(10kΩ + 1kΩ + 10 + A*1kΩ)

This gives A = 0.689Hz after solving.