UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS 40 — Fall 2003
Introduction to Microelectronic Circuits — Prof. King

FINAL EXAMINATION

December 10, 2003
Time allotted: 2 hours 50 minutes (170 minutes)

NAME: Solutions ______, ______
(print) **Last** **First**

Signature: ______ **STUDENT ID#:** ______

1. This is a **CLOSED BOOK** exam. However, you may use 3 sheets of notes and a calculator.
2. **SHOW YOUR WORK or REASONING** on this exam.
   (Make your methods clear to the grader.)
3. **Write your answers clearly (legibly) in the spaces (lines, boxes, or plots) provided.**
4. Remember to specify the units on answers whenever appropriate.

SCORE: 1 ______ **/ 20**

2 ______ **/ 20**

3 ______ **/ 20**

4 ______ **/ 20**

5 ______ **/ 20**

6 ______ **/ 20**

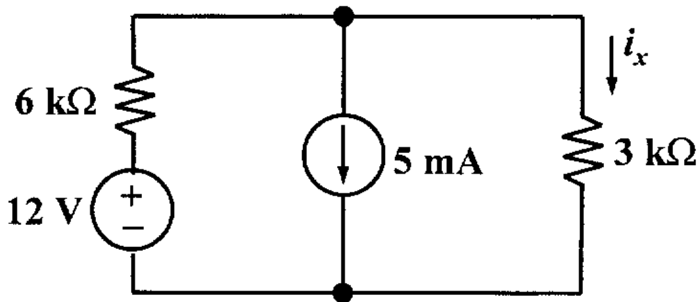
7 ______ **/ 20**

8 ______ **/ 10**

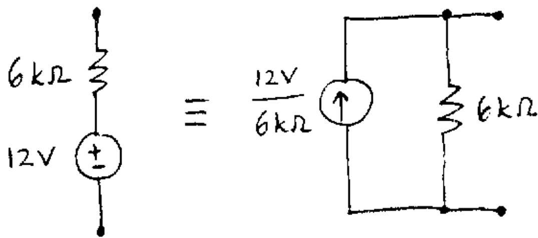
Total: ______ **/ 150**

Problem 1: Circuit Analysis and Equivalent Circuits [20 points in total]

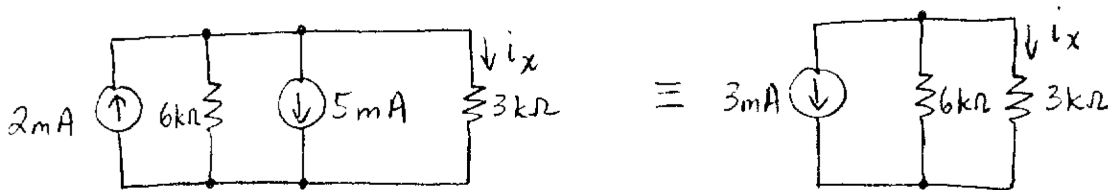
a) Consider the following circuit:



i) Use a source transformation in order to find i_x. **[6 pts]**



Therefore the circuit above is equivalent to

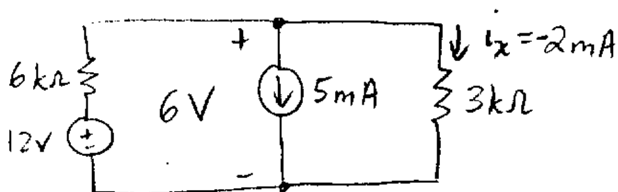


$$i_x = \frac{6k\Omega}{6k\Omega + 3k\Omega}(-3mA) = \frac{2}{3}(-3mA)$$

$i_x =$ −2 mA

ii) What is the power developed/absorbed by the 5 mA current source? **[3 pts]**

The voltage drop across the current source is $i_x \times 3k\Omega = -6$ V



$P = IV = (5mA)(-6V) = -30$ mW

$P < 0 \Rightarrow$ power is developed

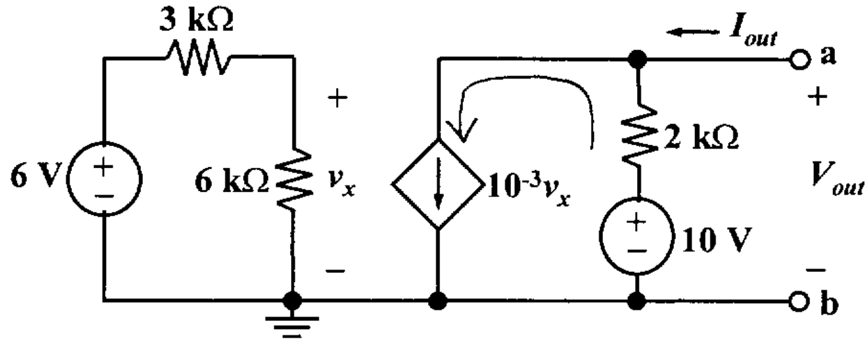
Power = 30 mW

[developed / absorbed] (developed circled)

(circle the correct choice)

Problem 1 (continued)

b) Consider the following circuit:

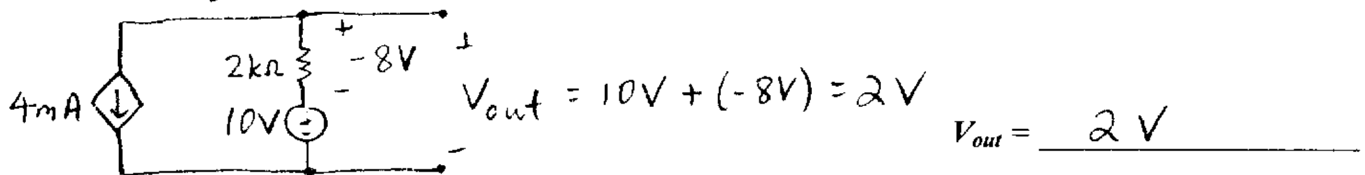


i) Find V_{out}. **[6 pts]**

$$v_x = \frac{6\,k\Omega}{3k\Omega + 6k\Omega}(6V) = \frac{2}{3}(6V) = 4V$$

dependent current source value $= 10^{-3} v_x = 4\times10^{-3}\,A = 4\,mA$

Voltage drop across $2k\Omega$ resistor is $(-4mA)(2k\Omega) = -8V$

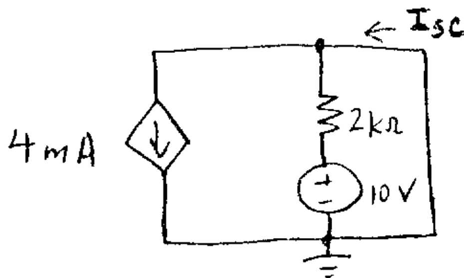


$V_{out} =$ 2 V

ii) Draw the Thevenin Equivalent circuit. **[5 pts]**

$$V_{out} = V_{oc} = V_{Th} = 2V$$

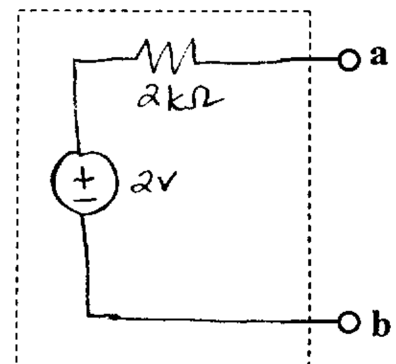
Determine the short-circuit current I_{sc}:



$$\text{KCL:}\quad I_{sc} = \frac{0-10}{2k\Omega} + 4mA = -5mA + 4mA = -1mA$$

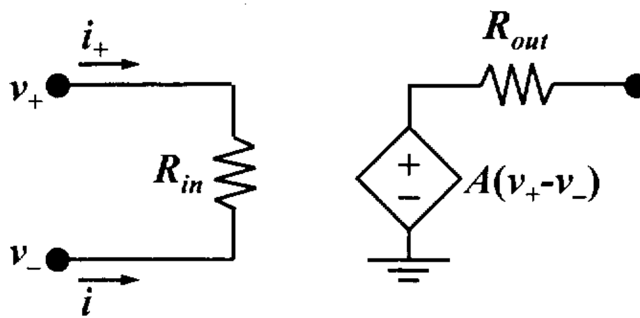
$$R_{Th} = \frac{V_{oc}}{-I_{sc}} = \frac{2V}{1mA} = 2\,k\Omega$$

Thevenin Equivalent Circuit:



Problem 2: Op Amp Circuit [20 points in total]

a) The following is the circuit model for an op amp circuit operating in its linear region:

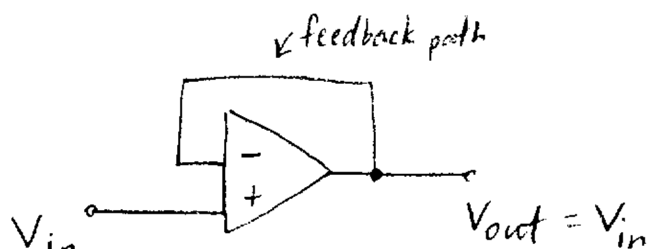


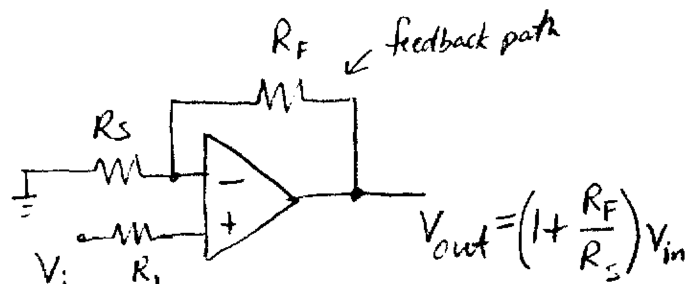
Typically, R_{in} is very large (~1 MΩ), A is very large (>10^4), and R_{out} is very small (<100 Ω).

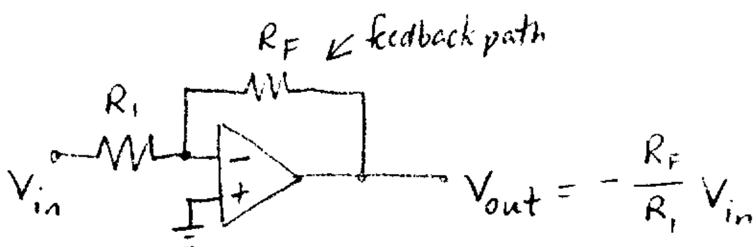
What type of feedback is used in an op amp circuit, in order to ensure that the op amp will operate in its linear region? Illustrate (with a simple diagram) how this is achieved. **[5 pts]**

Negative feedback is used to achieve linear operation.

Part (or all) of the op-amp output voltage is fed back to the (−) input terminal. Examples:

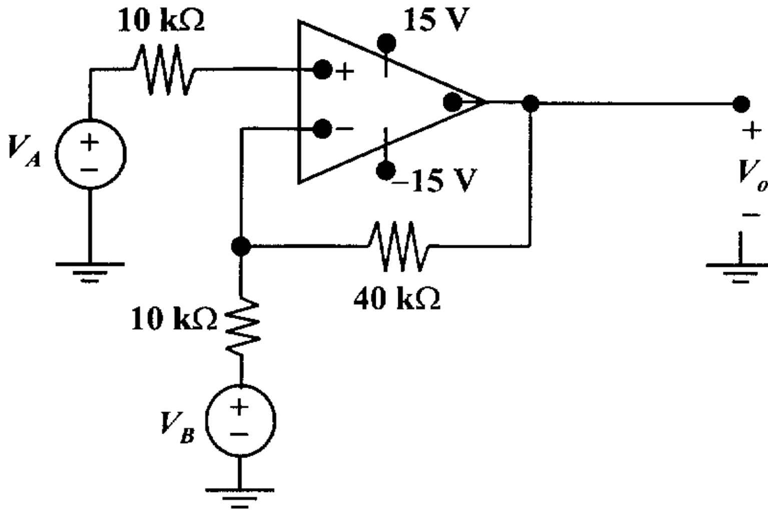






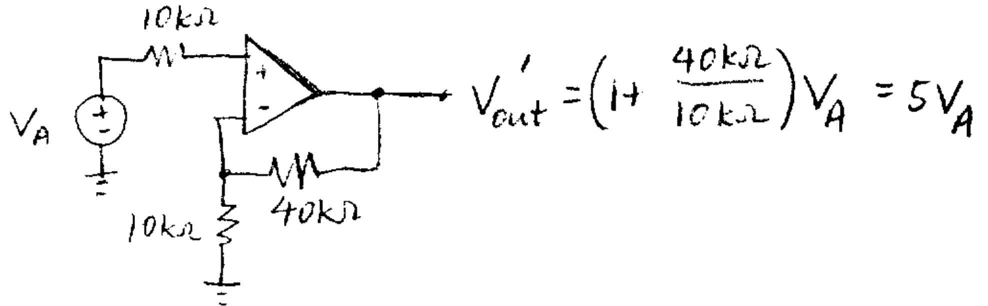
Problem 2 (continued)

b) Consider the following op amp circuit below. You can assume that the op amp is ideal.

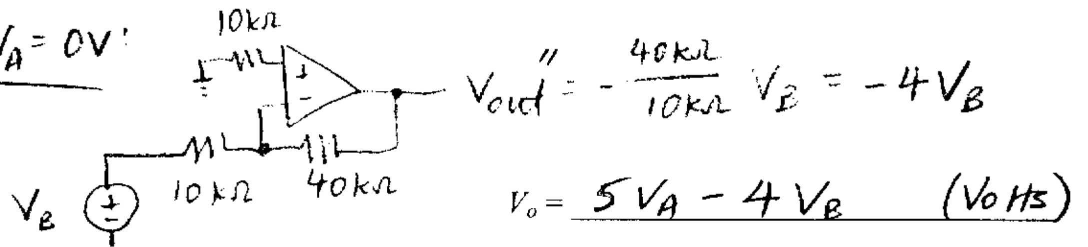


i) Find an expression for V_o, using superposition. **[10 pts]**

Setting $V_B = 0$ V:



Setting $V_A = 0$V:



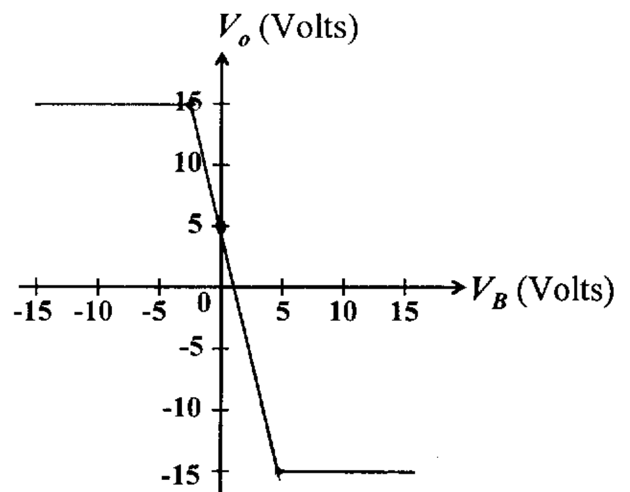
$V_o =$ $5V_A - 4V_B$ (Volts)

ii) Suppose V_A is fixed at 1 Volt. Plot V_o vs. V_B. **[5 pts]**

$V_o = 5(1) - 4(V_B) = 5 - 4V_B$

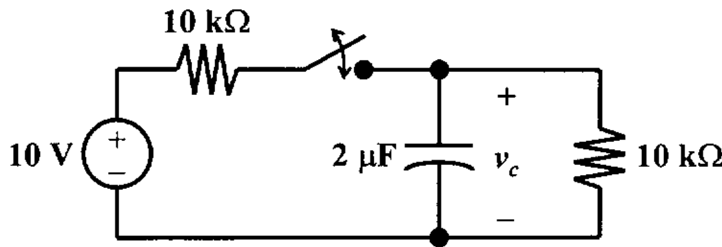
$-15V \leq V_o \leq 15V$

due to power supplies



Problem 3: First-Order Circuits [20 points in total]

In the circuit below, the switch is open for all $t < 0$. The switch is closed at $t = 0$, and then it is opened again at $t = 10$ ms.

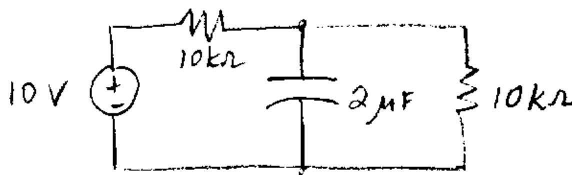


Initially, capacitor is discharged: $v_C(0^-) = 0\text{V}$

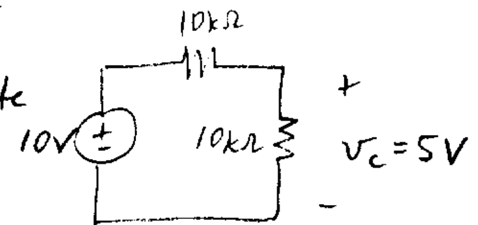
$\Rightarrow v_c(0^+) = 0\text{V}$

i) Write an equation for $v_c(t)$, for $0 \le t \le 10$ ms. **[8 pts]**

When the switch is closed, the circuit is



steady state $\longrightarrow$ (cap. is an open circuit)



The capacitor will charge up, toward the steady-state value $v_c = 5\text{V}$

The capacitor "sees" the parallel combination of the 10kΩ resistors

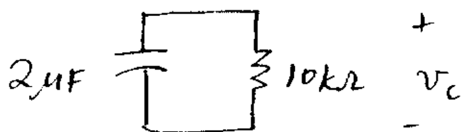
$RC = (5\text{k}\Omega)(2\mu\text{F}) = 10\text{ms}$

$0 \le t \le 10$ ms: $v_c(t) =$ $5\left(1 - e^{-t/10\text{ms}}\right)$ Volts

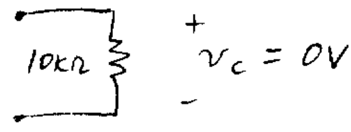
ii) Write an equation for $v_c(t)$, for $t > 10$ ms. **[8 pts]**

At $t = 10\text{ms}$, $v_c = 0.63\,(5\text{V}) = 3.15\text{ V}$

When the switch is open, the capacitor circuit is



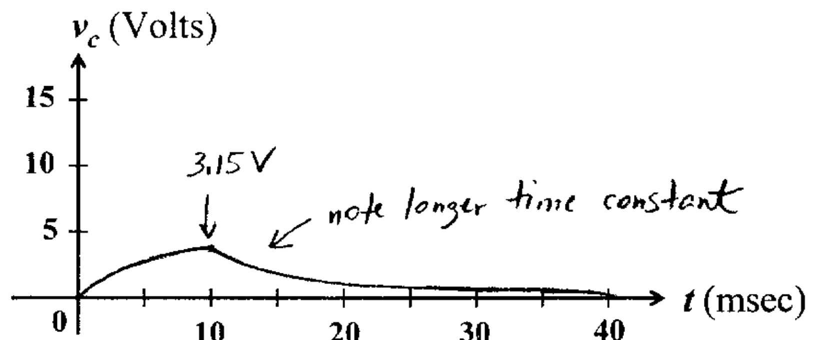
steady state $\longrightarrow$ (cap. is an open circuit)



$RC = (10\text{k}\Omega)(2\mu\text{F}) = 20\text{ms}$

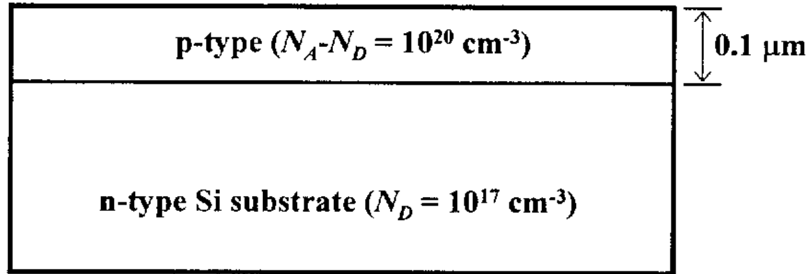
$t > 10$ ms: $v_c(t) =$ $3.15\, e^{-(t-10\text{ms})/20\text{ms}}$ Volts

iii) Sketch $v_c(t)$ for $t > 0$ **[4 pts]**



Problem 4: pn junctions; diodes [20 points in total]

a) Consider a pn junction formed in the surface of an n-type silicon wafer maintained at T = 300K. The p and n regions are uniformly doped, as indicated in the figure below:



Schematic cross-sectional view of pn junction

In the p-type region, the electron mobility is 100 cm²/V•s and the hole mobility = 50 cm²/V•s

i) Estimate the sheet resistance of the p-type region. **[6 pts]**
(Use the following values of constants: $q = 1.6\times10^{-19}$ C, $n_i = 10^{10}$ cm^{-3})

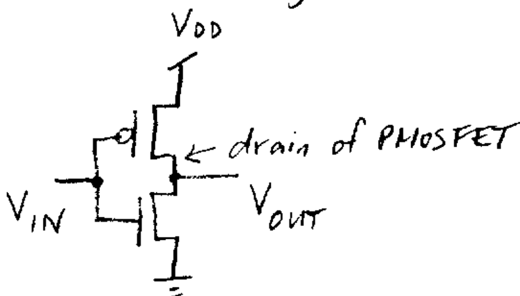
resistivity $\simeq \frac{1}{q\mu_p p} = \frac{1}{(1.6\times10^{-19})(50)(10^{20})} = 1.25$ mΩ-cm

sheet resistance $= \frac{\rho}{t} = \frac{1.25\times10^{-3}\ \Omega\text{-cm}}{0.1\times10^{-4}\ \text{cm}} = 125\ \Omega/\square$

Sheet resistance = $125\ \Omega/\square$

ii) Suppose the p-type region serves as the drain region of a p-channel MOSFET in a CMOS inverter, and that the n-type substrate is therefore biased at the power-supply voltage V_{DD}. How will the pn-junction capacitance change as the PMOSFET is turned on (so that the drain bias is changed from 0 V to V_{DD})? Explain briefly. **[4 pts]**

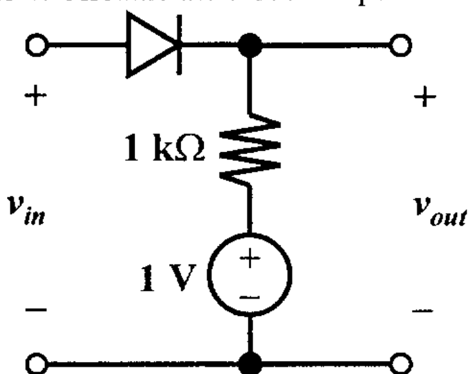
As the PMOSFET turns on, the output of the inverter charges from 0V to V_{DD}. The drain pn junction bias changes from $-V_{DD}$ to 0V.



Therefore the depletion-region width decreases (with decreasing reverse bias), and hence the drain capacitance increases.

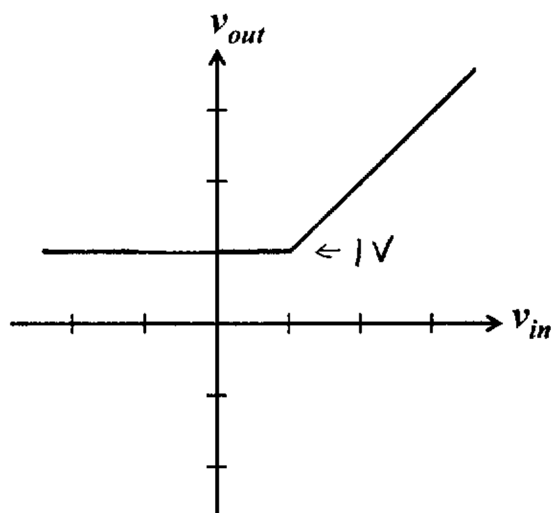
Problem 4 (continued)

b) Consider the diode circuit below. Assume the diode is a perfect rectifier.

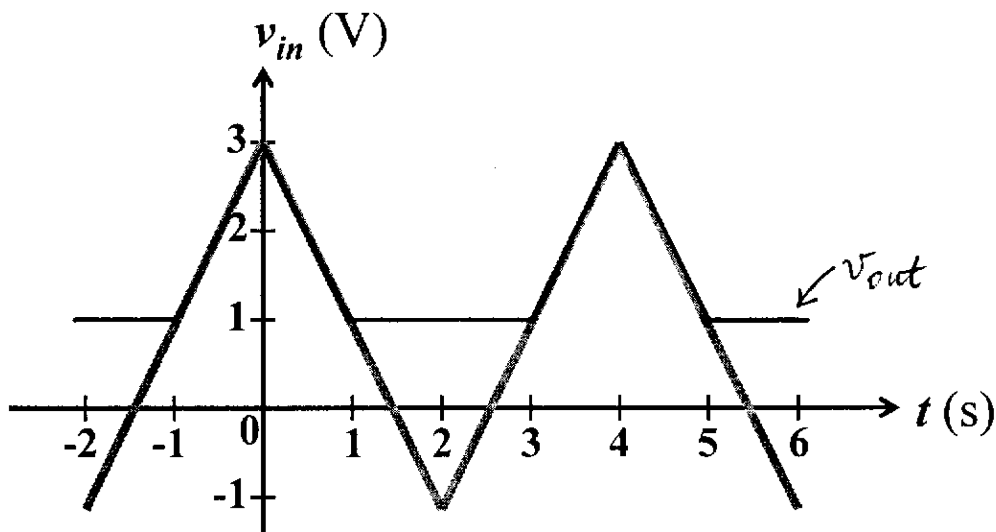


i) Plot v_{out} *vs.* v_{in}. **[5 pts]**

The diode will turn on when $V_{in} \geq 1$ V. When the diode is on, $V_{out} = V_{in}$. When the diode is off, $V_{out} = 1$V



ii) Sketch v_{out} for the given $v_{in}(t)$, using the same axes. **[5 pts]**



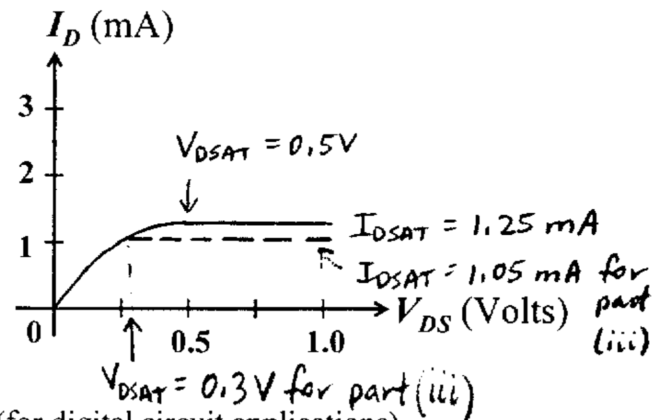
Problem 5: MOSFET [20 points in total]

a) Consider an NMOSFET with parameters $W = 1$ µm, $L = 0.1$ µm, $k_n' = 10^{-3}$ A/V^2, $V_T = 0.5$V, biased at $V_{GS} = V_{DD} = 1$ **V**. The areal gate capacitance $C_{ox} = 3\times10^{-6}$ F/cm^2.

i) Accurately sketch the I_D *vs.* V_{DS} characteristic in the range $0 \le V_{DS} \le 1$ V, neglecting velocity saturation and channel-length modulation. Indicate the numerical values for the saturation voltage (V_{DSAT}) and current (I_{DSAT}). **[6 pts]**

$$V_{DSAT} = V_{GS} - V_T = 1 - 0.5 = 0.5V$$

$$I_{DSAT} = \frac{W}{L}\frac{k_n'}{2}(V_{GS}-V_T)^2 = \left(\frac{1}{0.1}\right)\left(\frac{10^{-3}}{2}\right)(1-0.5)^2 = 1.25 \text{ mA}$$



ii) Estimate the effective resistance of this MOSFET (for digital circuit applications). (Again, assume that velocity saturation and channel-length modulation can be neglected. **[3 pts]**

$$R_{eq} = \frac{3}{4}\frac{V_{DD}}{I_{DSAT}} = \frac{3}{4}\frac{(1V)}{1.25 mA} = 600\,\Omega$$

$$k_n' = \mu_n C_{ox} \Rightarrow \mu_n = \frac{k_n'}{C_{ox}} = \frac{10^{-3}}{3\times10^{-6}}$$

iii) On the same plot in part (i) above, accurately sketch and label the I_D *vs.* V_{DS} characteristic, taking into account that the electron velocity in the MOSFET channel saturates at 10^7 cm/s. **[5 pts]**

$$v_{sat} = 10^7 \text{ cm/s}$$

$$V_{DSAT} = \frac{L}{\mu_n} v_{sat} = \frac{0.1\times10^{-4}}{(10^{-3}/3\times10^{-6})} 10^7 = 0.3V$$

$$I_{DSAT} = W C_{ox}\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right) v_{sat}$$

$$= (10^{-4})(3\times10^{-6})\left(1 - 0.5 - \frac{0.3}{2}\right)(10^7)$$

$$= 1.05 \text{ mA}$$

Problem 5 (continued)

b) High drive current (I_{DSAT}) is desirable for reduced equivalent resistance, to achieve smaller propagation delay to allow higher-speed circuit operation. Indicate in the table below how you would adjust various MOSFET parameters so as to increase I_{DSAT}. Briefly describe the tradeoff or disadvantage involved, if any, for each. (For example, the answer for gate length L is given.) **[6 pts]**

MOSFET Parameter	**To increase I_{DSAT}, parameter must be**	**Associated tradeoff or disadvantage**
Gate length L	**decreased**	Subthreshold leakage current increases, so that static power dissipation increases
Threshold voltage V_T	decreased	Subthreshold leakage current increases, so static power consumption increases.
Channel width W	increased	Intrinsic capacitance at the output of the logic gate increases; therefore dynamic power consumption increases.

Problem 6: Logic Circuits [20 points in total]

a) Given the following truth table for the logic function **F**:

A	B	F
0	0	1
0	1	0
1	0	1
1	1	1

(rows 1 and 3: $\bar{B}$; row 4: AB)

i) Write a simple logic expression for **F**. **[2 pts]**

$F = \bar{B} + AB$

Alternative logic expressions: $F = A + \bar{A}\bar{B}$

$F = A + \bar{B}$

$\overline{\bar{A} \cdot B}$

F = $\bar{B} + AB$

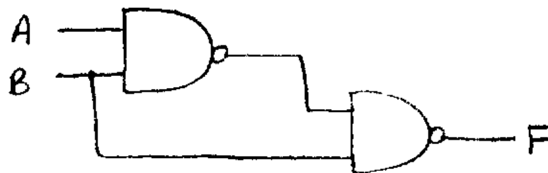
ii) Implement the function **F**, using only 2-input NAND gates. **[5 pts]**

From De Morgan's Law: $\bar{B} + AB = \bar{B} + \bar{\bar{AB}} = \overline{B \cdot \overline{AB}}$

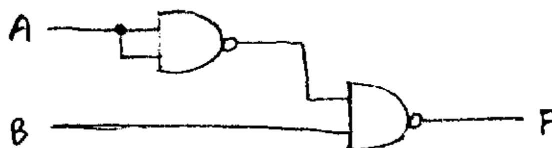
$\bar{X} + \bar{Y} = \overline{XY}$

$A + \bar{B} = \overline{\bar{A} \cdot B}$

Logic circuit for F:

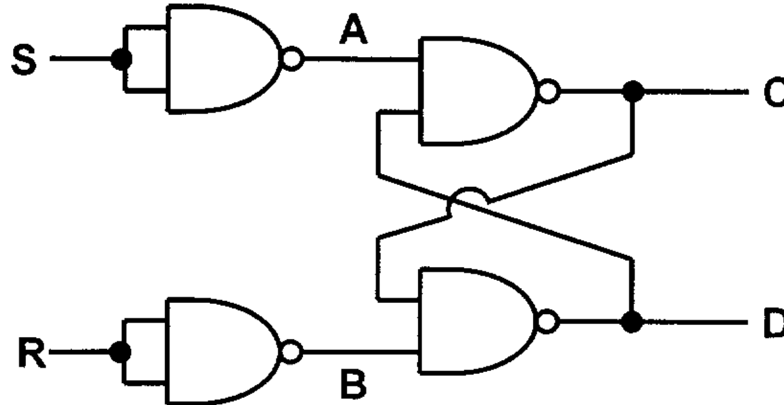


or



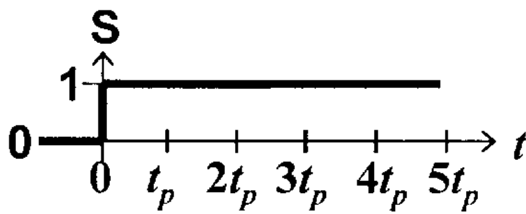
Problem 6 (continued)

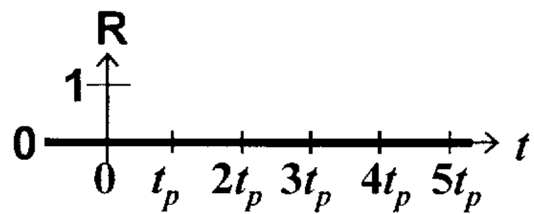
b) Consider the S-R flip-flop circuit below:

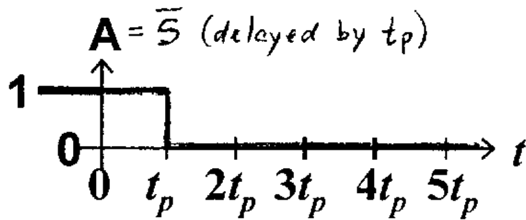


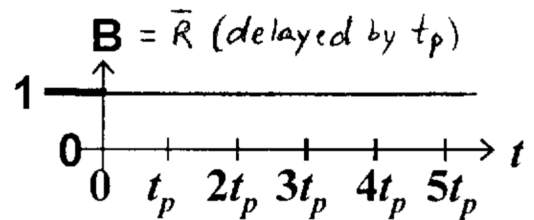
The output C is initially equal to 0, and the output D is initially equal to 1.

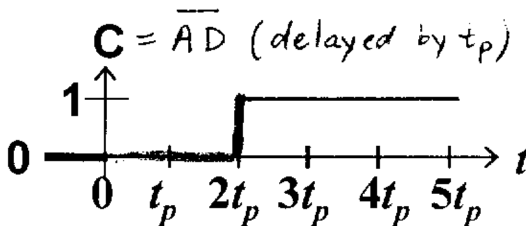
For the given **S** and **R** timing diagrams below, draw the timing diagrams (for $t > 0$) for **A**, **B**, **C**, and **D** on the plots provided. **[13 pts]**

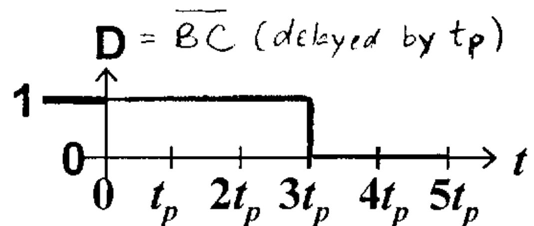






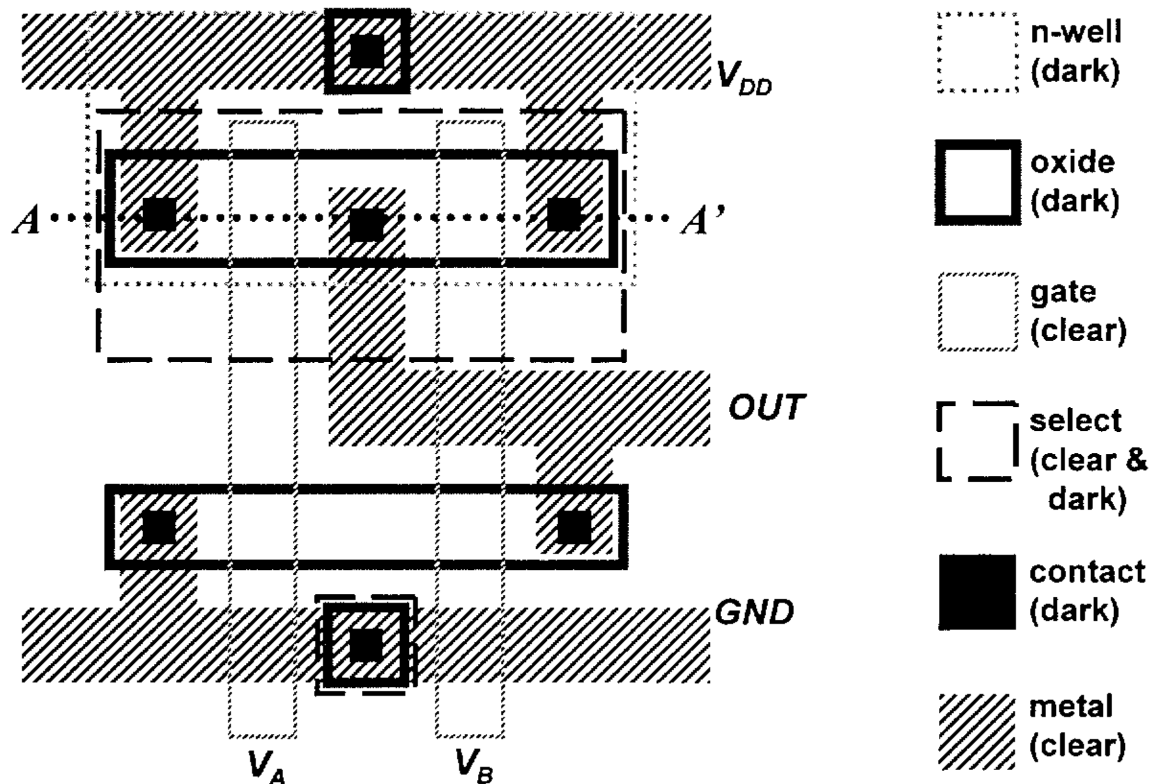






		NAND
0	0	1
0	1	1
1	0	1
1	1	0

Problem 7: CMOS Technology [20 points in total]
The layout of a CMOS logic gate is shown below:

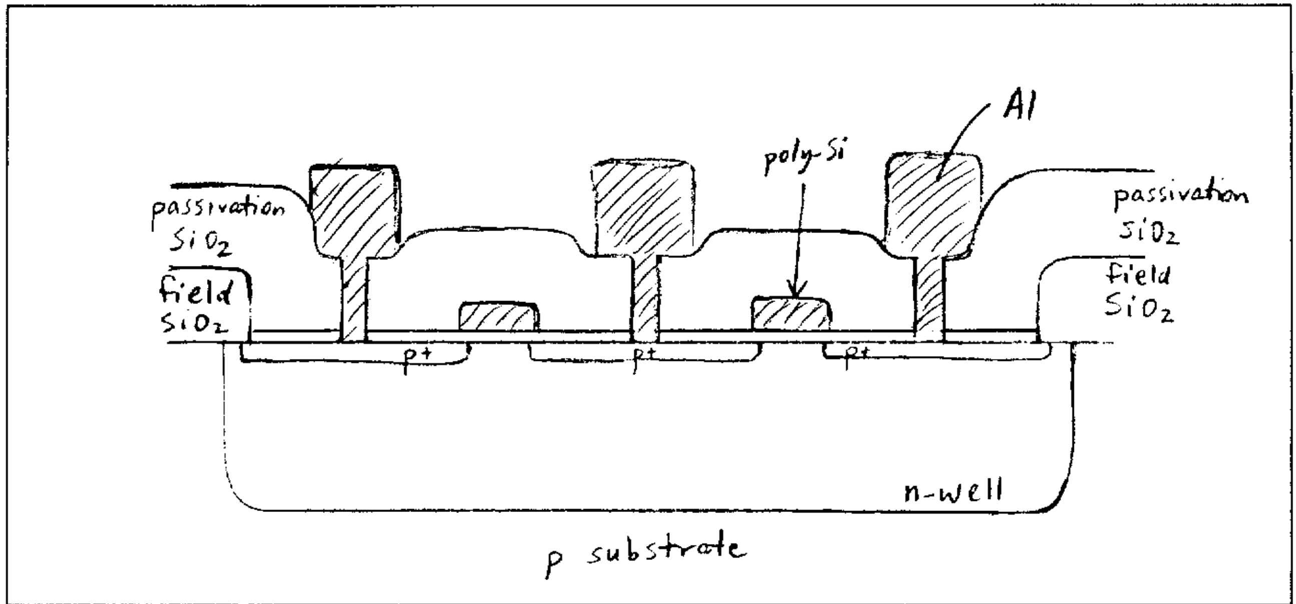


The following fabrication process (starting with a p-type Si wafer) is used:

1. Thermally grow 700 nm of SiO_2.
2. Pattern the SiO_2 using the n-well mask.
3. Implant phosphorus and perform a high-temperature, long anneal to "drive in" the well to a depth of 1 μm.
4. Remove the SiO_2 (using a highly selective wet etch process which does not etch Si).
5. Grow 0.5 μm of SiO_2 ("field oxide").
6. Pattern the SiO_2 using the oxide mask.
7. Thermally grow 10 nm of SiO_2 ("gate oxide") in the bare regions of the Si.
8. Deposit 200 nm of poly-Si (by CVD).
9. Pattern the poly-Si using the gate mask.
10. Use clear-field select mask to pattern photoresist; implant phosphorus. This will form the n+ source and drain junctions for the n-channel MOSFETs.
11. Use dark-field select mask to pattern photoresist; implant boron. This will form the p+ source and drain junctions for the p-channel MOSFETs.
12. Thermally anneal the wafer in order to activate the implanted dopants. The final source/drain junction depth is 100 nm.
13. Deposit 0.5 μm of SiO_2 ("passivation oxide").
14. Pattern the deposited SiO_2 using the contact mask.
15. Deposit 0.5 μm of aluminum.
16. Pattern the aluminum using the metal mask.

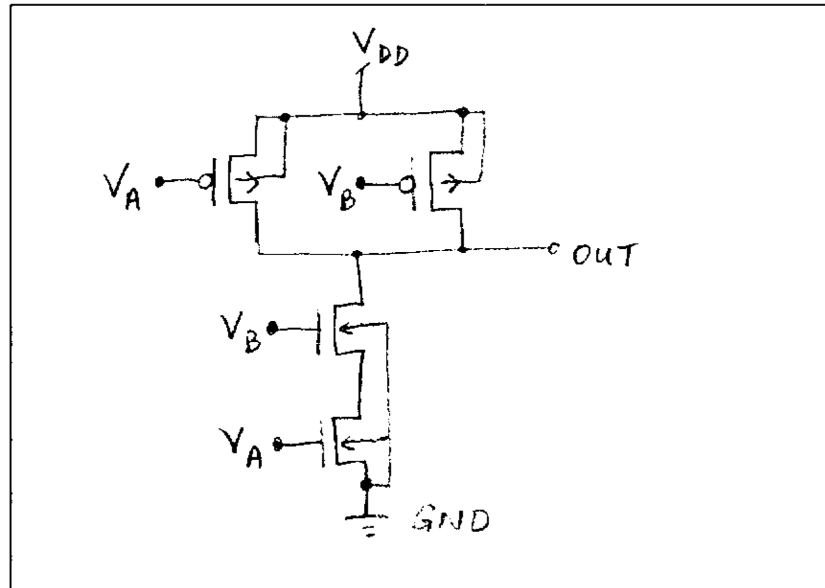
Problem 7 (continued)

a) Draw cross-section *A-A'* in the space provided. Identify all layers clearly. **[10 pts]**



Cross-section *A-A'*

b) Draw the circuit schematic, labeling V_{DD}, *GND*, V_A, V_B, and *OUT*. **[5 pts]**



Circuit Schematic

c) Assuming that $k_n' = 3k_p'$, would you expect this logic gate to have comparable worst-case "pull-up" and "pull-down" propagation delays? (Is $t_{pLH} \cong t_{pHL}$?) Justify your answer. **[5 pts]** Yes!

pull-up : $R = R_p \propto \frac{1}{(W/L)_p k_p'}$

pull-down : $R = 2R_n \propto \frac{2}{(W/L)_n k_n'}$

For $R_p = 2R_n$, $\left(\frac{W}{L}\right)_p k_p' = \left(\frac{W}{L}\right)_n k_n'/2$

$= \left(\frac{W}{L}\right)_n \frac{3k_p'}{2}$

$\Rightarrow \frac{(W/L)_p}{(W/L)_n} = \frac{3}{2}$ which is indeed the case!

Problem 8: Technology Scaling (Short-Answer Questions) [10 points in total]

a) Explain how transistor scaling improves both the cost (per function) and performance (circuit operating speed) of CMOS integrated circuits. **[5 pts]**

The circuit layout area and hence the chip area is reduced when the size of the transistor is reduced. Thus, more chips can be fabricated on a single wafer, and the cost per chip is reduced. (Note that the cost of a processing a wafer increases only moderately as technology is advanced.)

The output capacitance (due to drain pn junction capacitances, MOSFET gate capacitances, and wiring capacitance) is reduced

→ propagation delay $\propto C_{output}$ is reduced,

so logic gates can be operated at higher clock frequencies.

b) Explain why interconnect delay is becoming more of a concern as CMOS technology advances. **[5 pts]**

The spacing between the wires which interconnect the transistors is scaled down together with the lateral dimensions of the transistors. At the same time, the height of the wires is not being scaled down (in order to minimize the increase in resistance per unit length). Therefore, coupling capacitance per unit length between these wires increases, so that interconnect delay does not scale down as quickly as transistor delay. Thus, interconnect delay is a growing issue, particularly for long wires (used to route "global" signals).