Department of Electrical Engineering and Computer Sciences
College of Engineering
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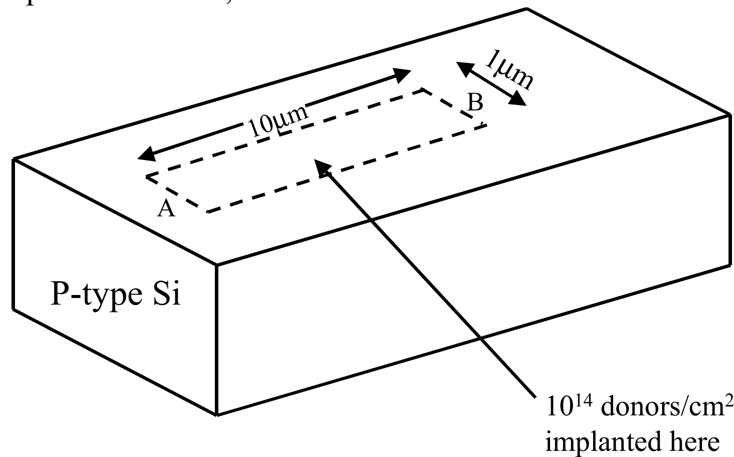
EECS 40 Summer 2002

Problem Set 9
Due Mon July 29 at 12pm

Problem 1: Sheet Charge and Resistance

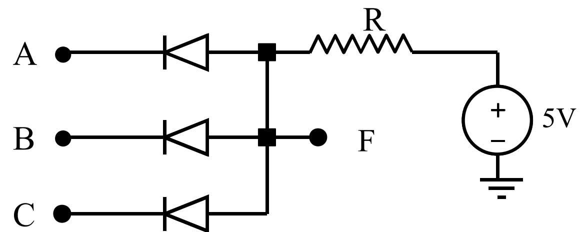
You make an integrated resistor with ion implantation in which you shoot a certain number of donors per square cm into a region of p-type Si. In the ion-implanted region the number of donors far exceeds the number of acceptors, so we simply consider the ion-implanted region to be n-type. Now you are not sure just how deep the n-type region is because you do not know the penetration depth of the ions. But you plunge on foolishly to calculate the resistance. You do not know the volume doping (donors/cm^3) and the thickness of the doped layer, but you do know the product of doping and thickness; this is the number of dopant atoms/cm^2, here 10^{14} donors/cm^2.



a) Assume the electron mobility is 1000cm^2/V-sec. If you attach contacts to the n-type region at the ends (A-B), what is the resistance R_{AB}? (Hint: plunge ahead with the resistor formula, leaving the thickness of the layer as some unknown t_x. Maybe you will find out that you do not even need it!

b) Obviously the resistance is proportional to the length (here 10μm), and inversely proportional to the width (here 1μm). What is the formula for the resistance of a square resistor (length = width) in terms of mobility, electronic charge and doping per cm^2? (We call this the sheet resistance of the n-type layer.) Hint: again, the depth of the implant (the thickness of the n-type layer) plays no role.

Problem 2: Logic Gates with Diodes



Logic gates can be made out of diodes. See the figure to the right. Using the perfect rectifier model find V_F and write a truth table for F with logic "1" corresponding to 4-5V and logic "0" corresponding to 0-1V. What type of logic gate does Figure 2.1 implement? Now use the large-signal diode model

(0.7V drop when diode on) and comment on the logic level problem, i.e. when can the gate fail?

Problem 3: Capacitor

Suppose we want to fabricate an MOS capacitor. The process sequence is:

1) Start with n-type wafer
2) Grow 200nm of silicon dioxide.
3) Do photolithography to end up with a positive photoresist layer covering the wafer except in a region 10 x 10 μm square.
4) Etch away the oxide in the 10 x 10 square with an etchant that does not attack either photoresist or silicon.
5) Remove the photoresist.
6) Deposit 15nm silicon dioxide (relative dielectric constant = 3.9)
7) Deposit an aluminum layer over the wafer.
8) Do photolithography to end up with a positive photoresist layer in a region 20 x 20 μm square, centered over the region of thin oxide.
9) Etch the exposed part of the aluminum film in an etchant that does not attack oxide, Si, or photoresist, so that only the 20 x 20 square of Al remains, centered over the thin oxide region.
10) Remove the photoresist.

a) Make a sketch of the structure, both top view and cross-section.
b) Show the masks used to fabricate the structure. Indicate if they are clear-field or dark field.

Calculate the capacitance, including both the thin-oxide and thick oxide components. What percentage of the total capacitance is the capacitance associated with only the thin oxide region.

Problem 4: Thermal Oxidation

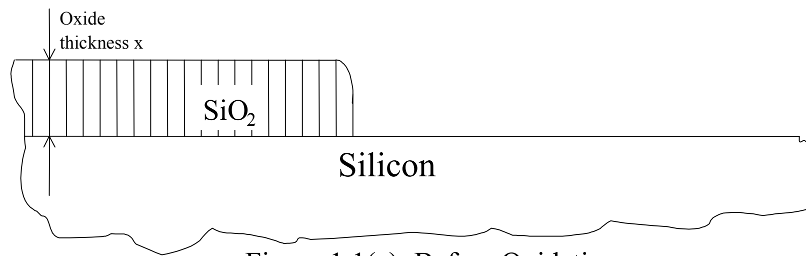


Figure 1.1(a): Before Oxidation

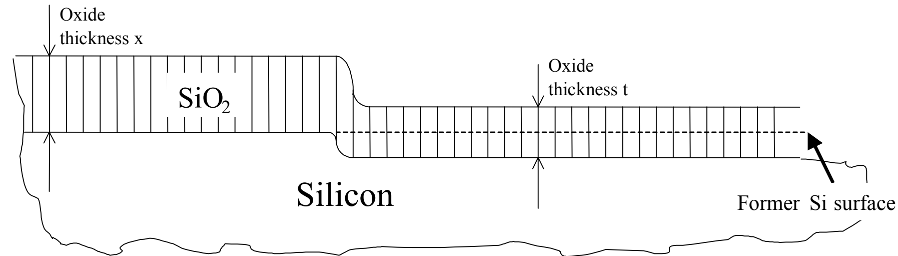


Figure 1.1(b): After Oxidation

When silicon is oxidized at high temperatures, the "thermal oxide" forms by consuming silicon. As a result, the interface between the SiO_2 film and the Si moves. As shown in the right side of Figure 1.1(b), the grown thermal oxide is half above and half below the original silicon surface. This is because in growing an oxide layer of thickness t we lose a thickness t/2 of silicon (to provide the Si needed in the silicon dioxide. This result holds if the silicon is not covered by an oxide layer before oxidation.

The left side of Figure 1.1 shows the effect of oxidation on silicon already covered by a thick SiO_2 layer. In this case the SiO_2 layer does not increase much in thickness during the thermal oxidation step because the oxide growth rate slows down as the oxide gets thicker. Note that at the boundary between the left side and right side of Figure 1.1(b), there is a step in the Si surface created by the different consumption rates of silicon in the two regions.

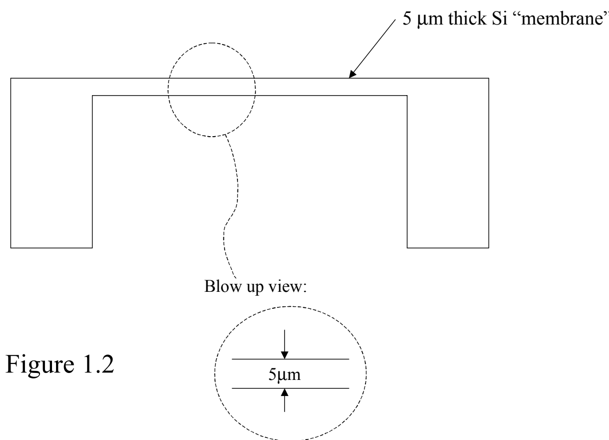


Figure 1.2

Figure 1.2 shows a partially fabricated silicon diaphragm structure that is used in microscopic pressure sensors. Now suppose we put this in a furnace with steam to thermally grow 1µm of SiO_2 on this structure. Carefully sketch a magnified view of the membrane part of the oxidized structure. Hint: Thermal oxidation grows oxide on all surfaces.

Note that SIMPLer does not really take the loss of silicon into account; in other words SIMPLer treats thermal oxidation and deposition of SiO_2 identically.

Problem 5 SIMPLer Warm-up
Fire up SIMPLer … see our Web Page. If you have questions about loading SIMPLer onto your PC, there are a few tips on the web page. Otherwise run it as a web applet. In any case, the location of SIMPLer stuff is given on our main web page, and I have recently downloaded it and run it on my computer as a test (Ben).
The first time choose one of the existing processes (in the "choose process" window that appears every time you hit restart. Just play around with it; modify it as you like; examine cross-sections, etc. Carry out the capacitor process of Problem 3, using SIMPLer. Print out the result and include with your homework.

Problem 6 MOS Parameter Extraction
Examine the MOS transistor curves in Figure 13.41, page 523 in the text book. (Interestingly, these curves were obtained in 1971 on a very early MOS transistor that was quite large by today's standard. It was estimated that the oxide thickness was about 150nm and the gate length was about 7.5μm.) Assume that this device is to be used in a digital system with V_{DD} = 6V, which will also be the logic high level.

(a) For this transistor what are I_{DS} and λ?
(b) Assuming this device has W=50, L = 7.5 μm, what are I_{DS} and λ for a device with W/L = 15/7.5?