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EECS 40 Summer 2002 **Ben Wild**

Problem Set 2 (due July 5 at 12PM)
Note: Problem set must be placed in EECS 40 boxes outside 275 Cory by 12PM
DO NOT BRING TO CLASS - that is too late

Problem 1 Refer to the solutions to Problem 4 from PS #1 This is a simple 2-input Exclusive OR realized with 5 NAND gates.
(a) Consider possible input transitions such as A remaining low and B going from high to low, or the opposite, or A and B going from low to high together, or….. How many different transitions are possible? Hint: it is more than 10!
(b) Compare two transitions starting with A=0, B=1. If either A goes to 1 or B goes to 0, the output will toggle from 1 to 0. Do these two transitions have the same number of gate delays? What are they?

Problem 2 We have a 4-input logic function (inputs **A,B,C,D** and output **F**). **F** is true only if **ABCD** = **0101.** Construct the circuit for **F** using (a) **NAND** gates of up to 4 inputs, (b) **NAND** gates with only 2 inputs. (Hint: first figure out how to construct a 4 input **NAND** gate out of 2 input **NAND** gates. It takes quite a few.)

Problem 3

(a) Another circuit you can construct with 4-input **NAND** gates is a 2-bit comparator. This is a circuit that compares two binary numbers (here each of 2 bits) and outputs a 1 only if the numbers are identical. Clearly there are 16 possibilities of which only 4 give a output "true". Call one number $\mathbf{A_1A_2}$ and the second $\mathbf{B_1B_2}$ with the output **F**. Write the Boolean expression for F and show the logic circuit using **NAND** gates of up to 4 inputs.

(b) Design a 2 bit comparator using 2 input **XOR** gates and 2 input **NAND** gates.

Problem 4 A 2:1 multiplexer circuit has 3 inputs, A, B and S. The output Z is equal to A if S = 0, and B if S = 1. (a) Write down the truth table of the output Z based on the inputs A,B,S. (b) From the truth table write down a Boolean expression for Z as a function of A,B,S. (c) Simplify this expression using the distributive law (**AB + CB = (A+C)B**) and the identity law (**$A+\overline{A} = 1$**) (d) show an implementation of this circuit using only 2 input **NAND** gates.