EE40, Fall 2001 W. Oldham

Problem Set#13
Due Dec 3, but accepted until Dec 5 at 3:10PM
(Last problem set this semester !)

Problem 1: Effect of Fanout

The coupled inverters in the circuit below can be switched at a maximum frequency of 38.1MHz (This is computed from the 0 to VDD/2 transition time and the VDD to VDD/2 transition times that are equal. Note that

- All NMOS transistors in this circuit have the same channel width W_n and length L_n.
- All PMOS transistors in this circuit have the same channel width W_p and length L_p.
- $W_p = 2W_n$ and $L_p = L_n$, which implies that $R_p = R_n$.

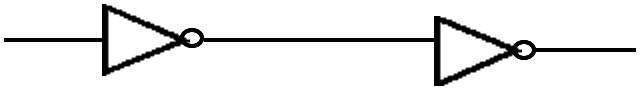


Figure 1.1

Determine the performance of the following circuit (Figure 1.2). Assumptions to make for the circuits of Figure 1.2: 1) Device sizes in any stage will be adjusted to achieve the same effective worst-case R_p and R_n values as the simple inverter (thus for example the NOR gates require doubling the PMOS Widths, and NAND gates require doubling the NMOS widths). 2) In parts (a) and (b) we will assume that the gate capacitances dominate and that they are proportional to the gate width.

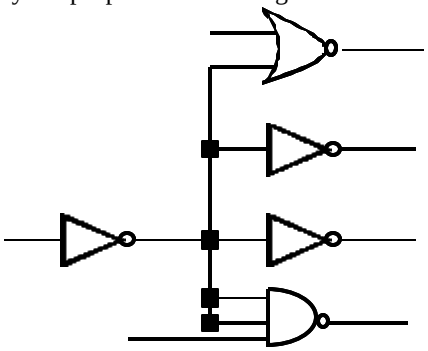


Figure 1.2

a) With these assumptions what will the gate delay of the first inverter, assuming it is not resized from that of Figure 1.1?

b) Now suppose we resize the first inverter to keep the same gate delay. By what factor must the transistor widths increase? (do not worry about driving the first inverter, remember we have a near-square wave driving it so the larger input capacitance of inverter one will not slow its performance in this example).

c) Now consider the effect of drain capacitance on question (b). Assume that in the original inverter chain of Fig. 1.1, the drain capacitances contributed to 25% of the loading of any node (of which the p-channel contributed 2/3 and the n-channel 1/3 because of their relative sizes). When we resize the first inverter to drive the large fan-out load, we necessarily increase its drain capacitances; consequently it will not speed up the circuit as much as we planned. Take this fact into account and recompute part (b).

Problem 2: Chip Power

Some of the advanced processor chips claim ~100M devices clocked at 2GHz. If the devices have a capacitance of about 1fF, what is the chip power, assuming all are clocked at 2GHz? Assuming there really are 100M devices and the clock runs at 2GHz, yet the chip power is only around 20W, what is the explanation?

Problem 3a: Comparator Analysis

We did not finish the design of the hysteresis in the lectures. In particular, what is the equation describing the size of the + feedback PMOS transistor in the low-to high transition. (The equation should give the PMOS device size in W/L relative to the input stage PMOS device W/L as a function of the desired shift in the input threshold compared to a zero feedback case).

Problem 3b: Comparator Design

You are to design a 2.5V comparator using 2.5V CMOS. The device is to switch at 1.15 and 1.35 V, in other words it has a hysteresis of 0.2V width. Assume the technology is 0.25µm CMOS with the same specifications as in Lecture 23 except that the input inverter is 10 time larger than the minimum, i.e. $(W/L)_n$ = (10µm / 0.25µm) $(W/L)_p$ = (20µm / 0.25µm).

Problem 4: Tapering

In the examples given in lecture 23, we looked at 1 and 3 stages of buffering with geometrically related device sizes. What is the individual-stage delay and total delay for the same problem (50pF load) if the number of buffered stages is increased from 3 to 5? (Hint: it's even better!).

Problem 5: More on Tapering

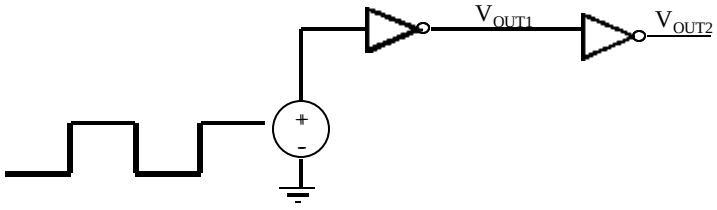
Lets do a slightly more accurate estimate of the benefits of tapering. Suppose we have a 1pF load (long on-chip wire) driven by the same system as considered in Lecture 23 (0.25 micron technology). But in this problem we assume that large CMOS devices result in a large drain capacitance, typically about 20% of the gate capacitance for a similar-sized device. If you include the drain capacitance, can you compute the following:

a) What is the delay if you drive the load with the direct output of a minimum sized device? (In this system the normal gate delay is 10nS without including the drain capacitance)
b) Now you insert an additional 2 stages of buffer. [Properly designed). What is the total stage delay through the 3 stages? Assume the drain capacitance increase in proportion to the W/L.

Problem 6: Inverter Switching f_{SQW}- square wave drive

Assume that the following circuit switches continuously, driven by a symmetric square wave that oscillates from 0 to 2.5V at frequency f. The CMOS inverters have the following circuit parameters:

C_{Gn}= 50fF R_n = 1.6k V_{tl} = 0.7V
C_{Gp} = 50fF R_p = 3.2k V_{th} = 1.8V



Note that in this configuration the output of the first inverter never reaches V_{DD} or ground before it is switched in the opposite direction. The value it reaches on the way down must be equal to or less than V_{tl} in order for the second inverter to toggle correctly. Similarly it must rise at least to V_{th} before reversing, again in order for the second inverter to toggle correctly.

We wish to find the maximum switching speed/frequency of the first inverter in the circuit. That is, we want to find the maximum possible frequency of the input square wave such that V_{OUT1} has enough time to reach V_{th} volts for input low and reach V_{tl} volts for logic high.

(a) In this asymmetric gate the rise and fall times will be different. Which transition (output falling or output rising) will limit the response? Note that during this transition the output of inverter one will

just reach the valid logic condition, and during the other transition, it will go well beyond the logic valid condition.

(b) Write an equation that describes V_{OUT1} during its pull down transition of the oscillation. Let the pull up transition start at t = 0 and end at $t = t_1$. Similarly write an equation for the pull down transition which begins at $t = t_1$ and ends at $t = t_2$. (What are the relationships between t_1, t_2 and the frequency f?)

(c) Find the maximum switching frequency of the circuit and the range of V_{OUT1}.

Problem 7A: Ring Oscillators 1 (short warmup problem)

Figure 7.1 shows a ring oscillator circuit consisting of three identical inverters. Figure 7.2 shows part of the waveforms of V_{OUT1} and V_{OUT2}. V_{th} and V_{tl} are also identified on the figure.

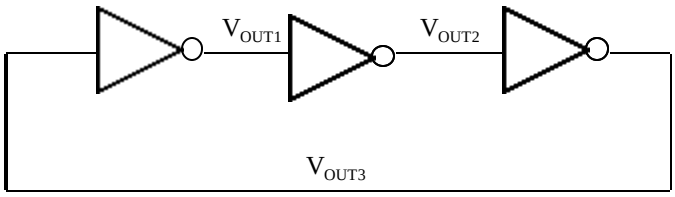


Figure 7.1

(a) Using the initial information about V_{OUT1} and V_{OUT2}, finish plotting V_{OUT1} and V_{OUT2} and sketch V_{OUT3} in the space provided above.

(b) From your sketch, determine the oscillating frequency. Verify that the period of oscillation equals to 2*(number of inverters)*(average propagation delay) where for ring oscillators the average propagation delay is the time to rise from 0V to V_{th} plus the time to fall from V_{DD} to V_{tl}. Note that to a good approximation, the highest output voltage of each inverter in the ring oscillator is *roughly* V_{DD}; the lowest output voltage is roughly zero.

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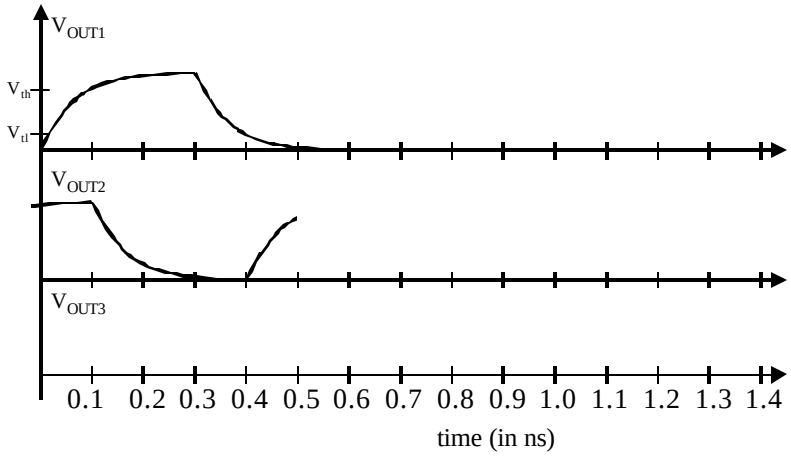

Figure 7.2

Problem 7B: Ring Oscillators - the calculation of f_{SQRO}

We have a 1001 stage ring oscillator. Each inverter in the oscillator has has the following parameters:

V_{DD} = 2.5V V_{tl} = 0.9V V_{th} = 1.6V C_{Gp} = 20fF C_{Gn} = 10fF C_{jA} = 1.5fF/μm^2

Drain area for p-channel: $2\mu m^2$

Drain area for n-channel: $1\mu m^2$

R_n = 4K and R_p =5K .

Each inverter is connected to each other through an interconnect wire. The interconnect wire has an area of $10\mu m^2$ with C_{wire} = .1fF/μm^2. The interconnect resistance is negligible.

Find the frequency and period of the 1001 stage ring oscillator. What is the frequency associated with a single stage, f_{SQRO} (the ring oscillator frequency divided by 1001).