EECS40 Summer 2002

Problem Set 12
Due Fri Aug. 9 at 3PM

Problem 1: **CMOS NAND GATE DELAYS**

Consider the Exclusive OR realization using 5 two-input NAND gates from problem set 1. Suppose another 2-input NAND gate ("stage 0") drives the input A. We want to estimate the worst-case gate delay of stage 0 in 0.25μm CMOS logic. Assume:
V_{DD} = 2.5V , $|V_t|$ = 0.5 for both NMOS and PMOS, k_{VS} = 50μA/V for NMOS, 25 for PMOS, and λ=0.04 for both devices. Gate oxide is 4nm (not 40 as in the last prob set), and again, drain capacitance is 1fF per square μm. Assume a drain length of 4λ (from earlier problem sets), i.e. 0.5μm in this technology . OOPS this is the design-rule λ, not the λ used above to describe the device I-V slope. Also, use a W/L ratio of 4 for the smallest transistor in the design.

a) compute Rn and Rp for stage 0
b) compute all the capacitances loading the node A and add them to get the total C.
c) What is the stage delay (in fSec) ?

Problem 2: CMOS Layout

Use SIMPLer to lay out a basic CMOS NAND gate with device sizes of W/L = 4. Wire the input in polysilicon and the output in metal. Try to make the layout reasonably compact. Do not bother to show select masks; i.e. show only 5 masks.

Problem 3: Complex Logic Functions in CMOS

a) Draw a CMOS static logic circuit that evaluates the function $\overline{F} = D + A \bullet (B + C)$
b) What is F for part a? (hint: this corresponds rather closely to the PMOS pullup).

Problem 4: Delays in Complex Logic Functions

a) Specifiy the devices sizes for the circuit of Problem 3a. Assume that the smallest NMOS devices have W/L of 4/1 and that the PMOS devices have just half of the k_{VS} of the NMOS devices. We want equal worst-case pull up and pull down circuit delays.
b) Assume that the load is node A of an identical logic block. What is the total capacitive load at the output node in terms of the gate capacitance per unit area and drain capacitance per unit area In this calculation we estimate the drain area as the device width times 4λ times the drain capacitance per unit area (see problem 1).
c) If the technology is the same as in Problem 1, what is the numerical value of the gate delay?

Problem 5: Flip Flops

a) Text 11.29
b) Text 11. 31 (Ignore hint (2) in part a. because it is misleading). For part a just start with the initial condition D = 1, CK = 0 and figure out X, Y, W, Z. Then recalculate X, Y, W, Z after each transition (Clock back to zero, D to 1, Clock up to 1, and clock back to zero. For part b you should assume that Q was initially 0 (so you see a transition when the clock goes high)