EECS40 Summer 2002

Problem Set 11
Due Mon Aug. 5 at 12PM

Problem 1: **Transfer curve (Vout versus Vin for a CMOS inverter).**
In Prob. Set 10, you were to generate I-V graphs for both NMOS and PMOS devices. If you did this correctly (check with the solutions), you have NMOS I-V in quadrant 1 and PMOS in quadrant 4. By over laying these graphs in a sensible way you can generate the transfer curves of a static CMOS inverter quite easily. What you should do was described in Lecture 18:

(a) Draw the inverter circuit diagram
(b) Find the relationship between I_{Dnmos} and I_{Dpmos}
(c) Find the relationship between V_{DSnmos} and V_{DSpmos}
(d) Find the relationship between Vin and V_{GS} for both NMOS and PMOS (for example if Vin is 1V, what are the two V_{GS} values?
(e) Use a graphical load line method to find I_D and V_{DS} for several different input voltages. (Obviously if you figure out how to make the graphs, the points are just the intersection of the response of the NMOS IV and PMOS IV curves at a given input voltage).

You will not have many points based on the limited set of curves you computed in PS 11, so feel free to compute more curves if you wish. Otherwise take liberty with sketching a guess.

Problem 2: Capacitance Values

In Problem Set 10 Problem 4 you also did a layout of a CMOS inverter. Your job here is to compute four capacitance values: C_{GS} for NMOS and PMOS and C_{DB} for NMOS and PMOS. You should consult the solutions sheet so everyone starts with the same device sizes. For this problem lets assume that drain capacitance is about 1fF per square μm. You have enough information to compute the gate capacitance per unit area (gate oxide thickness is 40nm and the relative dielectric constant is 3.9 and for free space ε_0 is 8.85×10^{-14} F/cm^2.)
Again, compute the four capacitances (units of fF or pF would be nice, please).

Problem 3: Resistance Values

On Problem Set 8, Problem 6 you found out that the effective resistance in discharging a capacitor from V_{DD} to $V_{DD}/2$ with a current source of constant current I_{DS} is approximately $0.75V_{DD}/I_{DS}$. (exact answer was $0.725V_{DD}/I_{DS}$). This is reasonable because, looking at the I-V graph of the current source we are moving from the point V_{DD}/I_{DS} to$0.5V_{DD}/I_{DS}$;thus the average is about $0.75V_{DD}/I_{DS}$. This crude approximation is equally valid (error less than 5% in computing delay) for current sources with a slope (i.e. MOS transistors with $\lambda > 0$). Hence we stated the formula for the effective R found in Lecture 15 (and even showed that it was pretty accurate for estimating the gate delay).
We want you to find the effective R for the NMOS and PMOS transistors of Problem Set 10, Problem 4 (The same device considered in Problem 2 above). These are 0.25μm devices. Assume that k_{VS} is 100μA/V for the NMOS and 50 for the PMOS device. V_{DD} for these devices is 2.5V, and V_T is 0.5V.

Problem 4: Gate Delay

Suppose we have a chain of inverters of the type considered in Problems 2 and 3, that is a circuit in which one inverter's output is connected to the input of the next, etc (i.e. each has a fanout of 1). Calculate the stage delay by considering the hypothetical situation of one input suddenly going high and observing how fast the output goes low. The delay τ_{HL} is defined as the time for the output to go from V_{DD} to V_{DD} /2. Also compute the delay when the input of one of the gates suddenly goes from high to low. Again the delay, $\tau_{LH,}$ is defined as the time for the output of that inverter to go from 0 to V_{DD} /2. You should obviously use the results of problems 2 and 3 in this calculation.