

Problem Set 10
 Due Fri Aug. 2 at 12pm

Problem 1: Field Effect

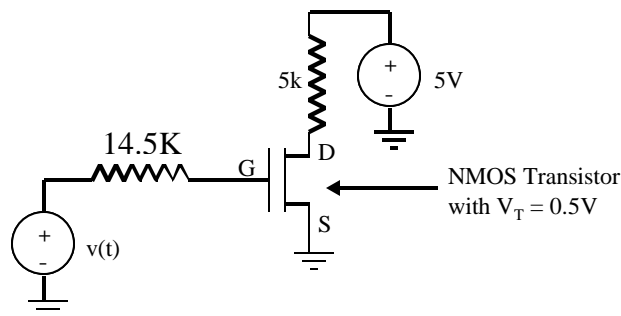
Let us calculate the result of an ideal field-effect device made by holding a metal plate (a "gate") just off the surface of a p-type Si substrate. Suppose the gap is only $0.01\ \mu\text{m}$ with the result that the capacitance per unit area (ϵ/d) is $8.85 \times 10^{-8}\ \text{F}/\text{cm}^2$, or $8.85 \times 10^{-4}\ \text{pF}/\mu\text{m}^2$.

- a) If we assume for simplicity that the threshold for inducing a negative charge of electrons on the surface is 0V , what is the charge per unit area at a gate-to-substrate voltage of 10V ?
- b) Assume the mobility of the electrons is $1000\text{cm}/\text{Vsec}$. What is the low-field sheet resistance of the electron layer for $10\ \text{V}$ gate bias.
- c) Suppose there were some way to contact a region $1\ \mu\text{m}$ wide by $0.2\ \mu\text{m}$ long, i.e. you have current flowing through a "sheet resistor" of electrons with geometry: length of resistor $0.2\ \mu\text{m}$ and width $1\ \mu\text{m}$. What is the current at a voltage of $0.1\ \text{V}$ applied across the resistor (remember there is still 10V gate to substrate voltage for the purpose of inducing the electron charge on the surface).
- d) If the velocity saturates abruptly at a field of $10\text{KV}/\text{cm}$ and the saturated velocity is $10^7\ \text{cm}/\text{sec}$ can you sketch the approximate I-V characteristics of this little "sheet resistor" which is $0.2\ \mu\text{m}$ long and $1\ \mu\text{m}$ wide? (Again for $10\ \text{V}$ applied to the gate to induce the electron charge). Hint: assume simple linear low-field behavior up to the applied voltage at which the velocity, and thus the current, suddenly saturates.

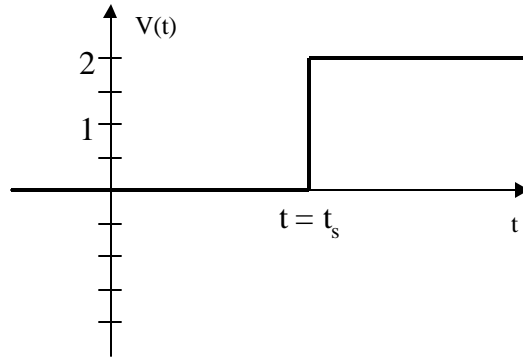
Problem 2: MOS Gate Charging

The MOS transistor below is made by forming a gate over an insulating oxide layer. The gate dimensions are: $W = 50\ \mu\text{m}$ by $L = 1\ \mu\text{m}$. The oxide thickness is 10nm and the relative dielectric constant of the oxide is 3.9 . (Free-space dielectric constant is $\epsilon_0 = 8.85 \times 10^{-14}\ \text{F}/\text{cm}$.)

- a) What is the gate capacitance per unit area (in units of $\text{fF}/\mu\text{m}^2$)? [Hint: femto = 10^{-15}]
- b) What is the gate capacitance? (units of fF)



$v(t)$ has the following graph:



- c) Note that $v(t)$ jumps from 0V to 2V at $t = t_s$. Sketch the gate voltage versus time (nsec? psec?) and find the time at which $V_{GS} = 1.5V$. (Assume that the only capacitance at the gate node is the MOS gate capacitance.)

Problem 3. SIMPLer Error

What is the error in the NMOS.SPF file in the SIMPLer kit? Hint, go through the process and see what is wrong....the NMOS device would not work.

Problem 4: Design Rules and Tolerance

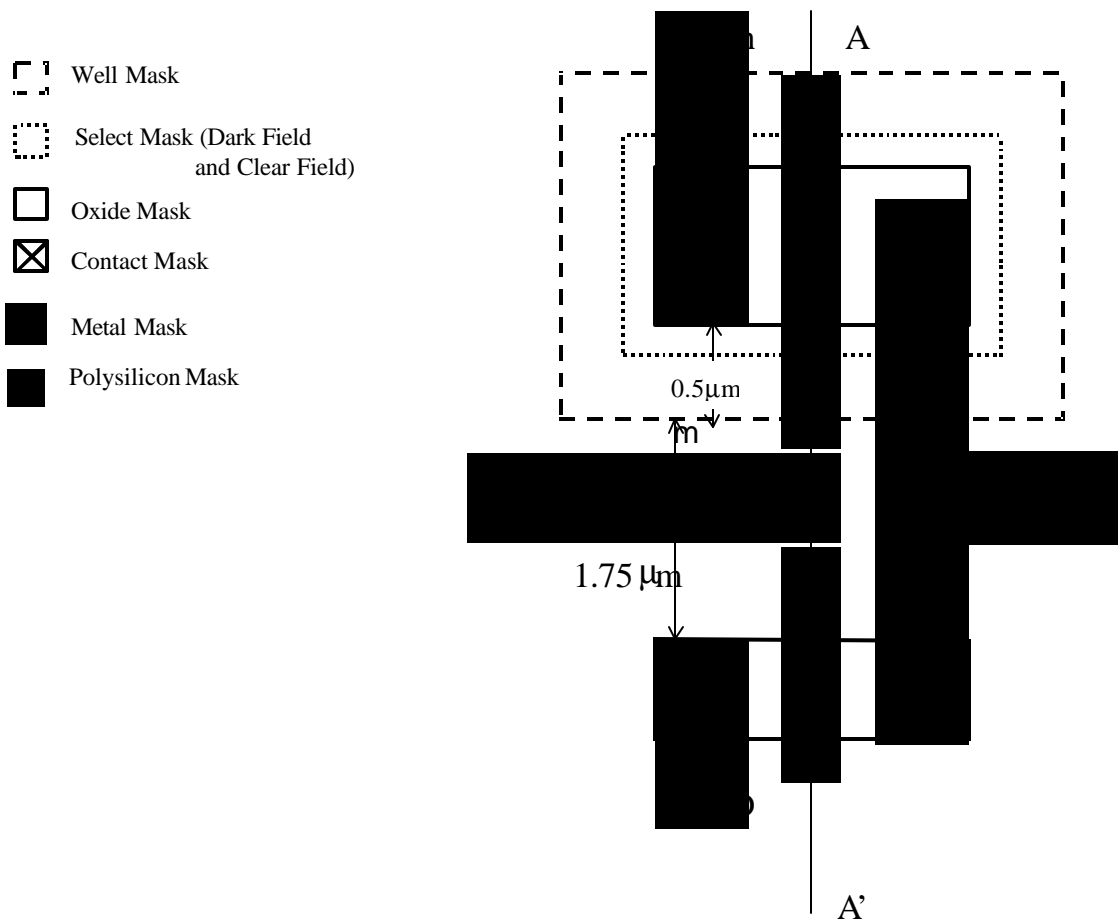


Figure 4.1

Figure 4.1 shows the general shape of a “quarter micron gate” CMOS inverter. In other words this is a “ $\lambda = 0.125\mu\text{m}$ ” process. The node labeled “Vhigh” is where V_{DD} is connected and is the most positive voltage in the circuit. GND is the lowest voltage..

The following processing steps were used:

1. p-type starting material; grow 500nm of oxide and pattern with n-well mask.
2. Implant phosphorus and anneal (“n-well drive in”) to a depth of 2 microns (or micrometers).
3. Strip off oxide and then grow 500nm of oxide and pattern with oxide mask.
4. Grow 40nm of thermal SiO_2 .
5. Deposit 750nm of CVD n^+ polysilicon and pattern using polysilicon mask.
6. Use dark field select mask and photoresist to implant the boron (acceptors).
7. Use clear field select mask and photoresist to implant the arsenic (donors).
8. Anneal implants to form source and drain regions that have a thickness of 250nm.
9. Deposit 500nm of oxide and pattern using the contact mask.
10. Deposit 1 micron of metal and pattern using the metal mask.

Obtain some graph paper (ruled in two dimensions) so that you can make very neat circuit layouts. You are to lay out the CMOS inverter so that it meets the following design rule specifications:

First the basic "default rules"

1. The minimum feature size is ($2*\lambda$) = $0.25\mu\text{m}$. Thus the gate length and the contact size are both $0.25\mu\text{m}$.
2. The safety margin for overlay error/tolerance is (λ) = $.125\mu\text{m}$.

Next some special rules:.

3. The minimum NMOS transistor to PMOS well spacing is $1.75\mu\text{m}$ or $7*\lambda$ (see Figure 4.1).
4. The minimum PMOS transistor inside the well spacing is 2λ or $0.5\mu\text{m}$. See Fig. 4.1.
5. Put as many contacts to source and drain areas as fit (all contacts are square).
6. Do not show contacts to polysilicon.
7. You provide a single contact to the well that has a minimum spacing to PMOS source-drain regions of 4λ . This is not shown on the present layout. You do not need to provide a contact to the p-type substrate.

The n-channel MOS has a (W/L) of 5; the p-channel MOS has a (W/L) of 10.

Your task is to neatly lay out the circuit using minimum spacing. Make your sketch by hand on grid paper ... it will take several attempts. You may also layout your result using SIMPLer, but that is probably more work than just using grid paper. The idea is that you put things as close together as possible, but never violating a design rule. For example two metal lines can never be closer than 2λ , etc. You should also put as many contacts into the source and drain regions of your layout that fit. Indicate if each mask is a dark field or clear field mask. You may want to also layout your result using SIMPLer. For simplicity, ignore the select masks in the layout. As you know they are almost copies of the well mask (except for the well contact area). Thus you need to show the location

of 5 masks in your layout. In all hand drawings use the same conventions as shown in the drawings above (dashed lines for well mask, X in squares for contact mask, etc.)

Problem 5: Translating Layouts into Circuit Diagrams

For reference, here are the circuit diagrams for the NMOS and PMOS transistors:

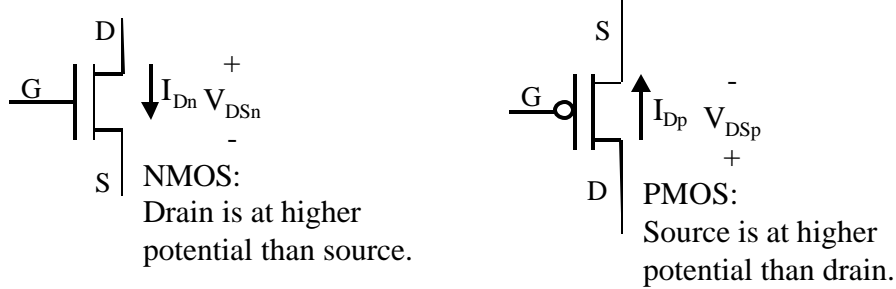


Figure 5.1

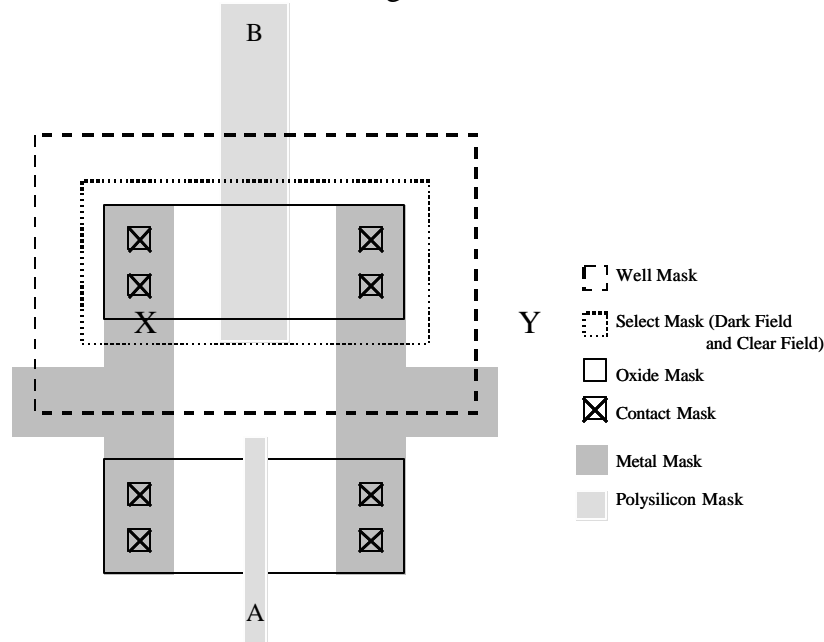


Figure 5.2

Suppose we process the layout shown in Figure 5.2. Note that the nodes (A and B and X and Y) have been identified on the layout.

The same CMOS processing steps are used as in Problem 4 above.

- (a) Translate Figure 5.2 into a circuit using the circuit symbols shown in Figure 5.1.
- (b) Now suppose we apply the above processing steps to the layout in Figure 5.3. Several nodes have been identified on the layout, namely A, B, V_{high} (voltage corresponding to logic high), GND (ground), and V_{OUT} . Translate Figure 5.3 in terms of the circuit symbols shown in Figure 5.1. Hints: You might find it very helpful to draw rough sketches of the cross sections X-X', Y-Y', and Z-Z'.

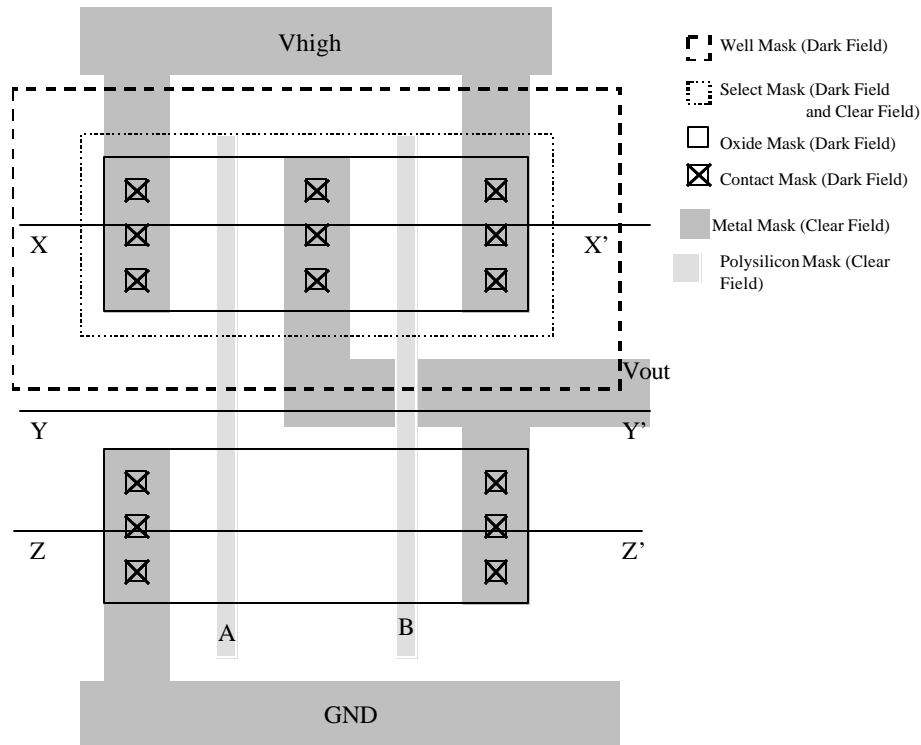


Figure 5.3

Problem 6: NMOS and PMOS I-V Characteristics

Consider a "quarter micron" technology that has the properties that follow. At gate-to-source voltages beyond threshold and drain to source voltages above saturation, velocity saturation limits the high-field drain current in both N and P-MOS to a constant value whose magnitude is given by $I_D = I_{DS}(1 - \lambda V_{DS})$. Moreover I_{DS} is given by the simple equation $I_{DS} = k_{VS}(W/L)(V_{GS} - V_t)$. The threshold voltage V_t , k_{VS} , and λ are given in the table below. We also give the approximate voltage V_{DSAT} at which the drain current saturates. For lower values of V_{DS} , we approximate the device as a simple resistor with an I-V characteristic passing through the origin and the point $I_{DS}(1 - \lambda V_{DSAT})$

	NMOS	PMOS
V_t (volt)	0.5	-0.5
k_{VS} ($\mu\text{A}/\text{volt}$)	$50\mu\text{A}/\text{V}$	$25\mu\text{A}/\text{V}$
λ	0.05	0.05
V_{DSAT}	1V	1V

- Neatly draw the I_D versus V_{DS} characteristics of a $2\ \mu\text{m}$ wide NMOS device at gate voltages of 0, 0.5, 1, 1.5, 2, 2.5 V.
- How wide would W need to make the PMOS device in order to get the same current (magnitude) in saturation as the $2\ \mu\text{m}$ wide NMOS devices (for equal values of $|(V_{GS} - V_t)|$).
- Now draw the I_D versus V_{DS} characteristic of this PMOS device. Use the same 0.5V intervals in $|(V_{GS} - V_t)|$. We strongly suggest you draw it in the fourth quadrant for PMOS (both I_D and V_{DS} are negative.) and use the same scale for both PMOS and

NMOS. You also need to keep a copy of the NMOS and PMOS characteristics. (This will be important for next week's problem set.)

Problem: CMOS Transfer Curve.

(Do not hand in... this is Problem 1 of the next Problem Set)

By over laying the NMOS and PMOS I-V graphs in a sensible way you can generate the transfer curves of a static CMOS inverter quite easily. (Its much like load-line problems you did on earlier problem sets). What you should do is

- (a) Draw the CMOS inverter circuit diagram
- (b) Find the relationship between I_{Dn} and I_{Dp}
- (c) Find the relationship between V_{DSn} and V_{DSp}
- (d) Find the relationship between V_{in} and V_{GS} for both NMOS and PMOS (for example if V_{in} is 1V, what are the two V_{GS} values?)
- (e) Use a graphical load line method to find I_D and V_{DS} for several different input voltages. (Obviously if you figure out how to make the graphs, the points are just the intersection of the response of the NMOS IV and PMOS IV curves at a given input voltage).
- (f) Plot two graphs: (1) V_{OUT} ($=V_{DS}$ NMOS) vs. V_{IN} ($=V_{GS}$ NMOS) and (2) I vs. V_{IN} .

You will not have many points based on the limited set of curves you computed in Problem 6, so feel free to compute more curves if you wish.