Department of Electrical Engineering and Computer Sciences
University of California, Berkeley

EECS 40 Summer 2002 **Ben Wild**

Problem Set 1 (Due July 1 at 11AM)
Note: Problem set must be placed in EECS 40 boxes outside 275 Cory by 11AM;
DO NOT BRING TO CLASS - that is too late

Problem 1 You are working out the logic for a burglar alarm for your apartment. You have switches on the front door, each of two windows and the garage door. The switches on the doors are closed when the doors are also closed; the switch on a particular window is closed when the corresponding window is closed. You construct a circuit at each switch that generates a "high" of 3V (i.e. logical 1) whenever the respective switch is closed and a "low" of 0V (logical 0) when a switch is open. Let's define logical variables F, W1, W2, and G to represent the conditions of the switches. (Thus, for example F = 1 if the front door is closed.) You also have a key switch to arm or disarm the alarm. It must be closed to activate the burglar alarm. Call this key function "K". Again, K=1 when this switch is closed. We can construct a truth table which gives the alarm condition as a function of F, W1, W2, G, and K. Let's call the alarm function "A"..

(a) Write out the truth table for A in terms of F, K, W1, W2 and G. This table of course has 32 rows, considering all possible binary values for the five input variables.
(b) Identify the row or rows in the truth table which produce the desired logical result (alarm variable is high when key switch is closed and one or more of the windows or door is open).
(c) Express this result as a sum of products logical expression. A= ?
(d) Show a possible overall circuit using only NAND logic gates.

Problem 2 Use a truth table to prove DeMorgan's Theorem:

$$A + B = \overline{(\overline{A} \cdot \overline{B})}$$

Hint: Simply construct a table with 4 columns: A, B, left hand side of above and right hand side. There need be only 4 rows, one for each possible combination of A and B.

Problem 3 Text Chapter 11 problem 11.5 (use sum of products form).

Problem 4 Text Chapter 11 problem 11.17 (use 5 gates to implement)

Problem 5 We revisit problem 4, but include the gate delays of each of the logic gates (including all NOT functions). See Problem 11.16 with respect to synthesis of NOT using CMOS. Assume that the gate delay for all gates is 20 nsec.

Assume that both inputs are 0, then one of the inputs switches to 1. Sketch the waveforms of all nodes on the path which is slowest.
Hint: For simplicity, we still show instantaneous transitions from high to low or low to high, but with the transition delay by the appropriate number of gate delays.