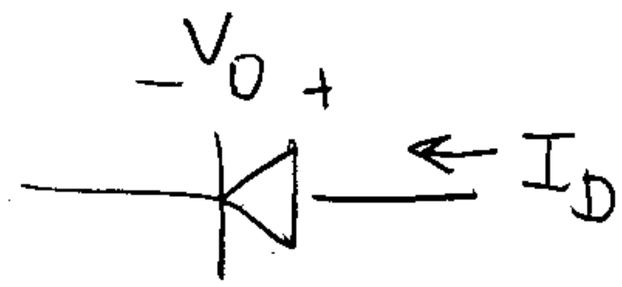
EE 40
Exam Review
Midterm 3

Topic: Diodes



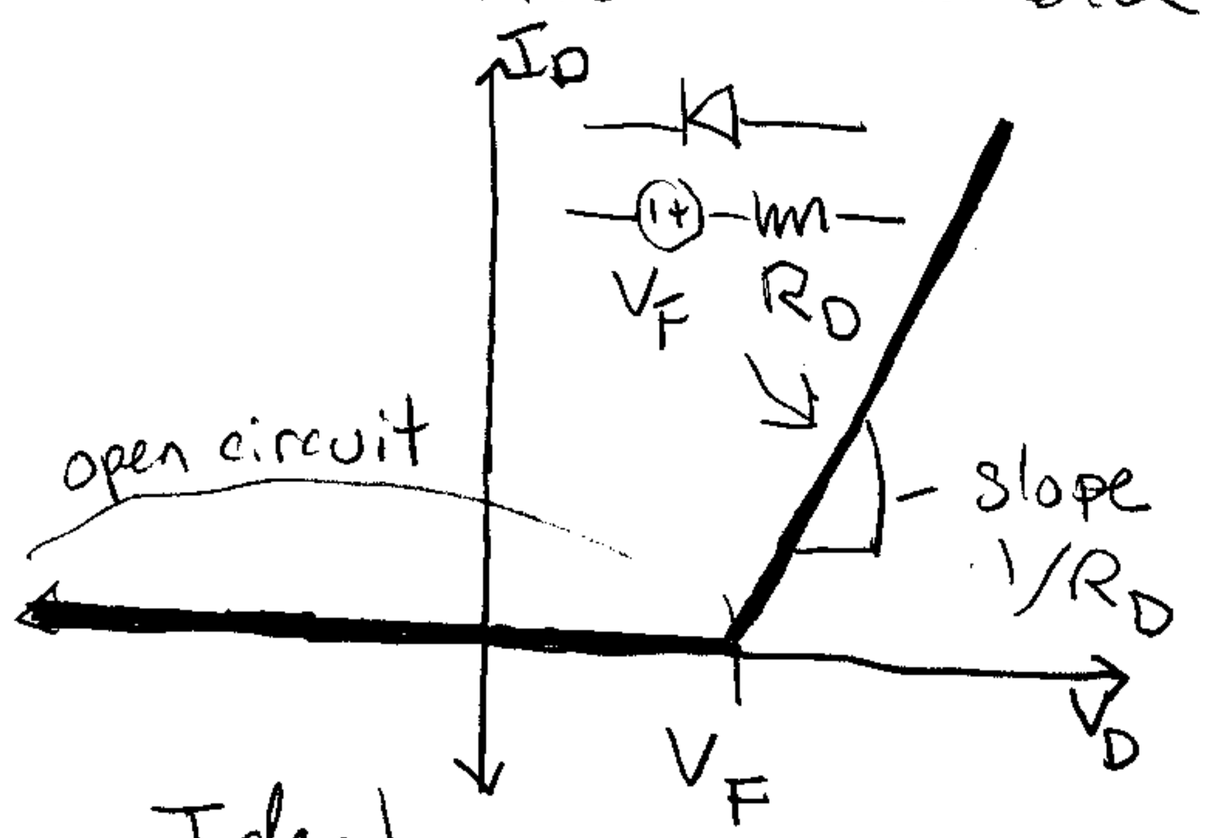
Diode Models (will be provided on exam)

Exponential
(most detailed but hardest)

$$I_D = I_0\left(e^{q\frac{V_D}{KT}} - 1\right)$$

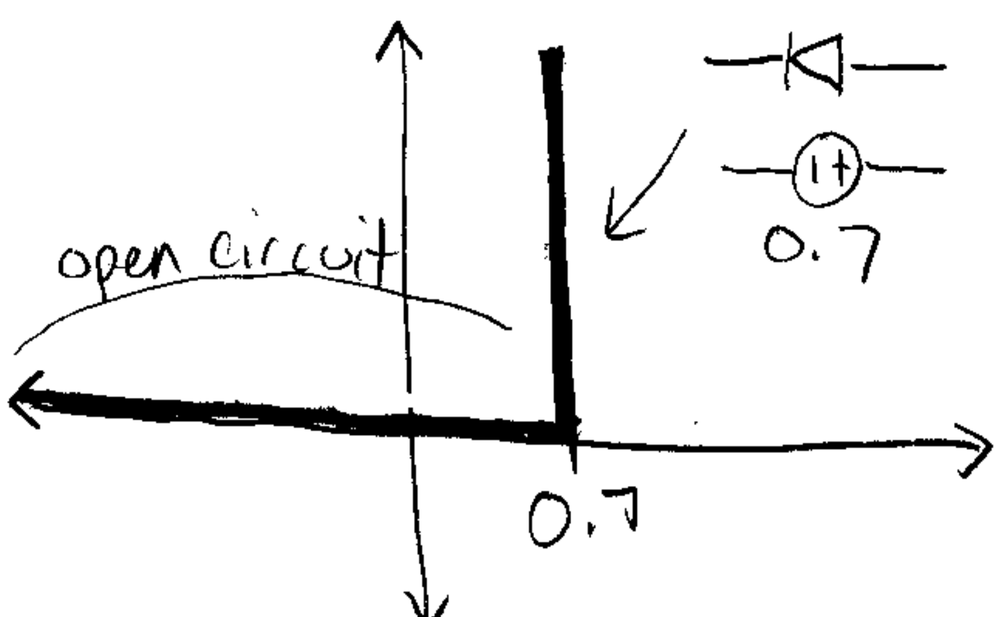
$$\left(\frac{q}{KT}\right)^{-1} \approx 0.026$$

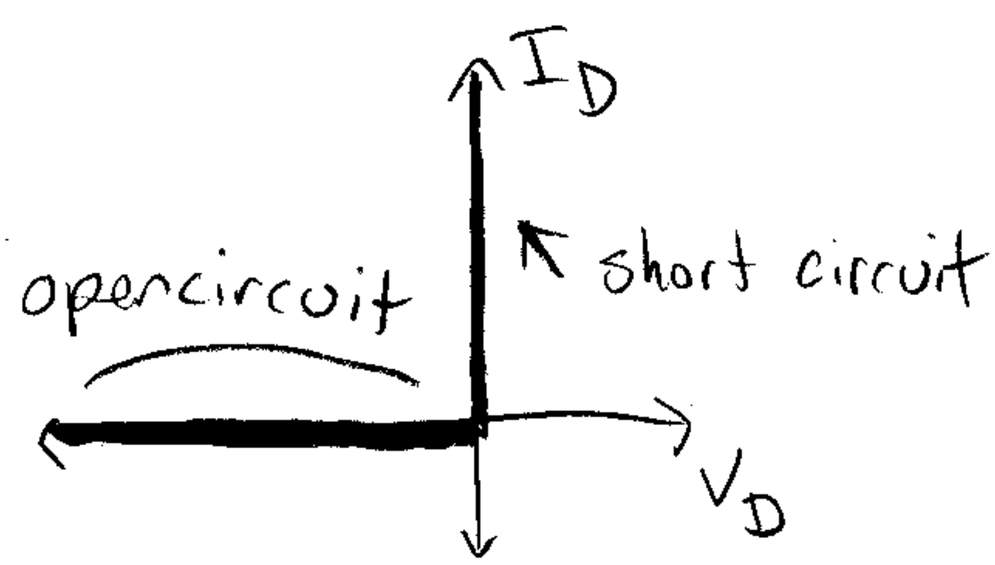
Small-Signal
(useful when voltage variation in diode must be considered)



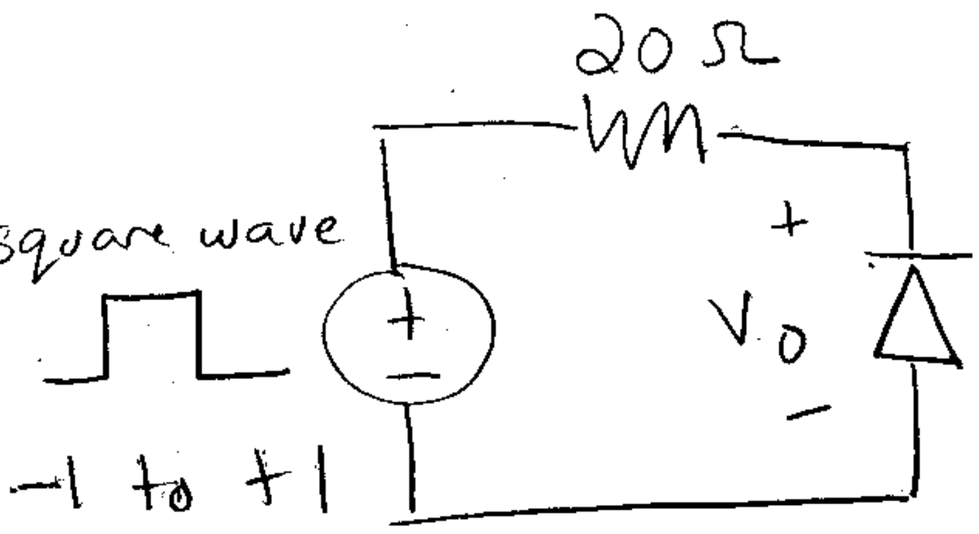
Ideal
(easiest but only gives basic idea of operation)

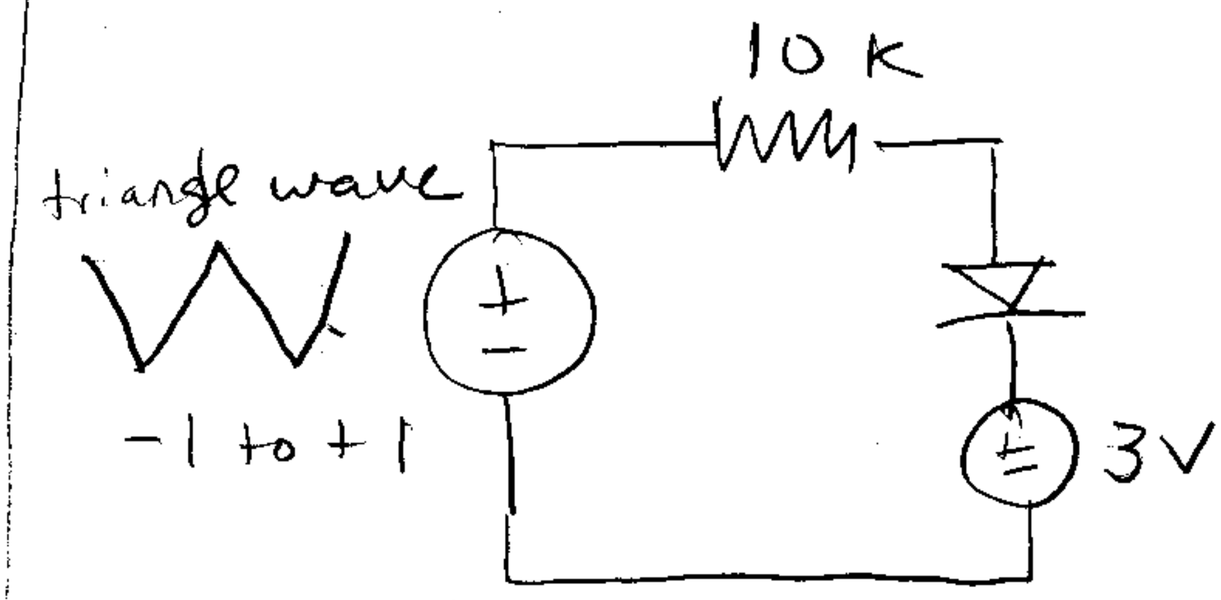
Large-Signal
(accurate enough for most purposes)

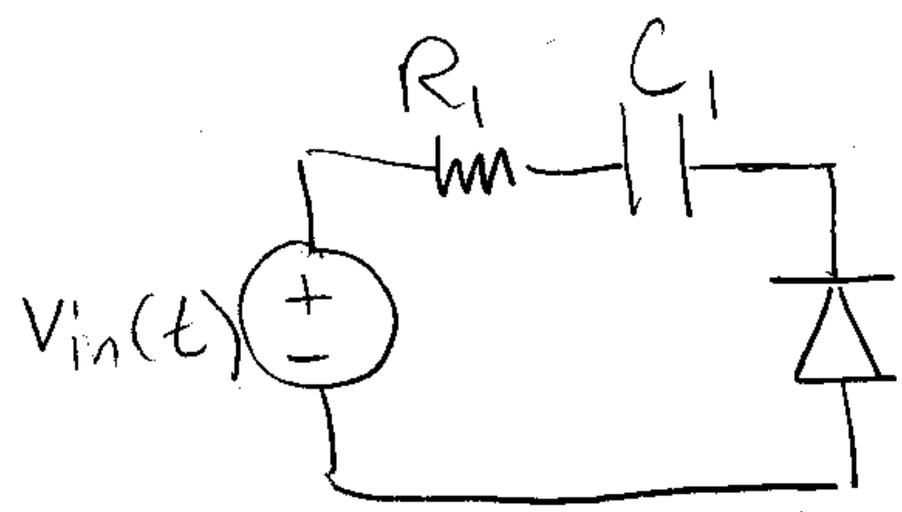


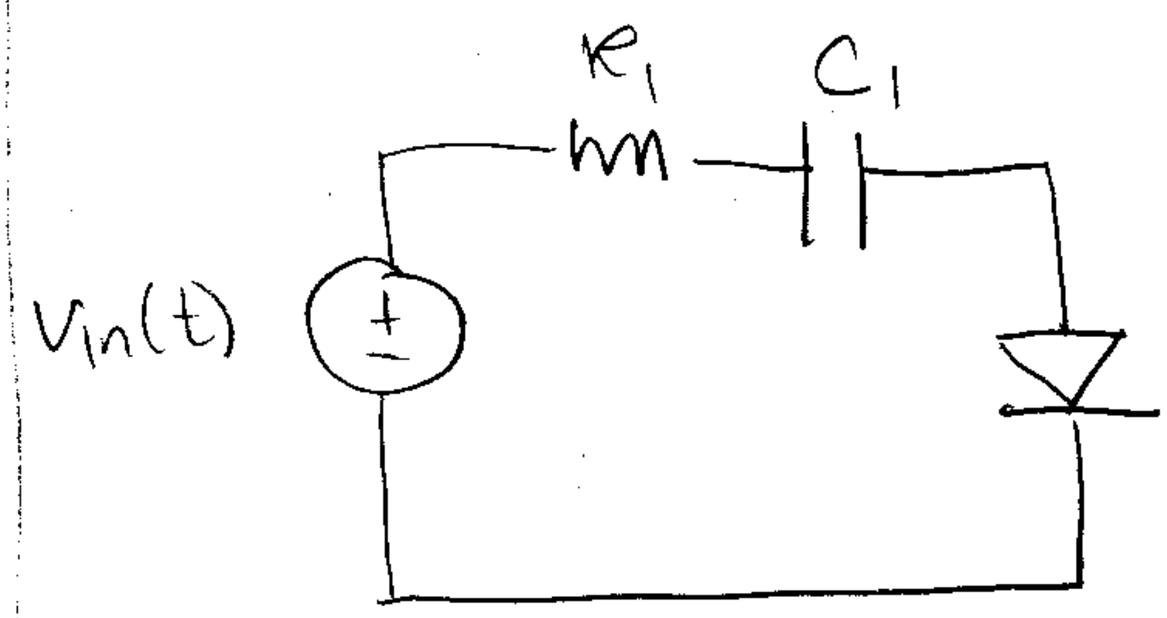


Analyze the following diode circuits using ideal, large-signal, and small signal models. Use $V_F = 0.6\ V$ and $R_D = 20\ \Omega$ for the small-signal model. Find $V_o(t)$ for each case.









$R_1 = 20\ \Omega$

$C_1 = 50\ pF$

$V_{in}(t)$ is square wave, frequency 1 Hz, amplitude 1 (-1 to +1)

Same parameters as ⟸

Topic: CMOS circuit logical operation

If you only need to know the logical operation of a circuit – the output for each possible combination of high/low inputs, a special transistor model may be used:

Because in this case

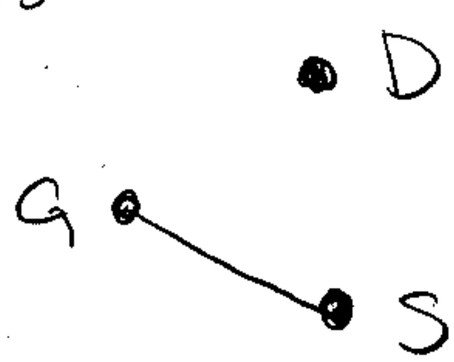
1) all transistor I_D currents are zero (as long as nothing is attached to output!)

2) all V_{GS} voltages are 0 or V_{DD} (high, negative for PMOS)

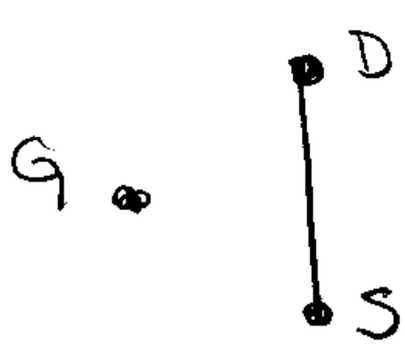
We use the following models:

NMOS

If $V_{GS}=0$



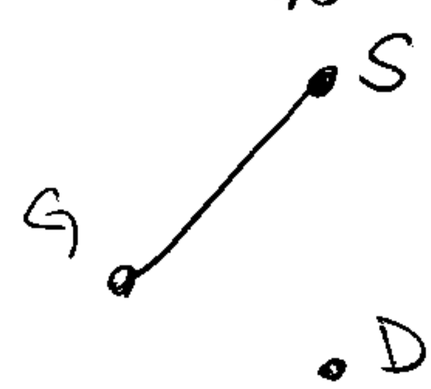
If $V_{GS}=V_{DD}$



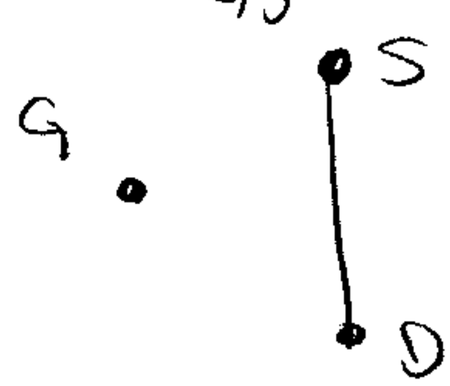
No current happens to flow thru wires!

PMOS

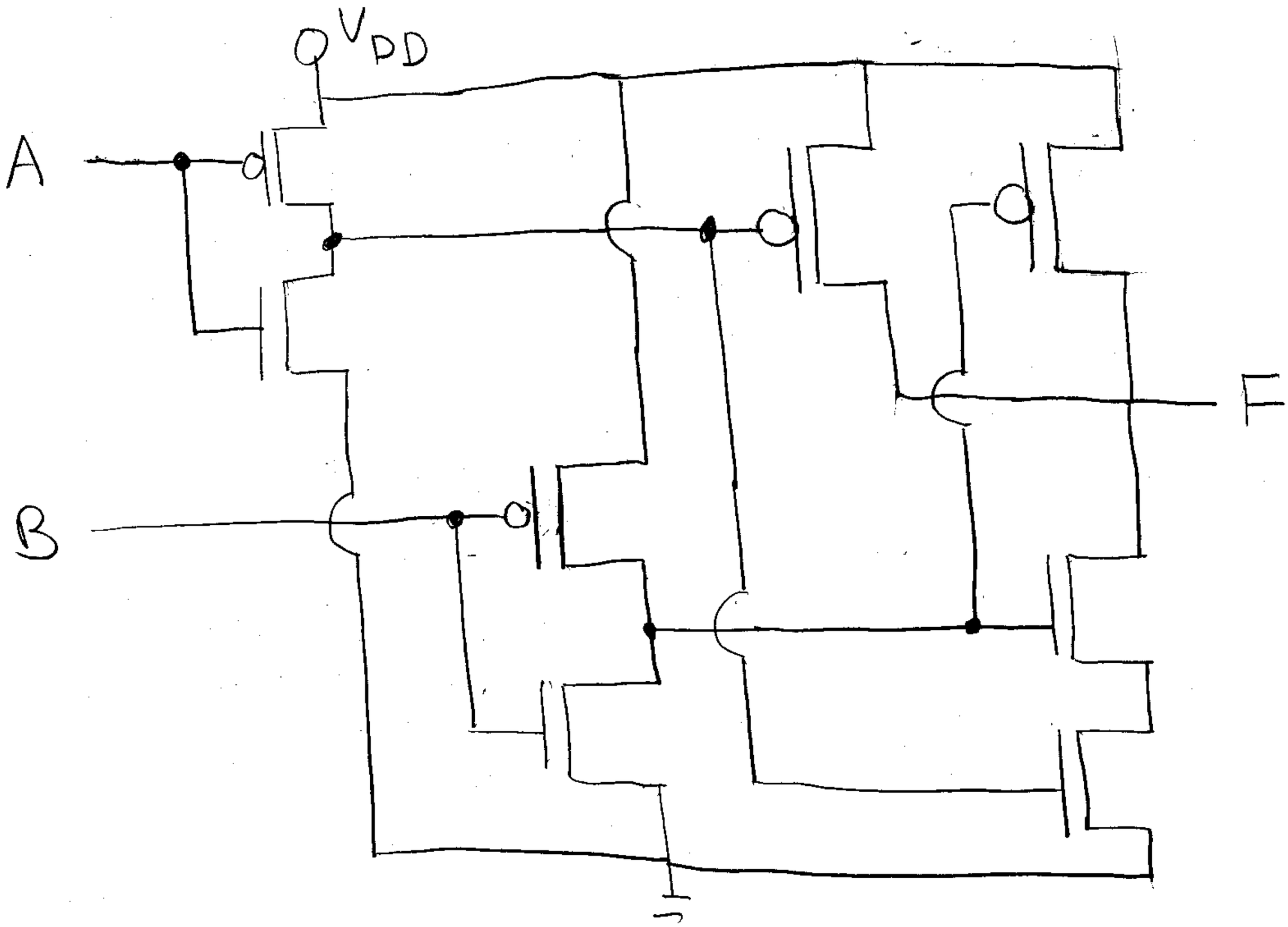
If $V_{GS}=0$



If $V_{GS}=-V_{DD}$



Create a truth table for the following circuit:

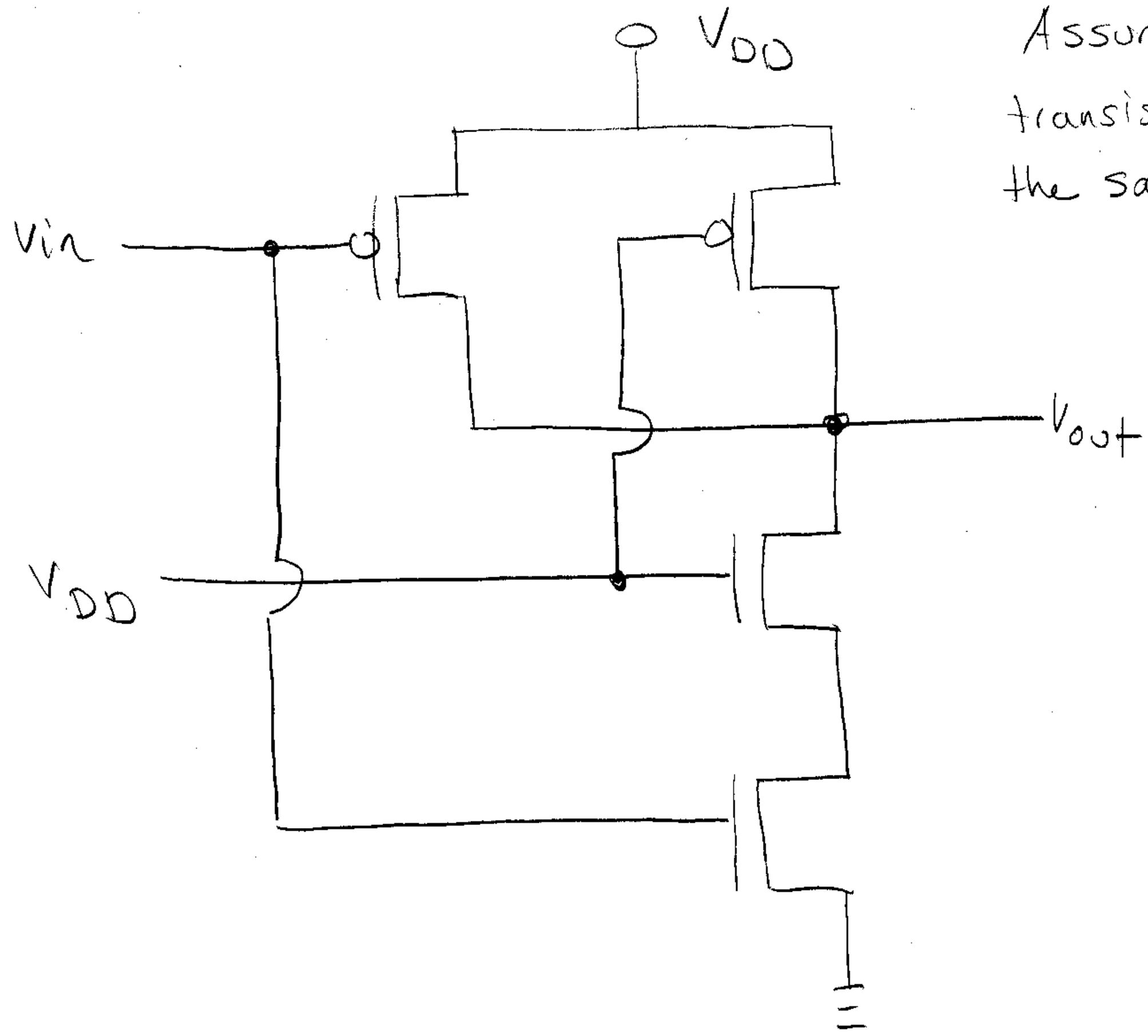


Topic: Making an educated guess about the mode a transistor is in

Principles:

- If V_{GS} is just above threshold, I_D is small
  - mode depends on what V_{DS} is.
    If V_{DS} very small $\Rightarrow$ triode
    Most likely, $V_{DS} > V_{GS} - V_T \Rightarrow$ saturation
- If V_{GS} is well above threshold,
  - V_{DS} can be seen from I_D:
    if I_D is small $\Rightarrow$ triode
    if I_D is large $\Rightarrow$ saturation
  - Mode can be seen from V_{DS}
    $V_{DS} \geq V_{GS} - V_T \Rightarrow$ saturation
    $V_{DS} < V_{GS} - V_T \Rightarrow$ triode

Find the mode that each transistor is most likely in when V_{in} is just above V_T and when V_{in} is just below $V_{DD} - V_T$.



Assume all transistors have the same $|V_T|$.

Topic: NMOS or PMOS transistor in a linear circuit - find I_D, V_{DS}

Use load-line method:

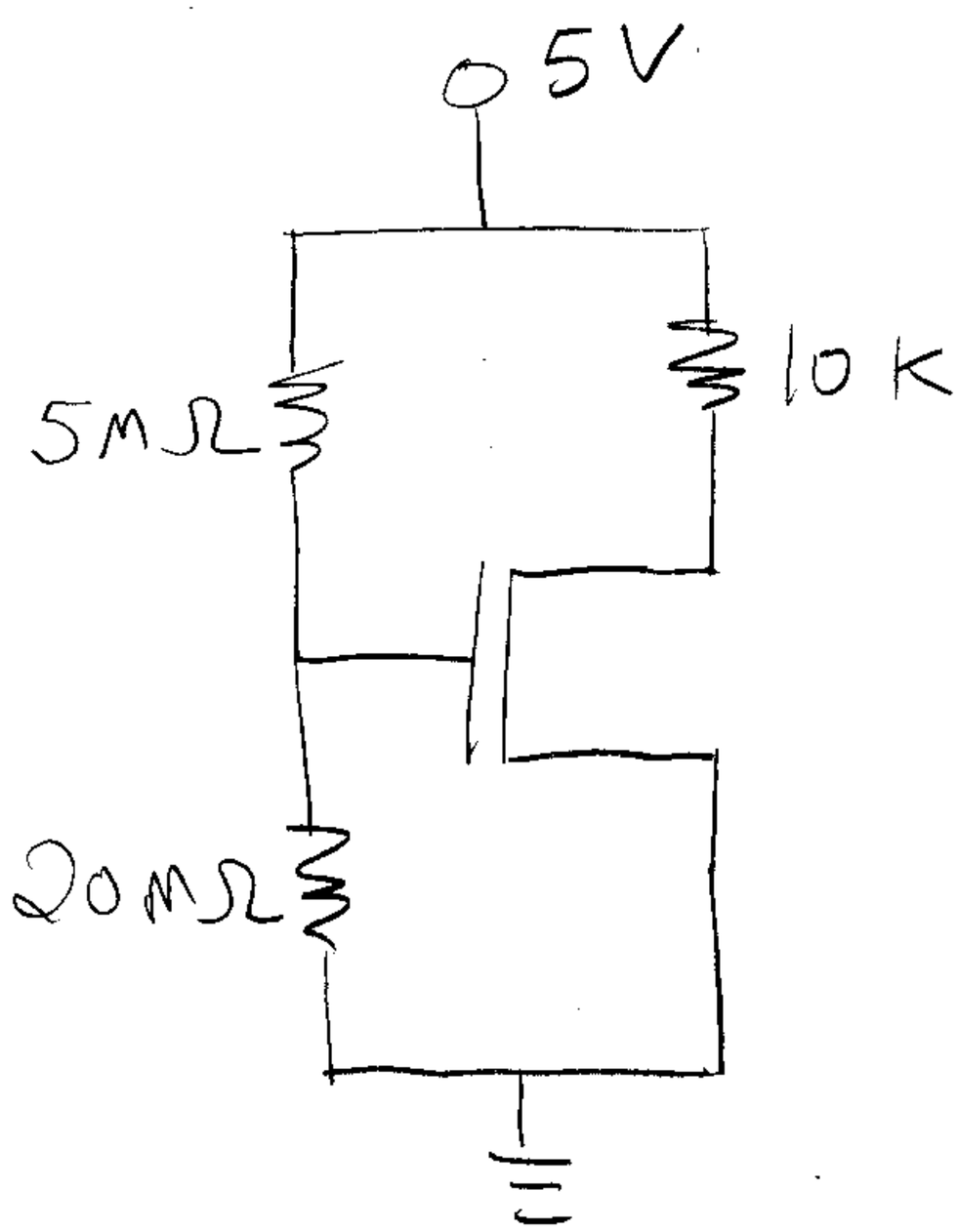
1) Find out how the linear elements relate I_D to V_{DS}. Write a linear equation.

2) Guess or reason out what mode the transistor is in. Write the equation for that mode.

3) Solve the linear equation and transistor equation together to get I_D & V_{DS}.

If the result conflicts with the mode of operation, repeat Step 2 with a different mode.

Find I_D for the transistor in the following circuit:



$\lambda = 0$

$V_T = 1\ V$

$I_{D_{SAT}} = 10^{-4}\ A$

Topic: CMOS circuit with 2 transistors, A and B. Solve for I_{D_A} & V_{DS_A} (I_D & V_{DS} for transistor A).

Use method similar to load line:

1) Relate I_{D_A} & V_{DS_A} to I_{D_B} & V_{DS_B} via 2 equations: usually KCL to relate I_{D_A} + I_{D_B} and KVL to relate V_{DS_A} & V_{DS_B}.

2) Guess the mode of transistor A and write the I_{D_A} vs V_{DS_A} equation.

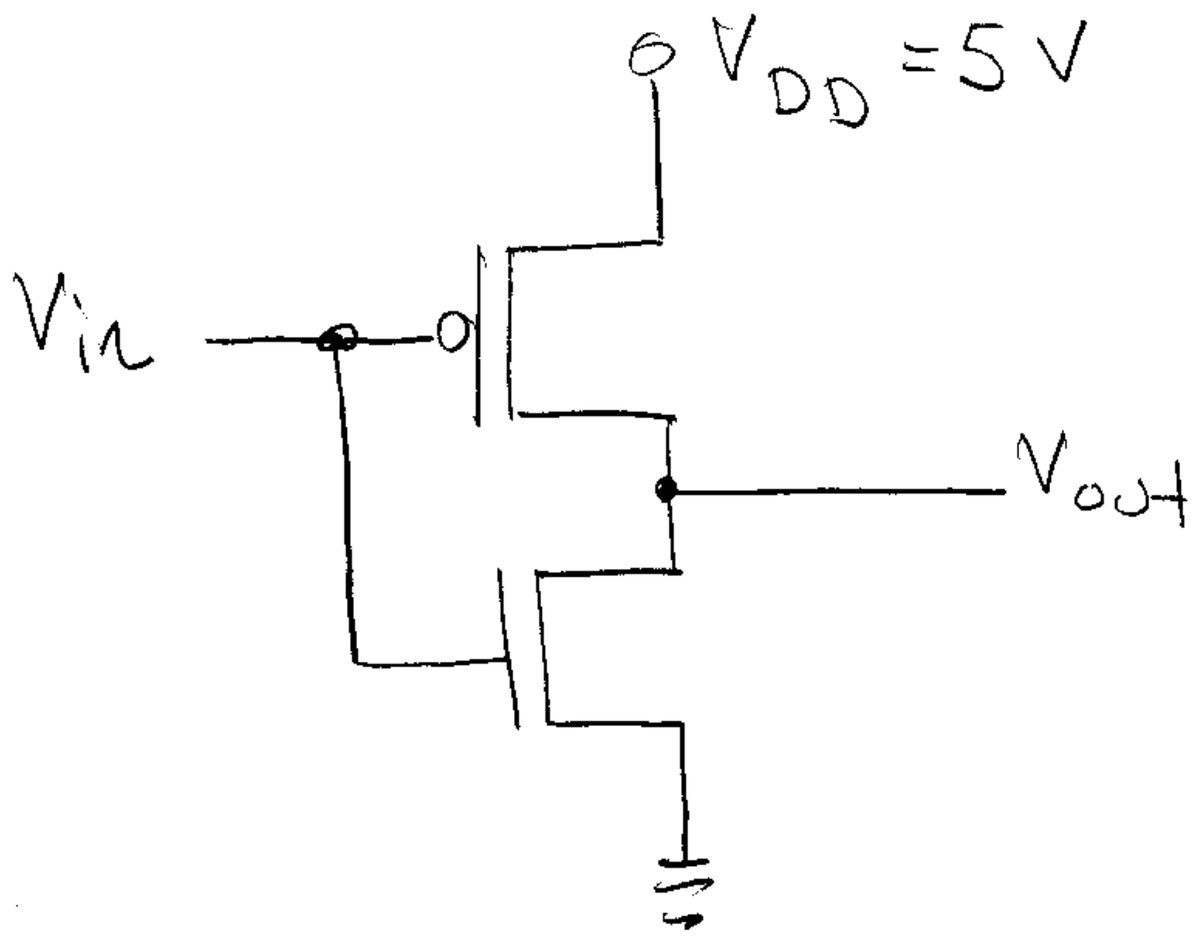
3) Guess the mode of transistor B and write the I_{D_B} vs V_{DS_B} equation.

4) Rewrite the I_{D_B} vs V_{DS_B} equation in terms of I_{D_A} & V_{DS_A} using 1).

5) Solve the two transistor equations to get I_{D_A} & V_{DS_A}.

If the answer conflicts with the assumed transistor modes, go back to 2).

For the CMOS inverter below, find V_{out} for an input $V_{in} = 1.2$ V. (10)



NMOS:

$\lambda = 0$

$V_T = 1$

$I_{D_{SAT}} = 10^{-4}$ A

PMOS:

$\lambda = 0$

$V_T = -1$

$I_{D_{SAT}} = -10^{-4}$ A