Measurement and Characterization of Multilayered Interconnect Capacitance for Deep-Submicron VLSI Technology

Jae-Kyung Wee, Young June Park, *Member, IEEE*, Hong Shick Min, Dae-Hyung Cho, *Member, IEEE*, Man-Ho Seung, and Hun-Sup Park

***Abstract*—This paper presents the measurement and characterization of multilayered interconnect capacitances for a 0.35-μm CMOS logic technology, which become a critical circuit limitation to high performance VLSI design. To measure multilayered capacitances of nonstacked, stacked, and orthogonally crossing interconnect lines, new test structures and measurement method are presented. The measured interconnect capacitances were employed to evaluate and calibrate TCAD tools for the simulation of high-speed interconnect technologies. This study shows that the calibration method considerably improves the accuracy of simulation results compared with measured results.**

I. Introduction

As CIRCUIT density steadily increases in advanced logic and memory chips, and as transistor performance improves with each new chip generation, multilayered interconnect plays an important role in the performance and density of today's VLSI circuits [1]–[4]. With the advent of global planarization processes such as chemical and mechanical polishing (CMP), reactive-ion-etched (RIE) aluminum-alloy lines, and fully plugged via contacts, more levels of insulators and interconnects can be realized. For logic chips and microprocessors, four or five levels of interconnect provides considerable advantage in speeds and die size reductions. However, the interconnect scaling gives rise to unanticipated signal integrity problems such as delay and unmatched signal timing, which becomes especially worse due to increase of the coupling capacitances in the parallel running lines and orthogonally crossing lines. Moreover, the chip area occupied by interconnects as well as the average length of the global interconnect continue to increase, and the chip performance is mainly restricted by the RC delay and the IR drop in the interconnect lines. Under this environment, accurate measurement and characterization of the multilayered interconnect are strongly required for a successful design of the chip.

Manuscript received August 29, 1997; revised April 16, 1998. This work was supported by Hyundai Electronics Company.

J.-K. Wee, Y. J. Park, and H. S. Min are with the School of Electrical Engineering and the Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-742, Korea (e-mail: wjk@mangchi.snu.ac.kr).

D.-H. Cho was with TCAD and Device, System IC Research Lab, Hyundai Electronics, Co., Ltd, Kyungki-do, Korea. He is now with the Intel Corporation, Santa Clara, CA 95052–8119 USA (e-mail: dcho1@td2cad.intel.com).

M.-H. Seung and H.-S. Park are with TCAD and Device, System IC Research Lab, Hyundai Electronics, Co., Ltd, Kyungki-do, Korea (e-mail: seung@sysic.hyundai.co.kr).

Publisher Item Identifier S 0894-6507(98)08368-7.

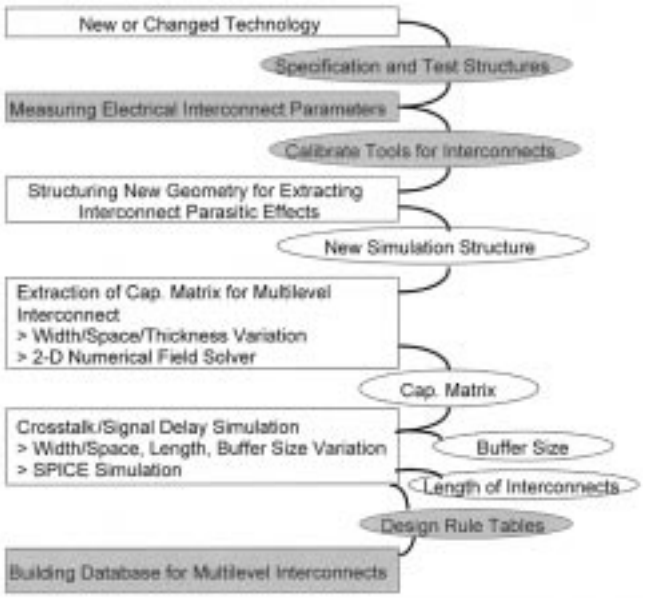
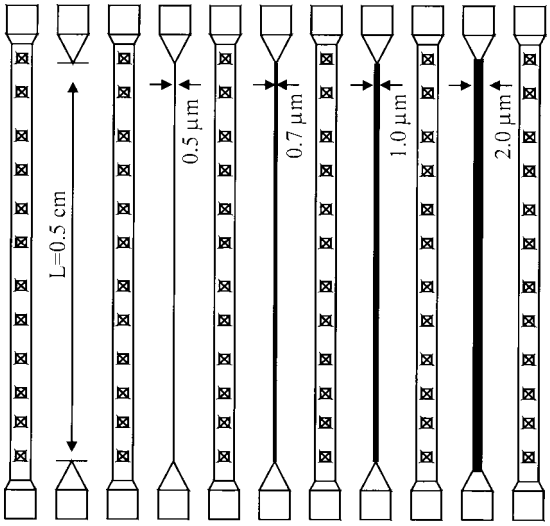


Fig. 1. The flow of characterization, modeling, and simulation for the multilayered interconnects of 0.35-μm CMOS logic technology.

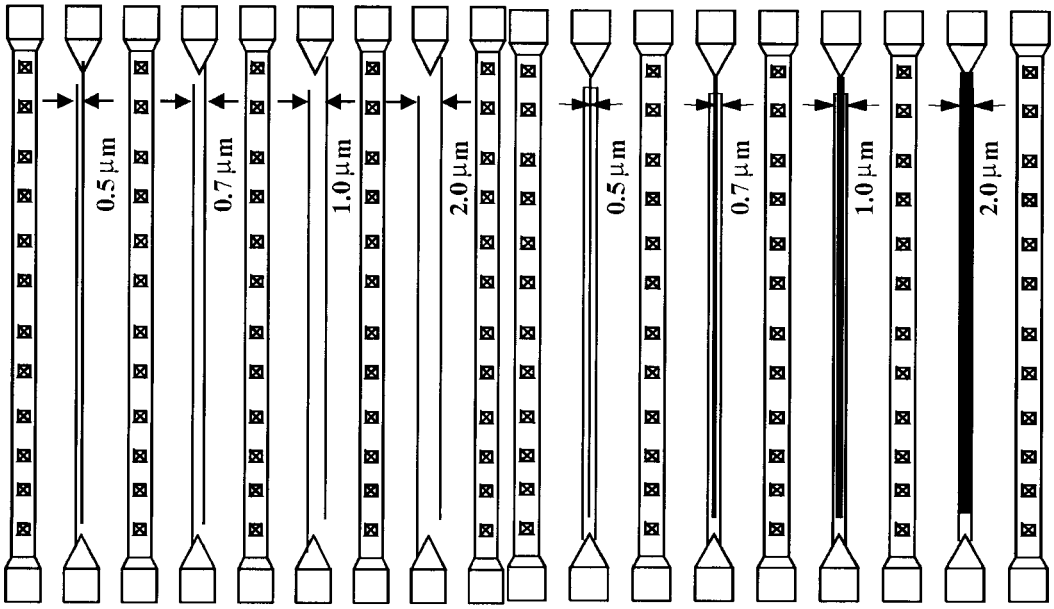
The objectives can be achieved by combining modeling, simulation, and measurement into standard VLSI design methodology as shown in Fig. 1. We have developed a systematic approach that consists of

1) determination of a interconnect library including test structures, extracting interconnect parasitics;
2) electrical measurement and extraction of interconnect parasitics;
3) dimensional measurements of the interconnects and insulator layers using SEM *et al.*;
4) calibration of the inputs of field solvers (or tools) based on measurements;
5) extraction of the interconnect parasitics of the structures which do not exist in the test patterns using the calibrated CAD tools;
6) evaluation of the calibrated CAD tools through comparison with the circuit simulation and the on-chip measurement for circuit performances including crosstalks and delays [5];

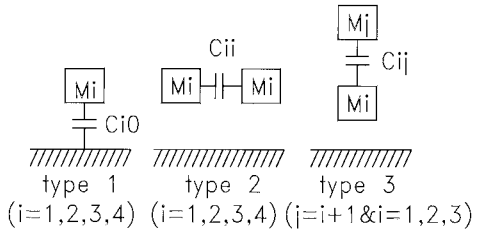
0894–6507/98$10.00 © 1998 IEEE



(a)



(b)



(c)

Fig. 2. Schematics of nonstacked multilayered interconnect test structure for the measurement of self and intralayer/interlayer coupling capacitances: (a) top view of deembedding open pad and single line metal lines for self-capacitance measurement, (b) top view of coupled metal lines for intralayer coupling and interlayer coupling capacitance measurement, and (c) schematics of the cross section of the above test patterns (a) and (b) for nonstacked multilayered interconnect test structure.

7) determination of the optimal interconnect design rules;
8) building the database of the electrical properties for all the possible interconnect structures using the calibrated CAD tools and the interpolations for parameterization.

In this paper, we will report the results of our study for the above steps from 1)–4) and 8) (denoted by the shade area in Fig. 1). For steps 1)–4), new test structures with three major types of stacked, nonstacked, and orthogonally

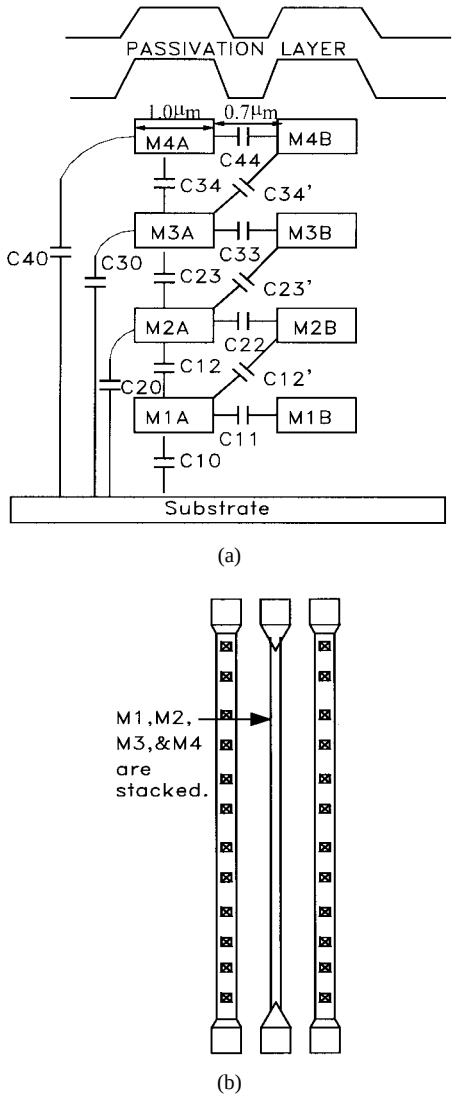


Fig. 3. Schematics of parasitic capacitances in stacked multilayered interconnects structure: (a) cross-sectional view and parasitic capacitances and (b) top view.

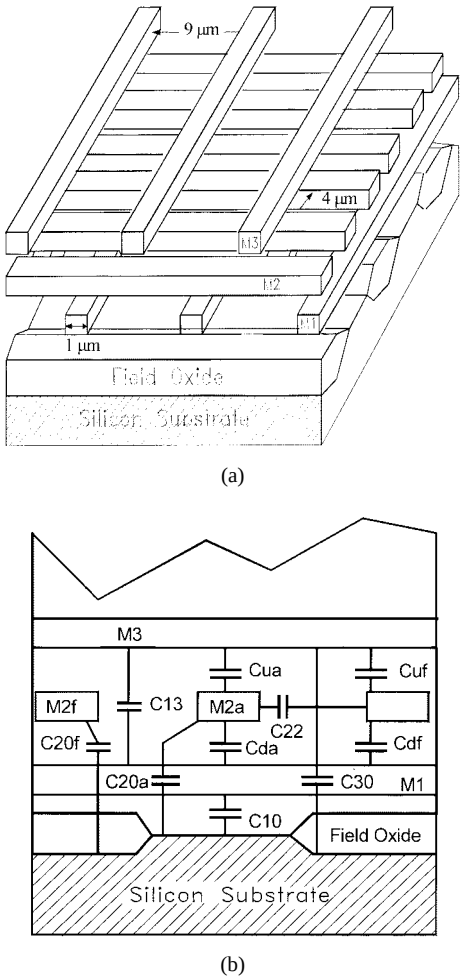


Fig. 4. A test pattern for measurement and simulation of an orthogonally crossing multilayered interconnect capacitances. Within a pattern having a 0.1×0.1 cm^2 size, total length of each interconnects and total number of crossing between a line and other line in a different layer are 10 cm and 10 000, respectively. All the line widths are fixed to 1 μm: (a) a schematic of 3-D simulation domain (30×30 μm^2 size), and (b) cross section and its coupling capacitances. Subscripts, "a" and "f," in capacitances such as Cd"a(f)," Cu"a(f)," and $C20$"a(f)," *et al.* represented lines on the active region and field region, respectively.

crossing multilayered interconnect will be presented, which have been fabricated using an advanced 0.35-μm CMOS logic technology. After the measurement and calculation method are described based on the test structure, the measured multilayered interconnect capacitances are compared to the two-dimensional (2-D) and three-dimensional (3-D) field solver [6], which is central to the characterization and modeling of the multilayered interconnect technology. In this work, the physical geometry data based on SEM photography have been dominantly used for calibrating the simulation tools according to the measurements. The final goal of this work (step 8) aims at building the database as a look-up table of multilayered interconnect capacitances and providing a new optimal interconnect design for high performance VLSI circuits.

II. Test Patterns and Tool Calibrations

First, test structures including nonstacked, stacked, and orthogonally crossing multilayered interconnects were fabricated and measured. The top view and their cross-sectional view of the nonstacked multilayered interconnect structure are shown in Fig. 2. This test structure has three types which are called single, intralayer coupled (between two interconnects of the same layer metal), and interlayer coupled (between two interconnects of different metal layers) interconnects, as shown in Fig. 2(c). In the layout, ground metal line and signal metal line are alternatively placed to shield the electrical flux between interconnect lines. Although widths of the signal interconnect lines are changed, widths of ground lines are fixed to 20 μm. The stacked multilayered interconnect test structure has a similar layout compared with the nonstacked multilayered interconnect structures. The cross-sectional and top view of the stacked multilayered interconnect structure are shown in Fig. 3. As shown in Fig. 3(a), metal lines of all layers are stacked in parallel. Assuming that the field interactions between the nearest interconnects and interconnects in the adjacent layers are important, only fourteen major capacitances are considered and other minor capacitances are

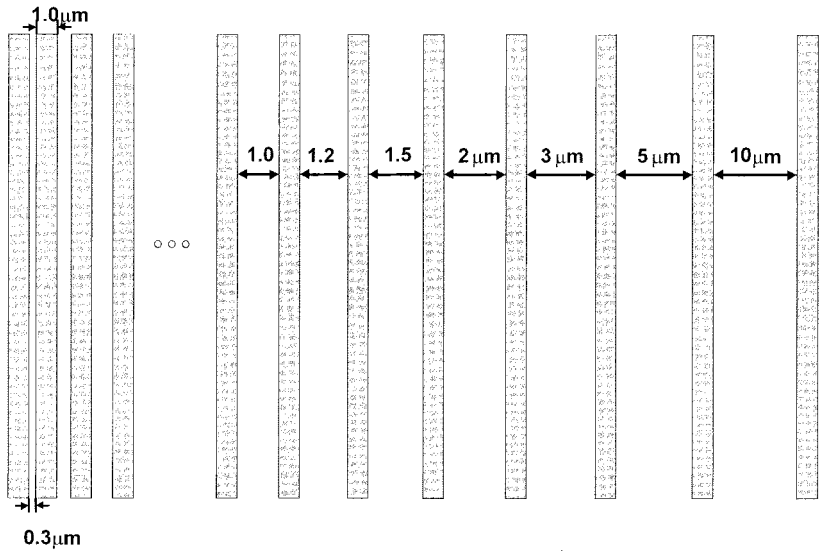


Fig. 5. Schematics of SEM-based calibration patterns using the spectrum types in multilayered metal.

ignored. A schematic of an orthogonally crossing multilayered interconnect pattern is shown in Fig. 4(a), where the specially devised PAD deembedded patterns are not shown. The comb type of metal 2 lines (M2) is devised in such a way that M2 lines (with the width of 1 μm) are alternately arrayed on field and active regions with the space of 4 μm. Metal 1 (M1) and metal 3 (M3) lines then cross the M2 lines. And the line widths are fixed to 1 μm. The self and coupling capacitances of this pattern are shown in Fig. 4(b), assuming that only the three-dimensional fringing field interactions between the nearest lines (in the same metal layer) and next adjacent interconnects are important as reported in [7].

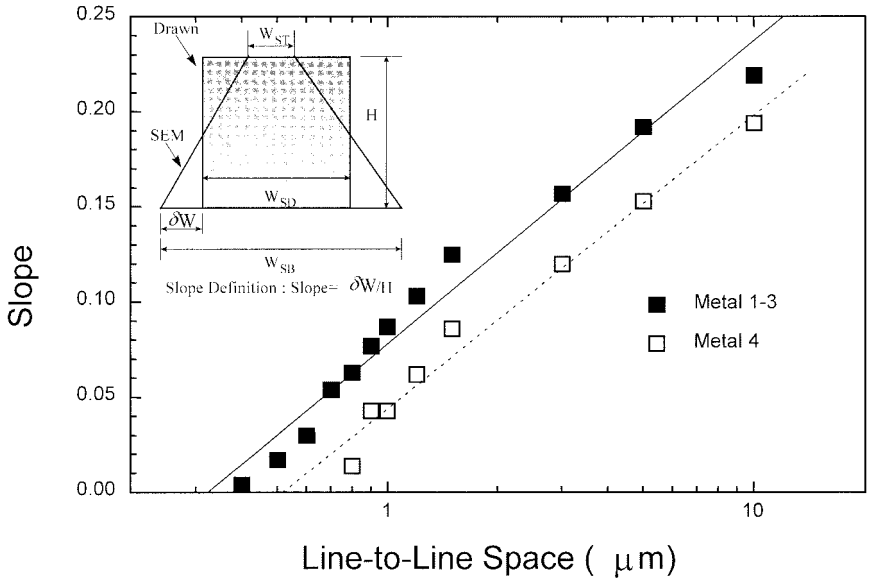
Second, for accurate determination of multilayered interconnect parasitics, we investigated the final geometry deviated from the baseline process recipes using the SEM photography. To demonstrate the dependence of the micro-loading effect on the drawn size of the line-to-line space, test structures for a variety of spectrum type patterns (both on a single layer and on multiple layers) are designed as shown in Fig. 5. In the spectrum type pattern, the drawn widths and lengths of metal lines were fixed at 1 μm and 0.5 cm, respectively, whereas the space between lines was varied from 0.3 to 10 μm. Fig. 6(a) shows the relation of the line-to-line space and the slope, which is defined as the ratio of one-side bottom width variation (δW in the figure) to the line thickness (H in the figure). Variation of the bottom width of metal lines comes from the micro-loading effect in the dry etching process. The slopes of metal 1 (M1) to metal 4 (M4) versus the line-to-line space are well fitted to the linear lines up to the space of 10 μm. But, we can not find a difference in slopes between the metal line in a single layer and the metal line in multiple layers. Table I shows that the thickness of interlayer metal dielectrics (IMD's) and metal lines also changes from baseline process recipes, due to the proximity effect and the process variation. The materials used in IMD layers have different dielectric constants, which have been measured using other test patterns. As shown in Fig. 6(b), the voids in IMD layers cause the change in the intralayer coupling capacitances as well as the reliability problem such as electromigration. However, the voids are not considered in this paper since the occurrence of voids is random and they should be removed.

Finally, the dielectric constants of IMD's were obtained from capacitance measurement using the 800 μm-squared parallel-plate capacitors. The sites were cross-sectioned and the IMD thickness was measured by SEM photography. The relative dielectric constants of the stacked IMD's from IMD1 to IMD4 are calculated to be 4.0, 3.9, 4.0, and 4.0, respectively. We assume that all the dielectric constants are single-valued scalar (isotropic and homogeneous).

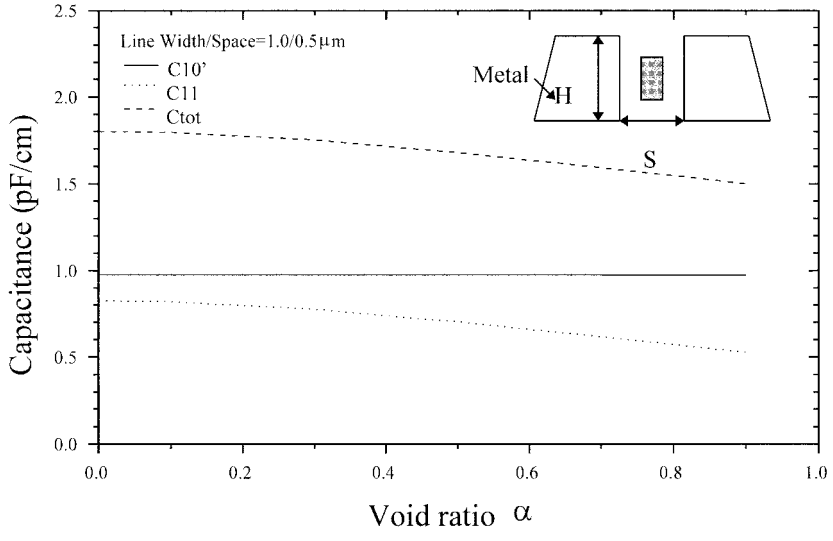
III. Nonstacked Multilayered Interconnect Test Structure

The single and coupled line test structures were used to measure the self ($C_{i0},\ i = 1, 2, 3,$ and 4) and intralayer ($C_{ii},\ i = 1, 2, 3,$ and 4)/interlayer ($C_{ij},\ i = 1, 2,$ and 3 and $j = i + 1$) coupling capacitances as the metal line width and line-to-line metal space vary. PAD deembedded structures, which are short pads and open pads, are also used for deembedding the parasitics of the pads. The interconnect line capacitances of the test structure were measured using HP 4284 (LCR meter) which operates at 80 kHz. The details of the measurement method and the measured results are shown in Table II and Fig. 7, respectively. In Fig. 7, the measured capacitances are compared with the Raphael simulations with two input structures; SEM calibrated structure denoted by "after calibration" and the one based on the baseline process recipe denoted by "before calibration."

As shown in Fig. 7, the simulation results based on the baseline process recipe are different from the measurements. This is caused from the process variation such as thickness, dielectric constant, and void formation of IMD as well as the micro-loading effect and these factors should be modeled and calibrated. While the simulation results of the self-capacitances ($C_{i0},\ i = 1, 2, 3,$ and 4) shown in Fig. 7(a) precisely match (under 3.5% error) with the measurement after the input are



(a)



(b)

Fig. 6. The geometric changes due to process variation: (a) the slope variation versus line-to-line space for multiple stacked metal lines and (b) effect of void in IMD layer on various capacitances versus void ratio [void area (shade box) over total side area ($H \times S$)].

calibrated, the simulation results of intralayer coupling capacitances in Fig. 7(b) show some errors even after calibration. Especially, the errors between measurements and simulations after calibration for the patterns with the line-to-line space under 1 μm are speculated to occur due to the change in relative dielectric constants. This is caused by voids formed randomly in IMD layer. SEM photos show that the voids are frequently formed in the patterns with the line-to-line space less than 1 μm. In addition to voids, there is a possibility that the real dielectric constants are not exactly modeled because we extracted the dielectric constants from planar patterns in place of the test patterns. Works are currently in progress to model other effects such as the void in IMD and nonhomogeneous and isotropic dielectric constants in the real multistacked IMD's.

Especially, as shown in Fig. 7(c), larger error is found between the measurement and the simulation because of the variation of IMD thickness determined by CMP process and the misalignment between different layers than the error in the self- and inter-coupling capacitances which are dominantly

TABLE I
THE THICKNESS OF IMD AND METAL LAYERS, THE TARGET BASED ON BASELINE RECIPE AND MEASUREMENT FROM SEM PHOTOGRAPHY

Materials	Thickness (Å) Baseline Recipe / SEM calibrated
IMO	10000/8700
Metal 1	5600/6410
IMD1	13000/12360
Metal 2	6600/7280
IMD2	13000/11600
Metal 3	6600/7630
IMD3	14000/12970
Metal 4	8800/9490
Oxide	3000/2430
Nitride	5000/4610

TABLE II
THE MEASUREMENT METHOD FOR THE SELF AND INTRALAYER COUPLING CAPACITANCES OF NONSTACKED MULTILAYERED INTERCONNECT TEST STRUCTURE

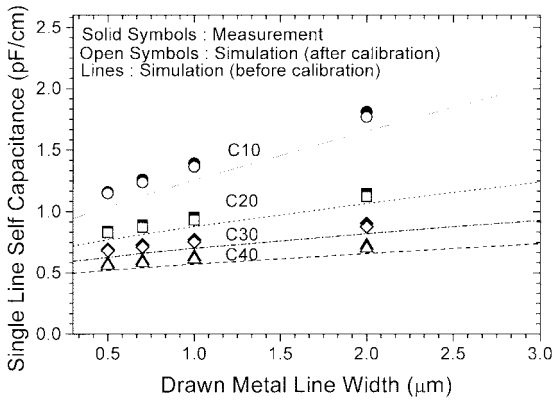
Cap. Symbols	Cross-sectional view and capacitance calculation	Schematics of top view
CpadA	One PAD capacitance for de-embedding.	CpadA
CpadAB	Two PAD capacitance for de-embedding.	CpadAB
Ci0 (i=1,2,3,4)	Mi, Ci0 C10 = preC10 - CpadA	M1, M1 preC10
Cii Ci0' (i=1,2,3,4)	Cii, Mi, Mi, Ci0' Ca=2Ci0', Cb=Cii+Ci0' Ca = preCa - CapdAB Cb = preCb - CpadA Ci0' = 1/2Ca Cii = Cb - 1/2Ca	M1, M1 preCa M1, M1 preCb
Cj0" Ci0" Cij (i=1,2,3,4 j=i+1 for j ≠5)	Ca=Cj0"+Ci0" Cb=Cj0"+Cij Cc=Cij+Ci0" Ca = preCa - CpadAB Cb = preCb - CpadA Cc = preCc - CpadA Cj0"=1/2(Ca+Cb-Cc) Cij =1/2(-Ca+Cb+Cc) Ci0"=1/2(Ca-Cb+Cc) Mi, Cij, Cj0", Mi, Ci0''	M1, M1 preCa M1, M1 preCb M1, M1 preCc

determined by line width variations. However, the errors after calibration reduce to the range from 30 to 45% to 2 to 20%. Fig. 8 shows the self (C_{self}) and total (C_{tot}) capacitances of the first metal line in nonstacked multilayered interconnect test patterns. In case of the total capacitance of a interlayer coupled line, the error of the simulation results based on baseline process recipe is relatively large compared with that of self-capacitance. The above results (Figs. 7 and 8) show the importance of calibration of IMD thickness and misalignment as well as line width variations and the statistical data for the process variation should be prepared for an accurate characterization and modeling of multilayered interconnect technology.

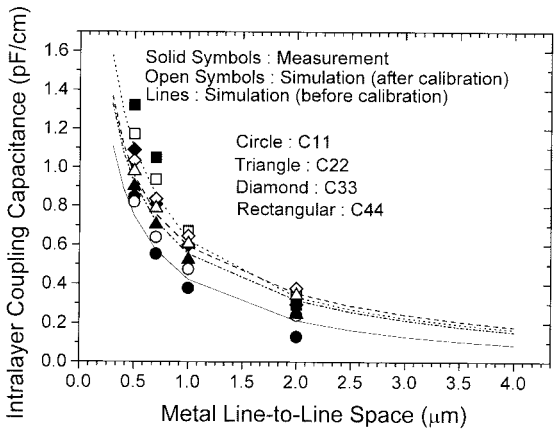
IV. STACKED MULTILAYERED INTERCONNECT TEST STRUCTURE

This section describes the experimental measurement method of parasitic capacitances of the stacked multilayered interconnect. The detail description of the measurement method and the measured results are shown in Table III and Fig. 9, respectively. In the measurement, the substrate is grounded and the followings are assumed:

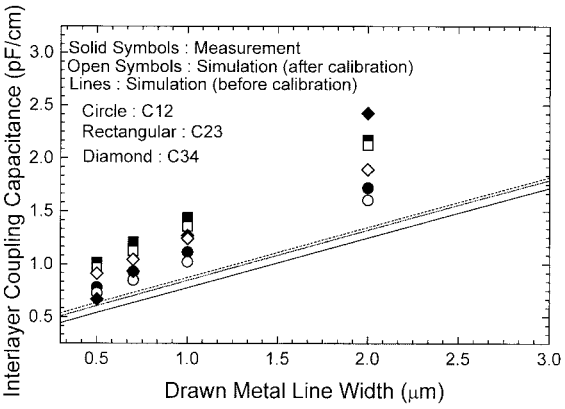
1) no capacitances exist between the equipotential electrodes;
2) the fringe capacitances always exist between the signal electrode and the substrate;
3) the capacitances between the neighboring electrodes are dominant;
4) the parallel metal lines are symmetrical.



(a)



(b)



(c)

Fig. 7. Comparison of measurement and simulation of nonstacked multilayered interconnect test structure shown in Fig. 2: (a) self-capacitance of single lines, (b) coupling capacitance of intralayer lines, and (c) coupling capacitance of interlayer lines.

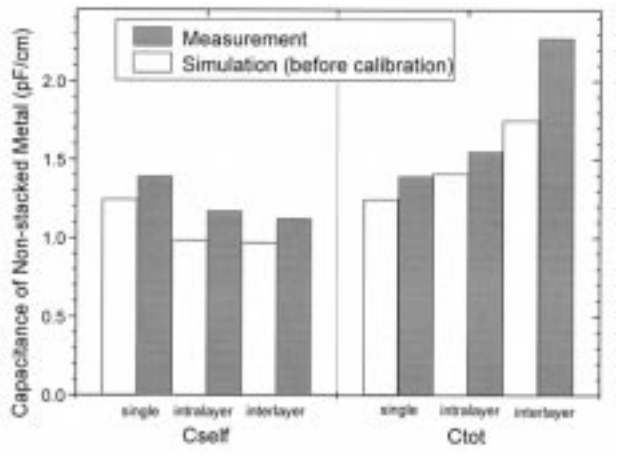


Fig. 8. Comparison between the measurement and simulation of self and total capacitances of nonstacked multilayered interconnects. Width of all the lines is 1 μm and line-to-line space for intralayer coupled metal line is 1 μm. Total capacitances (C_{tot}) of intralayer and interlayer coupled lines are defined as $C10' + C11$ and $C10'' + C12$, respectively.

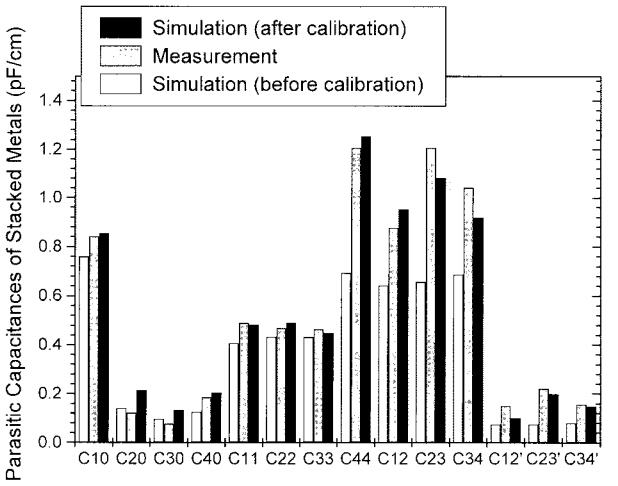


Fig. 9. Comparison between the measurement and the simulation of parasitic capacitances defined in Fig. 3(a).

Then, as described in Table III, the measurement and the calculation of all the parasitic capacitances are straightforward and PAD deembedding method is the same with that of nonstacked multilayered interconnects. Using the methods described in Table III, the measured capacitances were also compared to Raphael simulation. The measured results are the statistical-average values considering the wafer-to-wafer and run-to-run process variations. In the measurement, all data are consistently measured within the resolution of 0.01 pF for all wafers.

Fig. 9 shows the measured capacitance components in Fig. 3(a) and exhibits the importance of the input calibration where the shade bars are the measurement and the dark bars are the calibrated Raphael simulation based on SEM photograph. Without the SEM based calibration, the maximum error of 50% is found which comes from metal shape changes by the micro-loading effect, thickness variations of IMD's and metal lines, and the misalignment of the stacked multilayered interconnects. The errors between the measurement and simulation after calibration are reduced within 11% (except for $C12$, $C20$, and $C30$). However, slight discrepancies (especially, $C20$ and $C30$) between the measurement and the simulation after calibration are found since our extraction method is based on assumption that the structures are symmetric (no misalignment exists between metal layers). Even though slight errors can be produced by the calibration based on SEM photograph, accurate results

TABLE III
MEASURED METHOD FOR THE STACKED METAL STRUCTURES OF FIG. 3(a). OTHER ELECTRODES ARE ALL GROUNDED EXCEPT SIGNAL ELECTRODES FOR EACH MEASUREMENT. THE DIAGONALLY-CROSSED CAPACITANCES ARE NOT COMPLETELY DISPLAYED IN SCHEMATICS FOR SIMPLICITY BUT CONSIDERED IN CAPACITANCE EXTRACTION

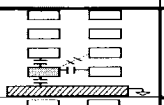
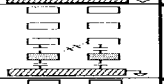
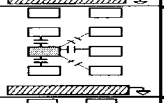
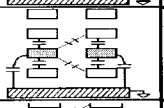
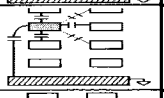
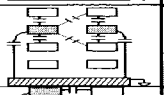
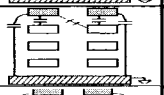
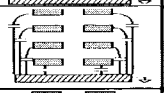
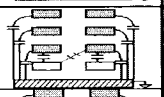
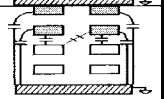
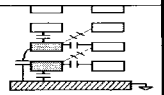
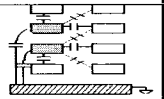
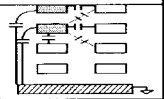
Measurement	Signal ( ) ground ( )	schematics	Calculation
C_1=C10+C11 +C12'+C12	M1A		C10= 1/4(C_2+C_9-C_10)
C_2 2(C10+C12 +C12')	M1A, M1B		C20= 1/4(-C_2+C_4+C_9 -C_11)
C_3=C20+C12 +C12'+C23 +C23'+C22	M2A		C30= 1/4(-C_4+C_6-C_8 +C_10)
C_4=2(C20+C12 +C12'+C23 +C23')	M2A, M2B		C40= 1/4(-C_6+C_8 +C_11)
C_5 C30+C23 +C23'+C34 +C34'+C33	M3A		C11= -1/2C_2+C_1
C_6 2(C30+C23 +C23'+C34 +C34')	M3A, M3B		C22= -1/2C_4+C_3
C_7=C40+C34 +C34'+C44	M4A		C33= -1/2C_6+C_5
C_8=2(C40+C34 +C34')	M4A, M4B		C44= -1/2C_8+C_7
C_9=2(C10+C20 +C30+C40)	All except substrate		C12= 1/4(C_2-C_9+C_10) -1/2(C_1+C_3-C_12)
C_10=2(C12 +C12'+C20 +C30+C40)	All except M1A, M1B		C12'= 1/2(C_1+C_3-C_12)
C_11=2(C23 +C23'+C30 +C40)	All except M1A, M1B, M2A,M2B		C23= 1/4(C_4 -C_10+C_11) -1/2(C_3+C_5-C_13)
C_12=C10+C11 +C12+C12' +C20+C22 +C23+C23'	M1A, M2A		C23'= 1/2(C_3+C_5-C_13)
C_13=C20+C22 +C12+C12' +C30+C33 +C23+C23' +C34+C34'	M2A, M3A		C34= 1/4(C_6+C_8-C_11) -1/2(C_3+C_5-C_13)
C_14=C30+C33 +C23+C23' +C40+C44 +C34+C34'	M3A, M4A		C34'= 1/2(C_5+C_7-C_14)

TABLE IV
MEASUREMENT AND EXTRACTION METHODS OF THE ORGONALLY CROSSING MULTILAYERED INTERCONNECT CAPACITANCES. THE SUBSCRIPTS REPRESENTED AS "a" AND "f" IN CAPACITANCES (i.e., CUA *et al.*) ARE FOR THE LINES ON THE ACTIVE AND FIELD REGION, RESPECTIVELY

Signal electrodes	Measurement	Cap.	Calculation
M1	C_1=2C13+Cda+Cdf+C10	Cuf	1/2(C_2 + C_4 - C_9)
M2f	C_2=Cuf+Cdf+2C22+C20f	Cua	1/2(C_3 + C_4 - C_8)
M2a	C_3=Cda+Cua+2C22+C20a	Cdf	1/2(C_1 + C_2 - C_6)
M3	C_4=Cua+C13+C30+Cuf	Cda	1/2(C_1 + C_3 - C_5)
M1,M2a	C_5=2C22+2C13+Cdf+C10+C20a+Cua	C10	1/2(C_5 + C_6 + C_10 - C_1 - C_2 - C_3 - C_4)
M1,M2f	C_6=2C22+Cda+C10+C20f+2C13+Cuf	C20f	1/2(C_6 + C_7 + C_9 - C_1 - C_2 - C_3 - C_4)
M2a,M2f	C_7=Cda+Cdf+Cua+C20f+C20a+Cuf	C20a	1/2(C_5 + C_7 + C_8 - C_1 - C_2 - C_3 - C_4)
M2a,M3	C_8=2C22+Cda+C20a+C30+2C13+Cuf	C30	1/2(C_8 + C_9 + C_10 - C_1 - C_2 - C_3 - C_4)
M2f,M3	C_9=2C22+Cdf+C20f+C30+2C13+Cua	2C13	1/2(C_1 + C_4 - C_10)
M1, M3	C_10=C10+Cda+Cdf+Cua+Cuf+C30	2C22	1/2(C_2 + C_3 - C_7)

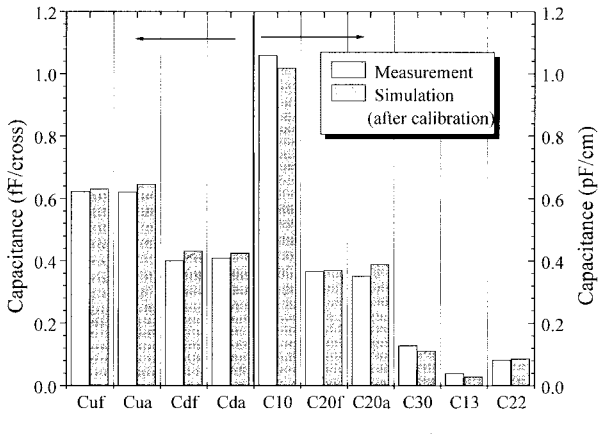


Fig. 10. Comparison between the measured and simulated capacitances per unit length and a crossing.

have been obtained by these calibrations which show the reliability of the proposed measurement method.

V. ORTHOGONALLY CROSSING MULTILAYERED INTERCONNECT TEST STRUCTURE

The crossovers among different metal layers frequently occur in a global interconnect according to the statistics in high-performance chips [7]. In this section we apply our calibration and measurement methods (introduce in Section IV) to the characterization of the crossover capacitances. The specially devised PAD de-embedding patterns are applied to removing the PAD parasitic capacitances. Then, the measurement and the calculation of all the parasitic capacitances are straightforward as described in Table IV. Measured and 3-D simulated results are illustrated in Fig. 10 for the self- and intra-coupling capacitances per unit length and the crossover capacitance per crossing. The input of CAD tool has been calibrated from the measured thickness of IMD's and metal layers based on SEM photography, but the changes of metal line shapes have not been considered because of CPU calculation limits. The errors between the measurement and simulation after calibration are within 13%.

In Fig. 10, we can find that first, the capacitances (self and crossover capacitances) of interconnects on active regions (C_{ua}, C_{da}, *et al.*) are not much different (1–3%) from those on field regions (C_{uf}, C_{df}, *et al.*), which means that stacked layers have been uniformly planarized by the CMP process. Second, the self-capacitances of the interconnect lines in Fig. 4(b) are smaller than those in single line patterns [Fig. 2(a)]. Especially, the decrease of self-capacitances is significant in the upper metal layers (such as $C20a$, $C20f$, and $C30$). Thirdly, the crossover capacitance is in the range of 0.4–0.62 fF per crossing, which is not negligible. And the capacitance between M1 and M3 is negligible in the real structures since M2 crossing between M1 and M3 shields the electrical field between M1 and M3. Although the self capacitance (0.35–0.37 pF/cm) of M2 line in Fig. 4(b) is smaller than that ($\sim$0.84 pF/cm) of M2 line in single line patterns, the total capacitance of M2 line in Fig. 4(b) is larger (1.3–1.4 pF/cm) if crossing capacitances are included.

The slight difference between the measurements and the calibrated 3-D Raphael simulations in the figure can be further reduced, if the misalignment (between metal lines in the different layers), the processed shape of the interconnects, and the change of dielectric constants due to void formation are included.

VI. CONCLUSION

We designed new test structures and presented the measurement method of the 2-D [8] and 3-D interconnect structures, which enables us to make the accurate measurement of multilayered interconnect capacitances. The calibration based on SEM photograph was performed and compared to the measurement results. The improved accuracy from the SEM calibration demonstrates not only the importance of the calibration but also the accuracy of the proposed measurement method. Thereby the final goal of this work is to build the database for multilayered interconnect capacitances of a 0.35-μm CMOS logic technology, which is indispensable for high-speed and high-performance VLSI circuit design.

ACKNOWLEDGMENT

The authors would like to thank Y. J. Chun, D. J. Lee, D. S. Jung, and H. S. Yoon of Memory Research Center of Hyundai Electronics Company for their technical supports.

REFERENCES

[1] H. B. Bakoglu, *Circuits, Interconnects, and Packaging for VLSI.* Reading, MA: Addison-Wesley, 1990.

[2] K. Rahmat, O. S. Nakagawa, S. Y. Oh, and J. Moll, "A scaling scheme for interconnect in deep-submicron processes," in *IEDM Tech. Dig.*, 1995, pp. 245–248.

[3] H. You and M. Soma, "Crosstalk analysis of interconnect lines and packages," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 1019–1026, Aug. 1990.

[4] S. Y. Oh and K. J. Chang, "2001 needs for multi-level interconnect technology," *Circuits Devices Mag.*, Jan. 1995.

[5] D. H. Cho, Y. S. Eo, M. H. Seung, N. H. Kim, J. K. Wee, O. K. Kwon, and H. S. Park, "Interconnect capacitance, crosstalk, and signal delay for 0.35-μm CMOS technology," in *IEDM Tech. Dig.*, 1996, pp. 619–622.

[6] *Raphael User's Manual*, Technology Modeling Associates, Inc., 1994.

[7] S. Y. Oh, K. Okasaki, J. Moll, O. S. Nakagaw, K. Rahmat, and N. Chang, "3D GIPER: Global interconnect parameter extractor for full-chip global critical path analysis," in *IEDM Tech. Dig.*, 1996, pp. 615–618.

[8] D. H. Cho, M. H. Seung, N. H. Kim, H. S. Park, J. K. Wee, Y. J. Park, and H. S. Min, "Measurement and characterization of multi-layered interconnect capacitance for deep submicron VLSI technology," in *Proc. IEEE ICMTS 1997*, pp. 91–94.

Jae-Kyung Wee was born in Seoul, Korea, on August 1, 1966. He received the B.S. degree in physics from Yonsei University, Seoul, in 1988, and the M.S. degree from Seoul National University, in 1990. Since August 1993, he has been working toward the Ph.D. degree in electronics engineering on modeling and characterization of interconnects for high-speed and high-density circuits at Seoul National University.

In 1990, he joined Hyundai Electronic Company, Kyungki-do, Korea, as a Process Engineer for 16MDRAM and LOGIC devices. His research interest is in the area of interconnect modeling and characterization for high-density and high-speed circuits and process developing.

Young June Park (S'77–M'83) received the B.S. degree in 1975 and the M.S. degree in 1977, both from Seoul National University. After developing Monte Carlo techniques for BJT and MOS structure simulations, he received the Ph.D. degree from the University of Massachusettes, Amherst, in 1983.

From 1983 to 1985, he worked for the Device Physics and Technology Department at IBM, East Fishkill, NY. In 1985, he joined Gold Star Semiconductor Company (currently, LG Semicon Company) to work in the area of the CMOS technology. In 1988, he joined Seoul National University, where he is currently a Professor. In 1993, he spent his sabbatical year at Stanford University, Stanford, CA, and performed research on advance semiconductor transport model. He was Director of the Inter-university Semiconductor Research Center (ISRC) at Seoul National University from 1995 to 1997. His areas of interest are the advanced device structures, device/noise and reliability modeling, and high speed circuit technology.

Hong Shick Min received the B.S. degree in electronics engineering from Seoul National University, Seoul, Korea, in 1966, and the M.S. and Ph.D. degrees in electrical engineering from the University of Minnesota, Minneapolis, in 1969 and 1971, respectively.

During 1971 and 1972, he was a Postdoctoral Fellow at the University Minnesota. In 1973, he joined the Department of Electronics Engineering at Korea University, Seoul, as an Assistant Professor. Since 1976, he has been with Seoul National University, where he is currently a Professor in the School of Electrical Engineering. His main research interests include noise in semiconductors and semiconductor devices.

Dae-Hyung Cho (M'97) received the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign in 1995.

From 1983 to 1990, he was with Samsung Electronics Co., Korea, where he worked on the MOS and bipolar transistor modeling and circuit simulations. Until 1995, he was a Research Assistant at the Beckman Institute for Advanced Science and Technology, Urbana, IL. In 1995, he joined the system IC R&D of Hyundai Electronics Co., Kyungki-do, Korea and he managed the device characterization group. In 1997, he joined the TCAD division of Intel Corporation at Santa Clara, CA, where he is a Senior Staff Engineer. His research interests include experimental characterization of nonquasistatic effects in MOSFET's, fast transient ESD diode, and high-frequency effects of interconnects.

Man-Ho Seung was born in Kwang-Ju, Korea. He received the B.S. degree in physics from Chonnam University, Kwang-Ju, in 1995.

Since 1995, he has worked at Hyundai Electronics System IC R&D Laboratory, Kyungki-do, where he has performed interconnect characterization, simulation, and modeling.

Hun-Sup Park, photograph and biography not available at the time of publication.