Calculating IC Cost

Use the following information…

Costas

The 1997 Roadmap (see transistor cost)

<table>
<thead>
<tr>
<th>Year</th>
<th>Feature nm</th>
<th>Area mm²</th>
<th>Density cm⁻²</th>
<th>Cost µc/tr</th>
<th>technology</th>
<th>wafer size</th>
</tr>
</thead>
<tbody>
<tr>
<td>1997</td>
<td>250</td>
<td>300</td>
<td>3.7M</td>
<td>3000</td>
<td>248</td>
<td>200</td>
</tr>
<tr>
<td>1999</td>
<td>180</td>
<td>340</td>
<td>6.2M</td>
<td>1735</td>
<td>248</td>
<td>300</td>
</tr>
<tr>
<td>2001</td>
<td>150</td>
<td>385</td>
<td>10M</td>
<td>1000</td>
<td>193?</td>
<td>300</td>
</tr>
<tr>
<td>2003</td>
<td>130</td>
<td>430</td>
<td>18M</td>
<td>580</td>
<td>157?</td>
<td>300</td>
</tr>
<tr>
<td>2006</td>
<td>100</td>
<td>520</td>
<td>39M</td>
<td>255</td>
<td>14</td>
<td>450</td>
</tr>
<tr>
<td>2009</td>
<td>70</td>
<td>620</td>
<td>84M</td>
<td>110</td>
<td>14</td>
<td>450</td>
</tr>
<tr>
<td>2012</td>
<td>50</td>
<td>750</td>
<td>180M</td>
<td>50</td>
<td>14</td>
<td></td>
</tr>
</tbody>
</table>

Overall Production Efficiency up by ~20X (!) from 1997 to 2012.
Where will the Extra Productivity Come from?
(note that Yield plays a diminishing role)

The Basic Yield Model

Assume a constant defect density $D$
Assume that it takes one defect to kill a circuit.
Find the probability that a circuit will work, given $D$ and the area $A$ of a circuit.

\[ P\{\Delta A \text{ is } \text{"bad"}\} = D\Delta A \]
\[ A = n\Delta A \]
\[ Y = P\{A \text{ is } \text{"good"}\} = \prod_{1}^{n} (1 - D\Delta A) = (1 - D\Delta A)^n \]
\[ \ln (Y) = \frac{A}{\Delta A} \ln(1 - D\Delta A) \rightarrow D \text{ } A \text{ when } \Delta A \rightarrow 0 \]
\[ Y = e^{-D \cdot \Delta A} \]
Negative Binomial (a more popular model)

If \( f(D) \) follows a Gamma distribution, then:

\[
Y = \left[ 1 + \frac{AD}{\alpha} \right]^{-\alpha}
\]

\((\alpha \sim 0.3 - 3)\)

And if clustering becomes an issue, then:

\[
Y = Y_o \left[ 1 + \frac{AD}{\alpha} \right]^{-\alpha}
\]

where \( Y_o \) is the “gross cluster yield”.

Typical Defect Size Distribution

This means that defect density increases to about \(1/\text{square} \sim 1/\text{cube} \) of line width!
Historical data on what percentage of WAFERS makes it to the end. (not all the DIE on each wafer makes it. See next slide for this info...)
Memory Defect Density, 0.45-0.6µm

\[ Y = \left( \frac{1-e^{-AD}}{AD} \right)^2 \]

A is the area. D is the defect density (goes up to 1/cube−1/square of line width for a given cleanroom class). Numbers here are for class 10. See next slides for data points from older technologies...

Logic Defect Density, 0.7-0.9µm CMOS

\[ Y = \left( \frac{1-e^{-AD}}{AD} \right)^2 \]
Logic Defect Density, 0.7-0.9μm CMOS

\[ Y = \left( \frac{1-e^{-AD}}{AD} \right)^2 \]