### Spring 1999 EE290H Tentative Weekly Schedule

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<td>Functional Yield of ICs and DFM.</td>
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<td>Yield Learning and Equipment Utilization.</td>
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<td>Statistical Estimation and Hypothesis Testing.</td>
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<td>Analysis of Variance.</td>
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<td>Two-level factorials and Fractional factorial Experiments.</td>
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<td>Distribution of projects. (week 9)</td>
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<td>Run-to-run control.</td>
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<td>Real-time control.</td>
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**IC Yield & Performance**

- Process Modeling
- Process Control
- Metrology
- Manufacturing Enterprise

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### IC Yield and Performance (cont.)

- **Defect Limited Yield**
  - Definition and Importance
  - Metrology
  - Modeling and Simulation
  - Design Rules and Redundancy

- **Parametric Yield**
  - Parametric Variance and Profit
  - Metrology and Test Patterns
  - Modeling and Simulation
  - Worst Case Files and DFM

- **Equipment Utilization**
  - Definition and NTRS Goals
  - Measurement and Modeling
  - Industrial Data

- **General Yield Issues**
  - Yield Learning
  - Short loop methods and the promise of in-situ metrology
IC Structures can be highly Variable

Transistor

Interconnect

Variability will impact performance

What is Parametric Yield?

- When devices (transistors) do not have the exact size they were designed for,
- When interconnect (wiring) does not have the exact values (Ohms/µm, Farads/µm², etc.) that the designer expected,
- When various structures (diffused layers, contact holes and vias, etc.) are not exactly right,
- The circuit may work, but
- **Performance (speed, power consumption, gain, common mode rejection, etc.) will be subject to statistical behavior...**
What are the Parametric Yield Issues?

- Binning and Impact on Profitability
- The Process and Performance Domains
  - Characterizing the Process Domain
  - Identifying Critical Variables
  - Modeling Process Variability
  - Associated (Statistical) Metrology
- Process Variability and the Circuit Designer
- Design for Manufacturability Methods
- A Global (re)view of Yield

What is the Critical Dimension?

Gate is typically made out of Polysilicon
Basic CD Economics

Leading Edge CD Control Revenue Leverage:
\[ \sim \$7.5/\text{nm} \]

Application of Run-to-Run Control at Motorola

\[ \text{Dose}_n = \text{Dose}_{n-1} - \beta (\text{CD}_{n-1} - \text{CD}_{\text{target}}) \]
CD Improvement at Motorola

(CD - Target) Distributions

Pre etch

Before ACDC

σ_{eff} reduced by 60%

(D. Gerold et al, Sematech AEC/APC, Sept 97, Lake Tahoe, NV)

After ACDC

Post etch

Why was this Improvement Important?

Tighter lot CD distribution allowed target shift to shorter L_{eff} without yield hit

<table>
<thead>
<tr>
<th>Speed Bin</th>
<th>% Pre-ACDC</th>
<th>% Post-ACDC</th>
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<tr>
<td>1</td>
<td>1.6</td>
<td>0.0</td>
</tr>
<tr>
<td>2</td>
<td>8.8</td>
<td>0.0</td>
</tr>
<tr>
<td>3</td>
<td>39.6</td>
<td>3.1</td>
</tr>
<tr>
<td>4</td>
<td>44.2</td>
<td>91.1</td>
</tr>
<tr>
<td>5</td>
<td>5.6</td>
<td>5.8</td>
</tr>
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Mean ASP: $S$ $S$

$2M/\text{wk}/1K$ starts

600k APC investment, recovered in two days...
Process and Performance Domains

- CD is not the only process variable of interest...
- Speed is not the only performance of interest...
- In general we have a mapping between two multi-dimensional spaces:

So, what to do?

- What process parameters to measure?
- How to reduce Process Variability?

- What electrical parameters matter?
- How can we set reasonable specs on those?

- How to simulate performance variation?
- How to design a circuit that is immune to variation?

- What performance is important?
- What Process/Layout parameters can we change to satisfy critical performance specs?
Translating Specifications between Domains

- Performance Specs, imposed by the market, translate to an “acceptability region” in the process domain.
- This “acceptability region” is also known as the Yield Body (YB).
- The Yield Body can be mapped into either domain.

So what is Parametric Yield?

- One is keenly interested in mapping and in maximizing the overlap between YB and PS.
- This can be accomplished in various ways.
  - first, we should be able to measure (characterize) the Process Spread (PS).
  - then, one has to figure the mapping from Process to Performance!
  - Finally, one needs design tools to manipulate the above.
Parametric Test Patterns

Typically on scribe lanes or in "drop-in" test ICs.
E-test measurements:
- transistor parameters
- CDs
- Rs
- Rc
- small digital and analog blocks
- ring oscillators

Parametric Transistor Measurements
There is no agreement about Interconnect Parameters...

Interconnect Characterization Structures
Ring Oscillator for Interconnect Characterization

Interconnect Structures are very Complex...
Statistical Metrology for CDs

Where does variability come from?
What are its spatial components?

- Causal
- Equipment
- Recipe
- Spatial
- Within Die
- Among Die
- Among Wafers
- Random/Deterministic
- Response from Equipment A

Variability Sources can be identified

Test Pattern Placement

5 Linewidth Structures: 0.25-0.45µm in x and y
36 modules/field
24 fields/wafer

Short Loop Fabrication Sequence
Minimize confounded effects from fabrication.

Poly Deposition
Lithography
Coater Stepper Developer
Poly Etch
Data Collection

- Electrical Measurements facilitate data collection.
- Raw data contains confounded variability components from the entire “short loop” process sequence.

Variance can be Decomposed Spatially

\[ \text{cd} = p + f + w + e \]

Periodic:
- Deterministic Within Field
- Stepper (Optics)

Shot-to-shot:
- Deterministic Within Field
- Random Field to Field
- Stepper (Dose/Focus/Leveling)

Wafer:
- Deterministic Within Wafer
- CVD
- Coat
- Develop
- Etch

Error series:
- Random

Signal
- Causal
One can further decompose the influence of the Stepper Optics

Linearized Response:
\[ \Delta c_{d_p}(x,y) = A(x,y) + B(x,y) \Delta c_{\text{reticle}}(x,y) \]

Fixed Parameters:
- Resist/Develop system
- Resist/develop settings
- Nominal \( c_{d_{\text{reticle}}} \)
Decomposition Across Stepper Field

\[ \text{cd}_p(x,y) = A(x,y) + B(x,y) \Delta \text{cd}_\text{reticle}(x,y) \]

Decomposition to sub-step Variance Contributions
Information can be used for “Centering” Process

Response Surface

Mask Design

Desirable

Isolated

Side Line

5-line Grid

Mask “bias” used to achieve 0.35µm lines.

Statistical Metrology for Dielectrics

Rapid Characterization and Modeling of Pattern-Dependent Variation in Chemical-Mechanical Polishing
Brian E. Stine, Dennis O. Ouma, Member, IEEE, Rajesh R. Divecha, Member, IEEE, Duane S. Boning, Member, IEEE, James E. Chung, Member, IEEE, Dale L. Hetherington, Member, IEEE, C. Randy Harwood, O. Samuel Nakagawa, and Soo-Young Oh, Member, IEEE. IEEE TSM, VOL. 11, NO. 1, FEBRUARY 1998
Dielectric Thickness vs Position in Field

Studies like this can be used to complement “random” variability with the deterministic, pattern dependent variability. The combination of the two leads to simulation tools that can predict very well the “spread” of circuit performances.

Impact of Process Variability to Circuit Performance

- Obviously, not everything in the process impacts the Circuit Performance.
- Studies have tried to focus on the most important process parameters.
- CD is clearly one of them.
Impact of Pattern-Dependent Poly-CD Variation

Use basic Optical Model to determine “actual” pattern...


Simulated Performance Variability in 64x8 SRAM Macrocell
Circuit Sensitivity to Interconnect Variation

Fig. 1. Cross section of an interconnect structure.

Sample Sensitivities to Interconnect

ILD Thickness

Metal Thickness!

0.8 - 1.2µm
Modeling Spatial Matching

- Component Matching is an aspect of process variability that affects the yield of Analog Circuits:
  - D-A converters: capacitor matching.
  - Diff amplifiers, current sources: transistor matching.

Circuit Element “Matching” Models

- In order to describe matching one needs a “spatial” distribution.
- In this case location, as well as distance are factors that will affect process (and performance) variability.
- Several models have been created, either empirically, or by taking into account detailed device parameters.
Pelgrom's Model

\[ \sigma^2(\Delta P) = \frac{A_p}{2WL} + S_p^2 D_x^2 \]

\[ \sigma^2(\Delta P) = \frac{A_p}{WL} + S_p^2 D_x^2 \]

Variance inversely proportional to area, proportional to distance^2.

Example - Resistance Variance vs. Pattern
Example on Variance in Element Array

Example of Variance vs. size, distance

\[ \sigma^2_{\Delta R/R} \text{ vs } 1/L \]

\[ \sigma^2_{\Delta R/R} \text{ vs } D^2 \]
Simulating Parametric Yield

• The process domain can be mapped to the performance domain through random exploration.
• The Yield can then be estimated as \( Y = \frac{N_p}{N} \).
• Though this estimate converges rather slowly, it does have some nice properties.

\[ P\{|Y_{est} - Y| > k\sigma\} < \frac{1}{k^2} \]

Monte Carlo - the speed of Convergence

• Since \( Y \) is a estimate of a random variable, bounds for the actual value of \( Y \) are given by the general Tchebycheff inequality:

\[ P\{|Y_{est} - Y| > k\sigma\} < \frac{1}{k^2} \]

• Since each random experiment can be seen as a Bernoulli trial with \( Y \) probability of success, then if \( N \) is large and \( Y(1-Y)N > 6 \) (or so), we can employ the approximation:

\[ \mu_y = Y \]
\[ \sigma^2_y = Y(1-Y)/N \]

• The estimation bounds are independent of the dimensionality of the process domain.
An Example - EPROM Sense Amp

The two Domains for the Sense Amp
Yield Simulation Example

N = 100, Np = 59
Y = 0.59, \( \sigma^2 = Y(1-Y)/N = 0.05^2 \)
Y = 0.59 +/- 0.15 => 0.44 < Y < 0.74

Next Time on Parametric Yield

- Current and Advanced DFM techniques
  - Worst Case Files
  - Statistical Design
- The economics of DFM