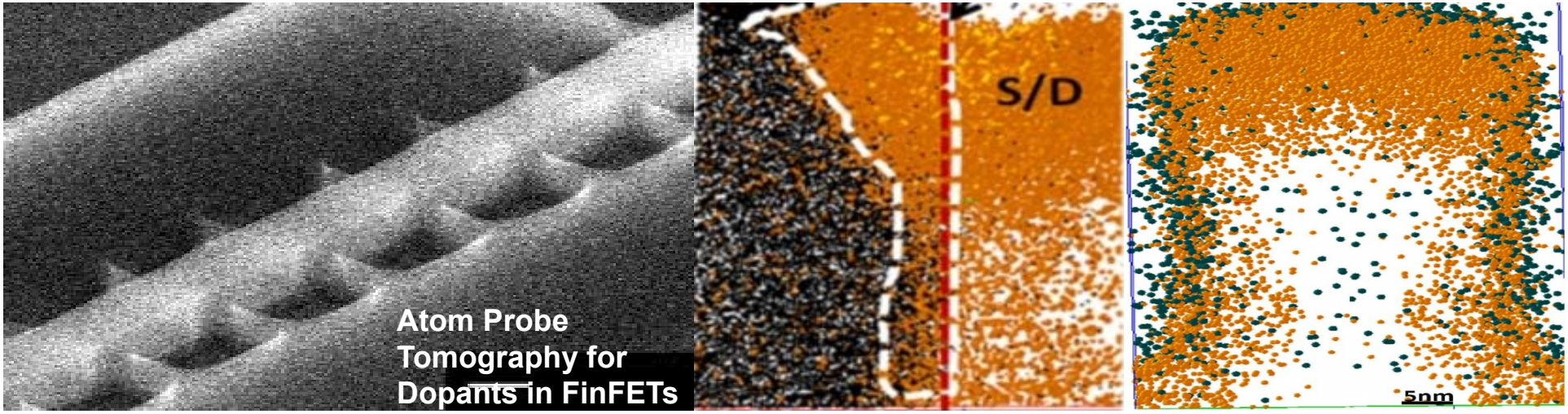


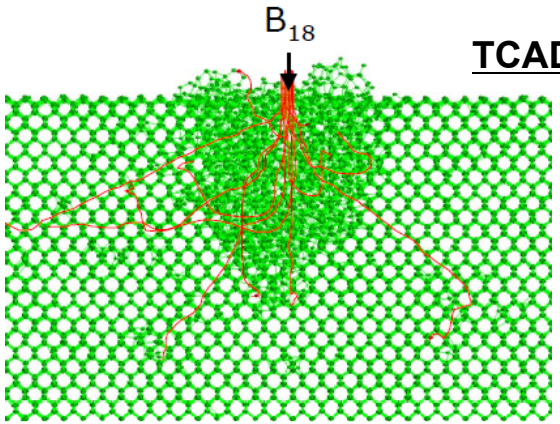
A.K. Kambham (imec), VLSI-T 2012

Lecture 8

- Thin-Body MOSFET's Process II
  - Source/Drain Technologies
  - Threshold Voltage Engineering

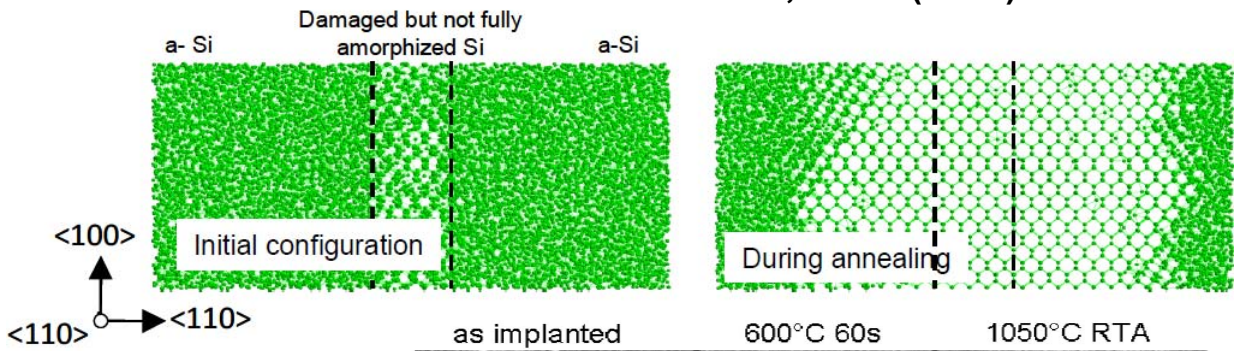
Reading: multiple research articles (reference list at the end of this lecture)

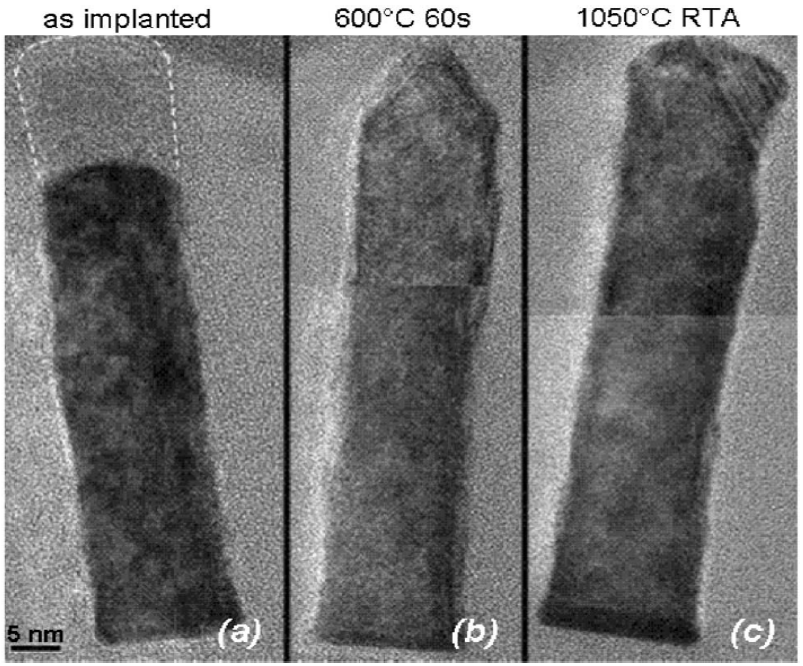
FinFET Source/Drain Doping Challenges: I. Fin Amorphization



TCAD Simulation Results

L. Pelaz, IEDM (2009)





- **After the high energy implantation, Source/Drain regions are always amorphized.**
  → Requires annealing for S/D regrowth to prevent leakage and reliability issues.
- **Source/Drain For <110> FinFETs, the (111) planes will eventually prevent the Si re-crystallization.**

R. Duffy, APL (2007)

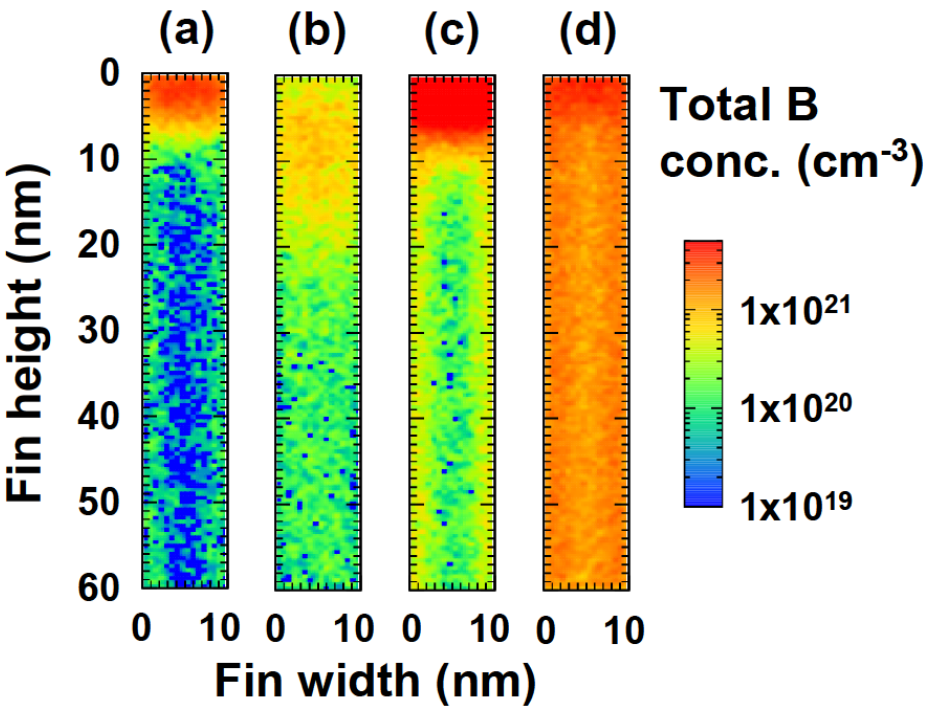
FinFET Source/Drain Doping Challenges: II. Vertical Conformance

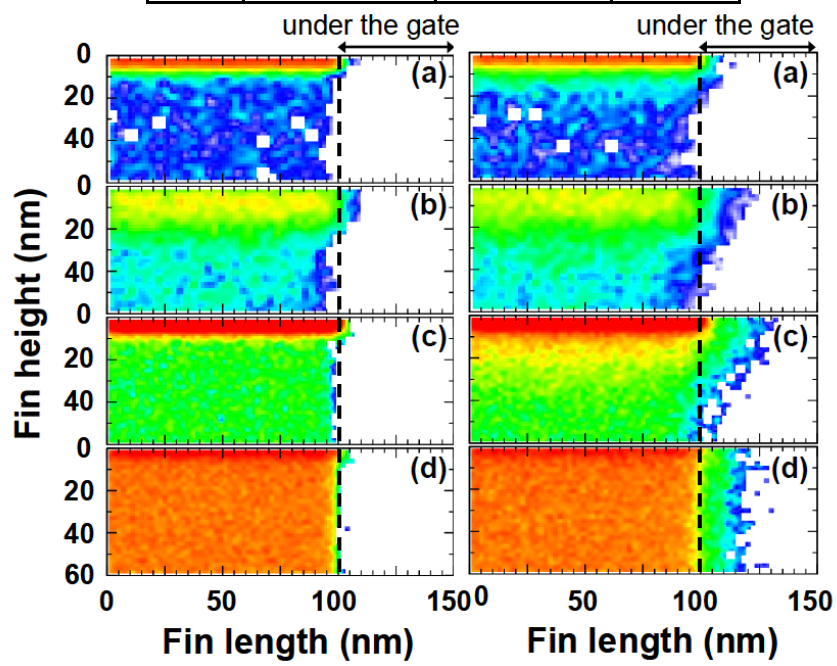
L. Pelaz, IEDM (2009)

	Energy	Dose	Tilt
a	0.5	10^{15}	10°
b	2	10^{15}	10°
c	0.5	$5x10^{15}$	10°
d	0.5	10^{15}	45°

TCAD Simulation Results

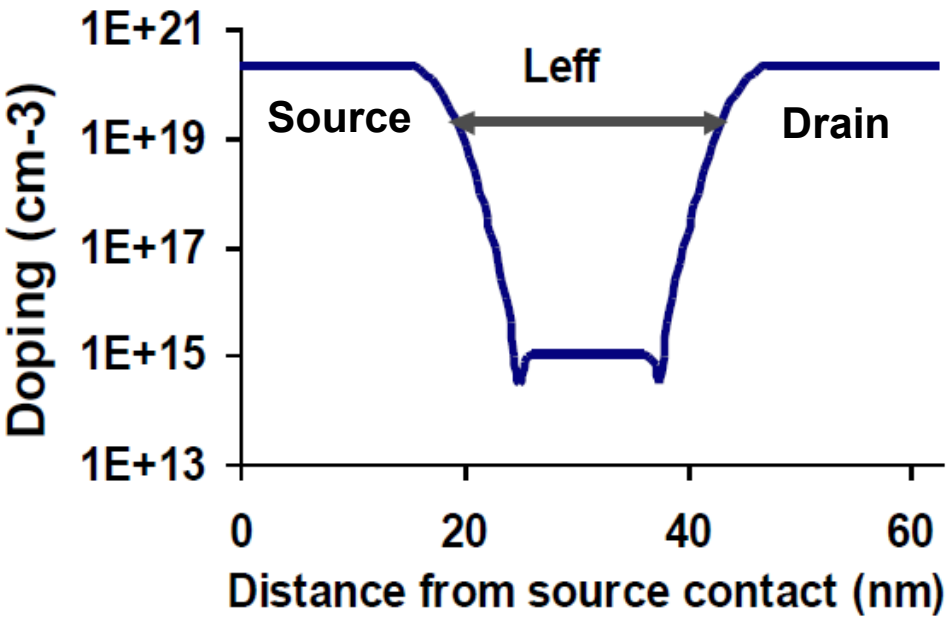
Cross-sectional (left) and lateral (right) view of the B concentration in a FinFET implanted region with:



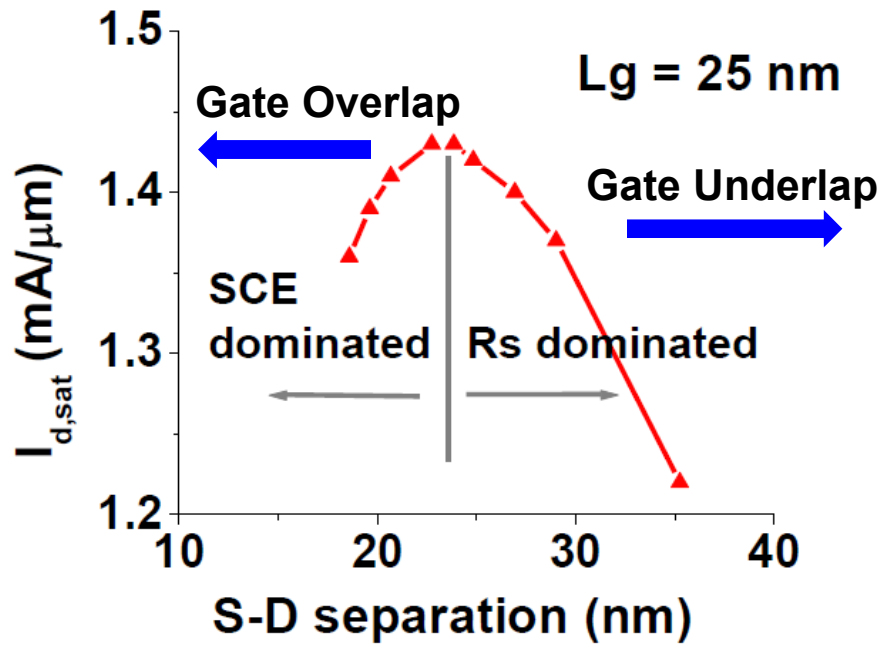


After 1100°C Spike Annealing

Effective Channel Length (L_{eff})



L_{eff} is defined as the separatic between the points where the doping falls off to $2x10^{19}$ cm^{-3}

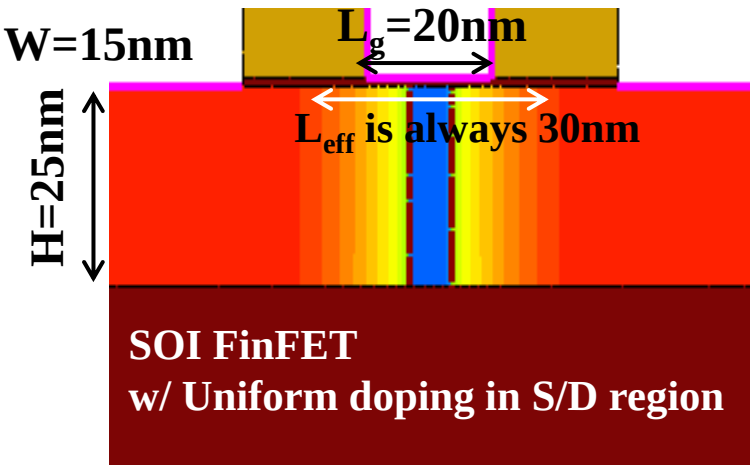


I_{off} spec.: 300 nA/μm

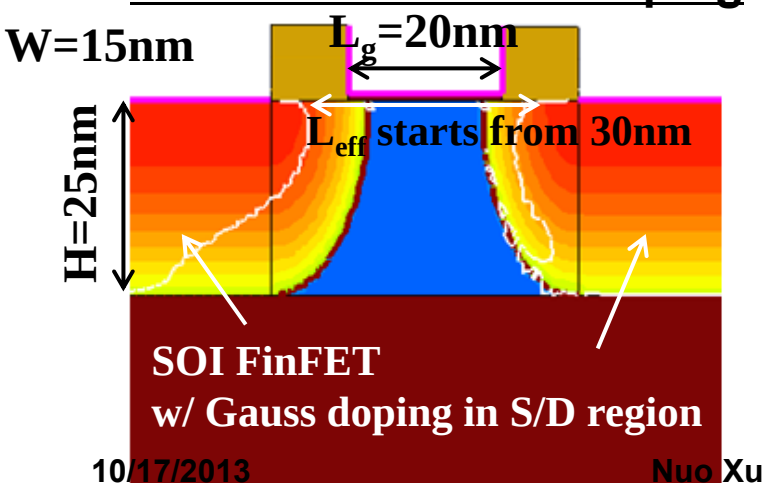
- More reasonable (than L_g) parameter to optimize device performance with a certain gate pitch (*i.e.* technology node).

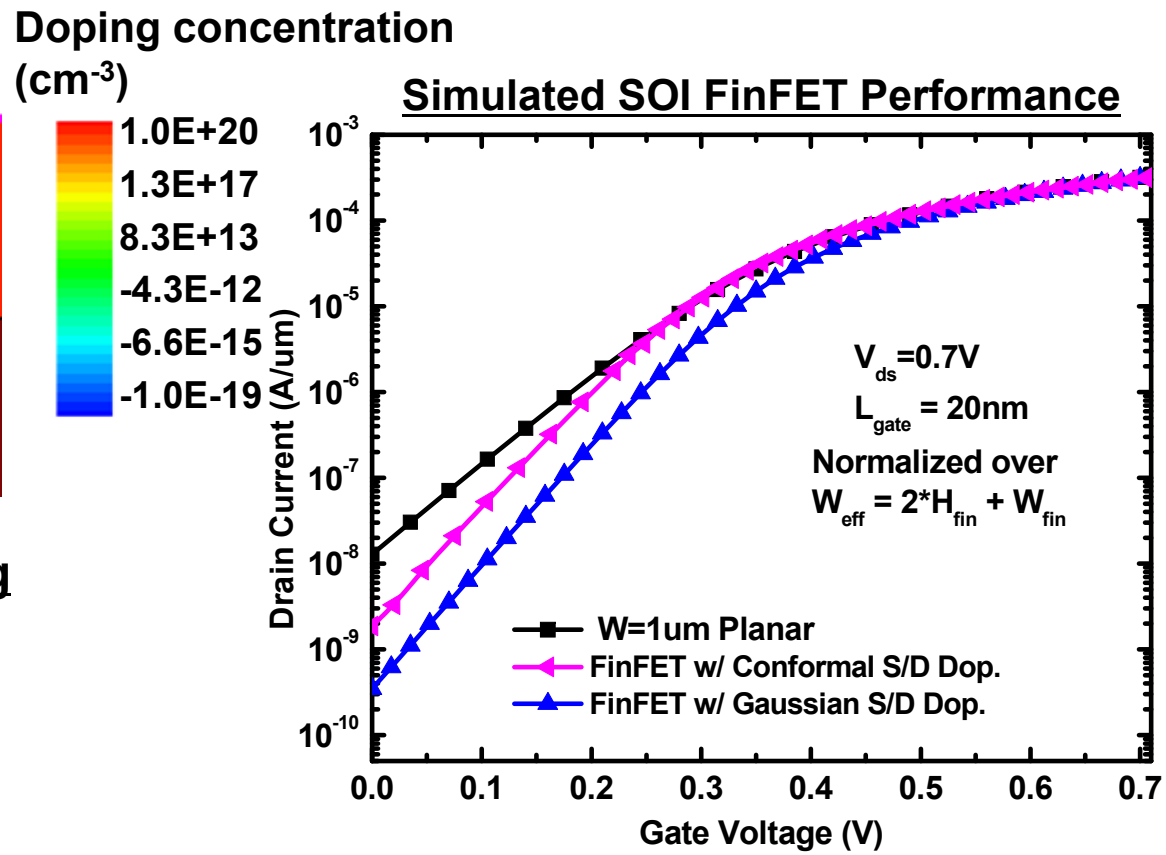
Impacts of Source/Drain Doping Conformance

Conformal S/D Doping



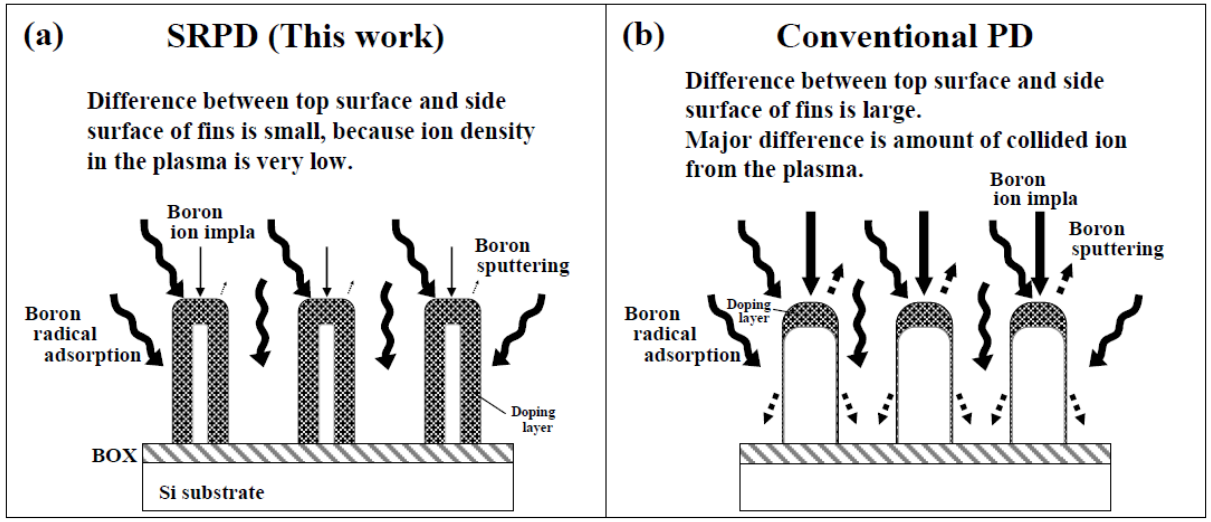
Non-conformal S/D Doping

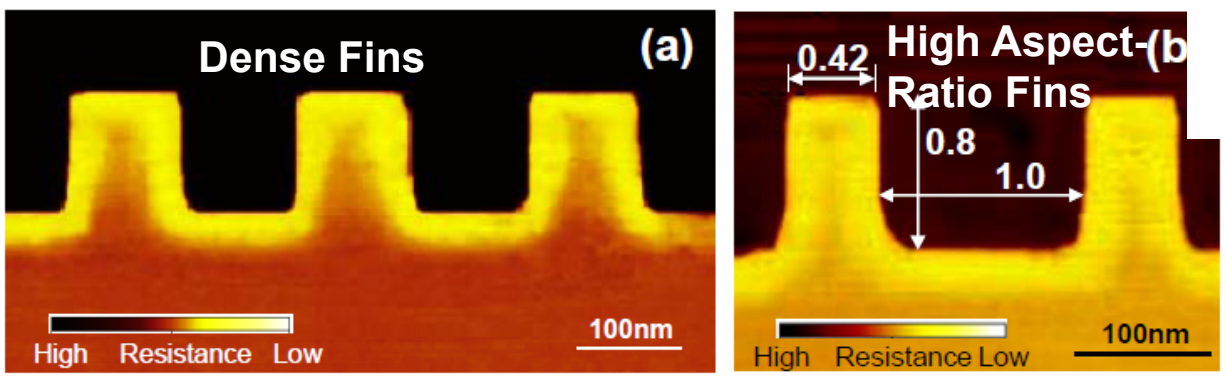


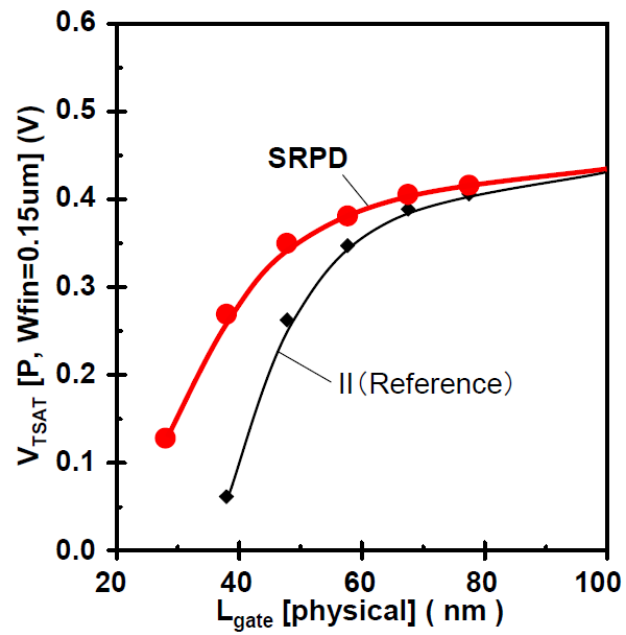


- S/D doping conformance strongly affects FinFET's L_{eff} and causing performance change.

Self-Regulatory Plasma Doping in FinFET's S/D

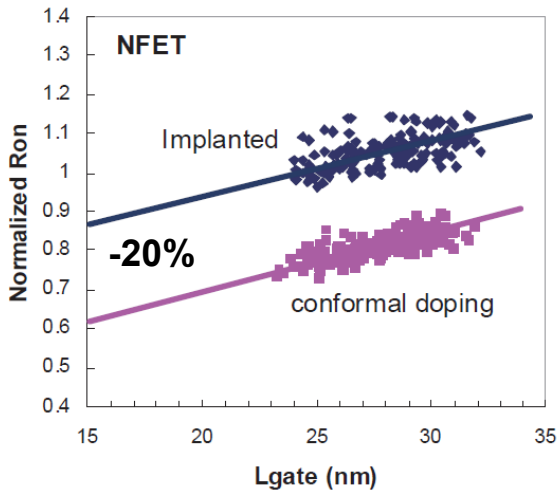


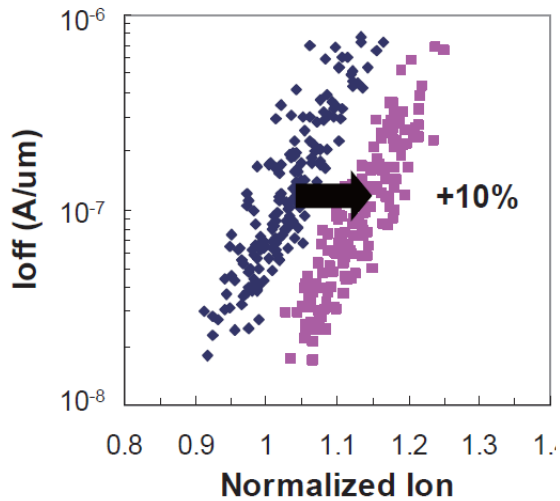




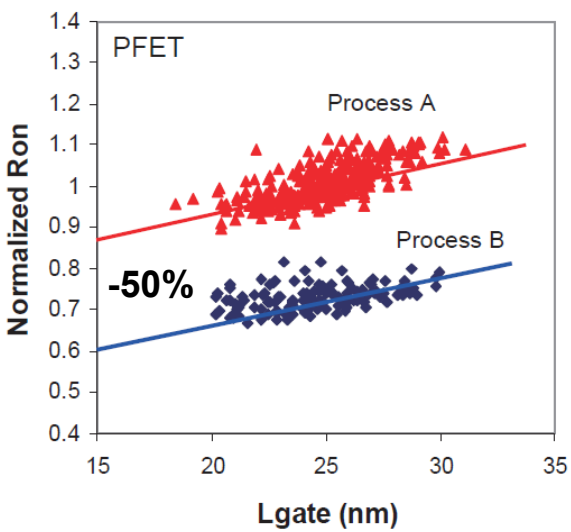
Y. Sasaki, IEDM (2008)

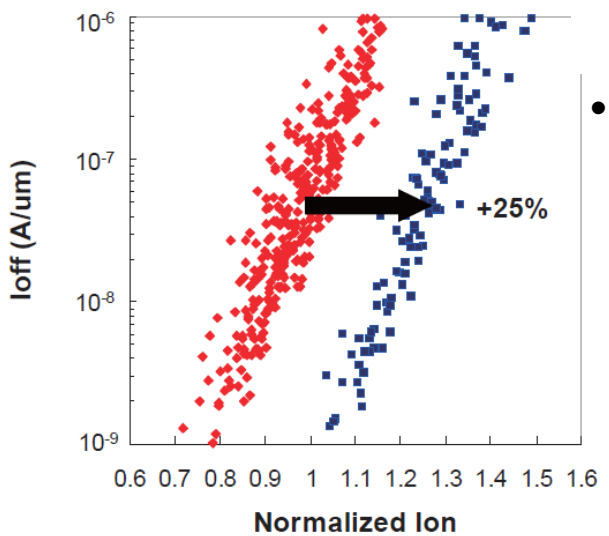
S/D Doping Optimizations for Improving FinFET Performance





- Offset spacer RIE
- Native oxide removal
- Conformal doping for NFET/PFET Extension
- Extension anneal
- Epi pre-clean
- ISBD SiGe Epi grow on PFET/ISPD Epi grow on NFET
- Spacer2 formation
- Multi-Steps S/D Implantation (MSI)
- SD Activation anneal
- Silicide
- Contact/M1



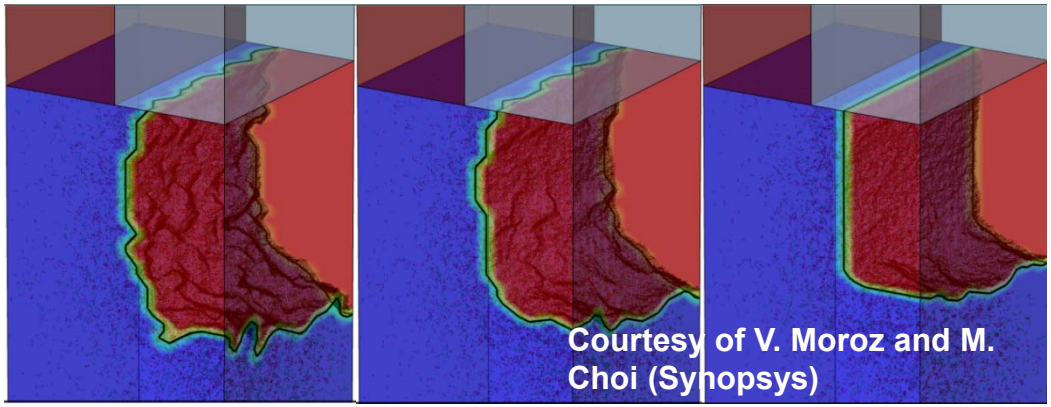


- **A multi-step implantation with different energies and ion species improves the vertical doping conformance.**

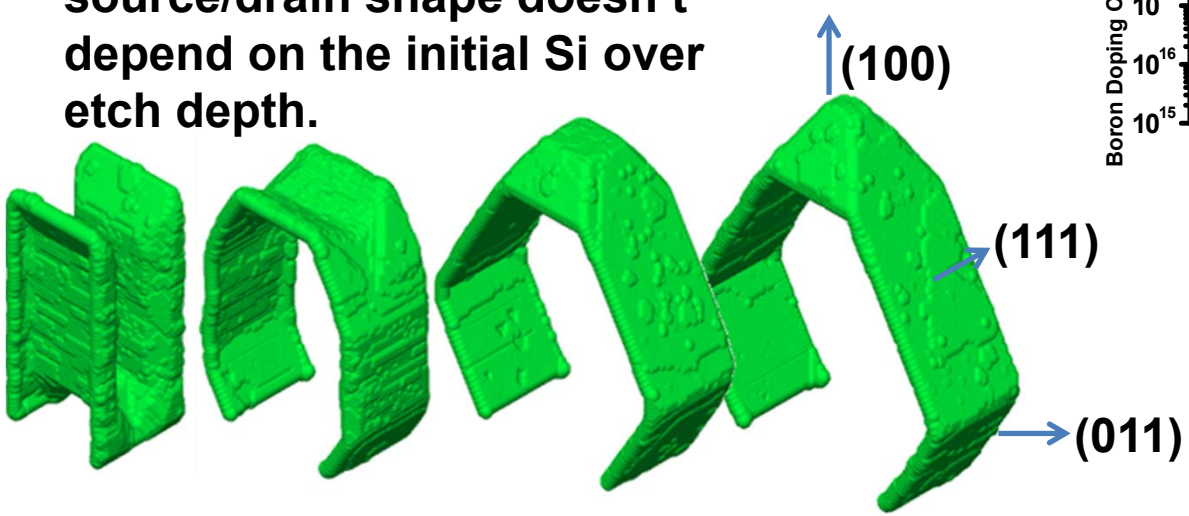
T. Yamashita, VLSI-T (2011)

In Situ-Doped S/D in FinFETs

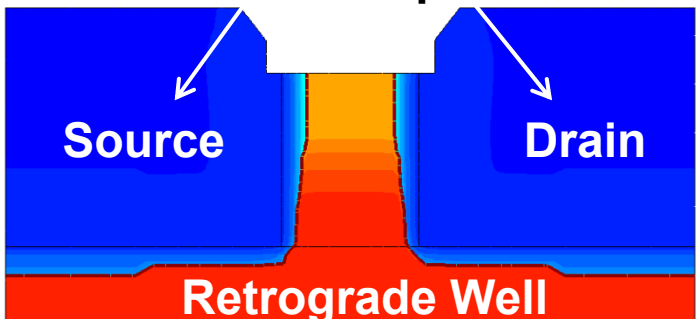
TCAD Simulation Results of S/D epi-regrowth after etching

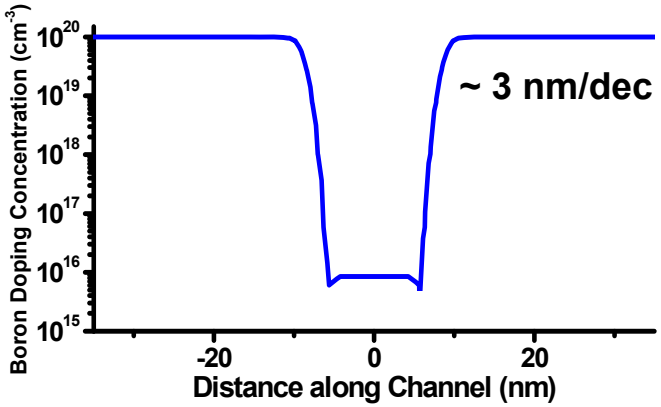


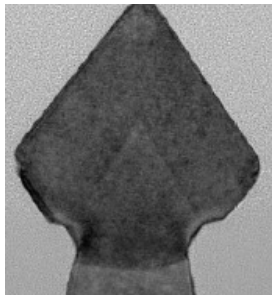
- **Simulation shows the final source/drain shape doesn't depend on the initial Si over etch depth.**



In Situ-doped

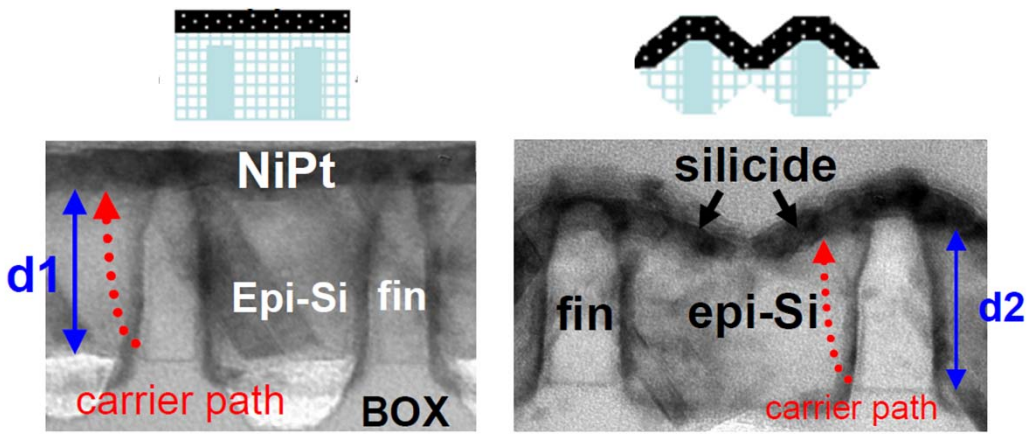


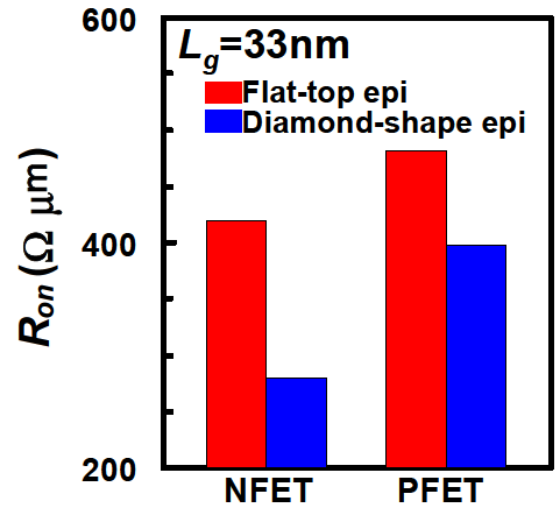


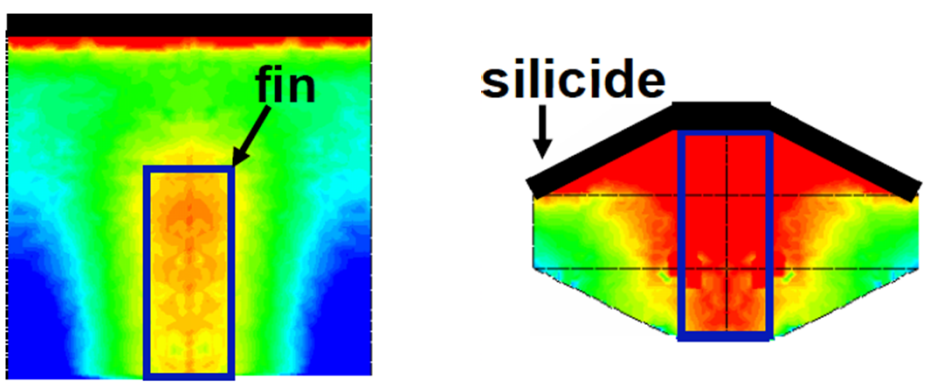


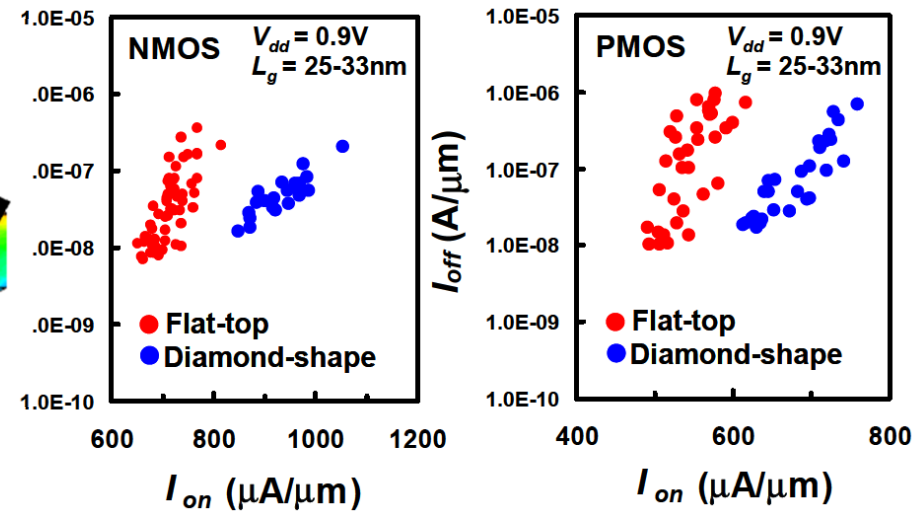
Intel's TriGate FET's S/D

Impact of FinFET's Raised S/D Shape









H. Kawasaki, IEDM (2009)

Why We Want Multiple V_{TH}?

DIFFERENT APPLICATIONS => DIFFERENT NEEDS

SOC

MULTI-FUNCTIONAL

Mobile Internet Device

High-Speed >2GHz
Low Operation Vdd
Low Stdby Leakage

MPU

MONO-FUNCTIONAL

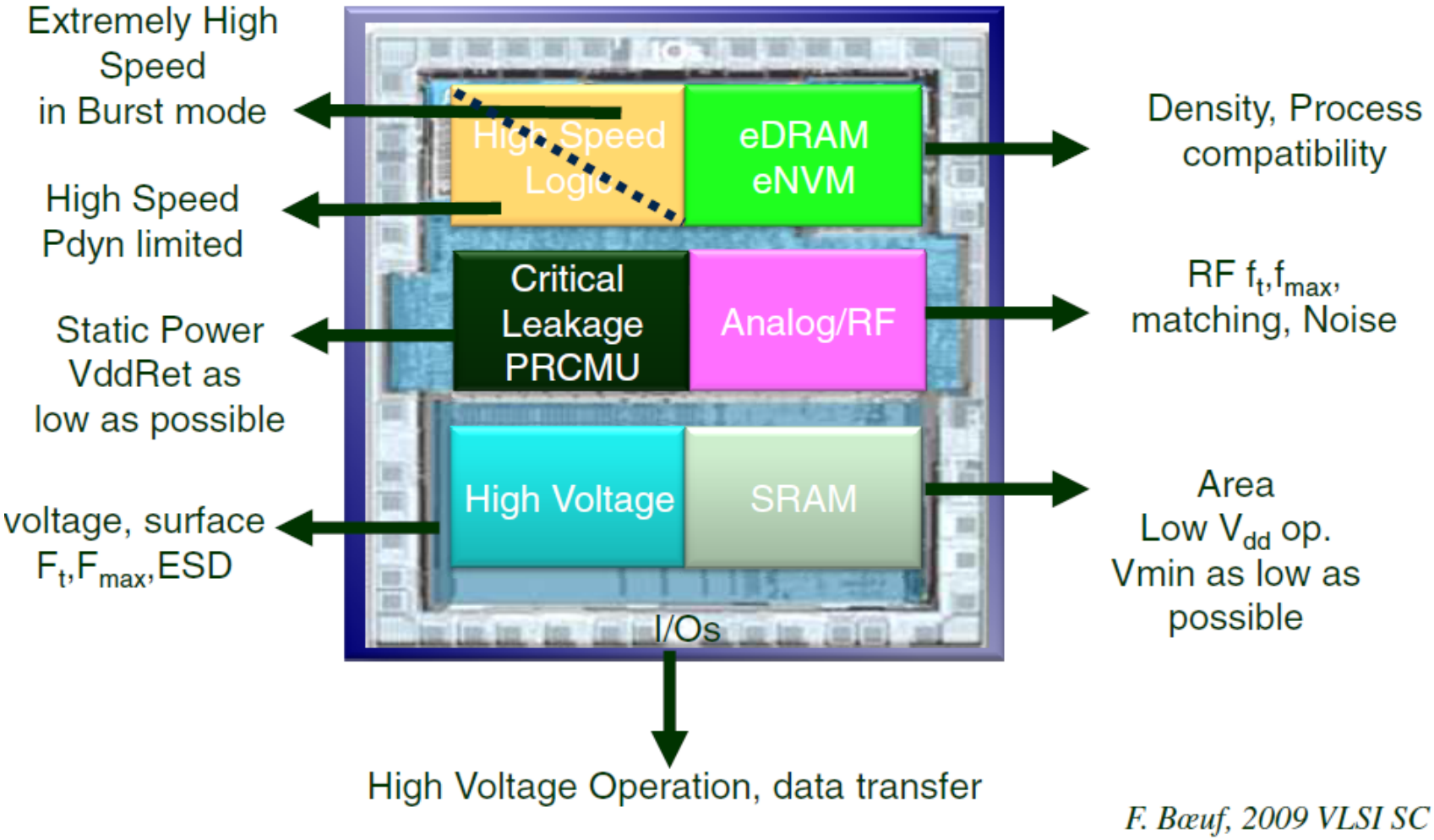
Computers, Servers

High-Speed >>2GHz
High Operation Vdd
High Stdby Leakage

Computers, Servers

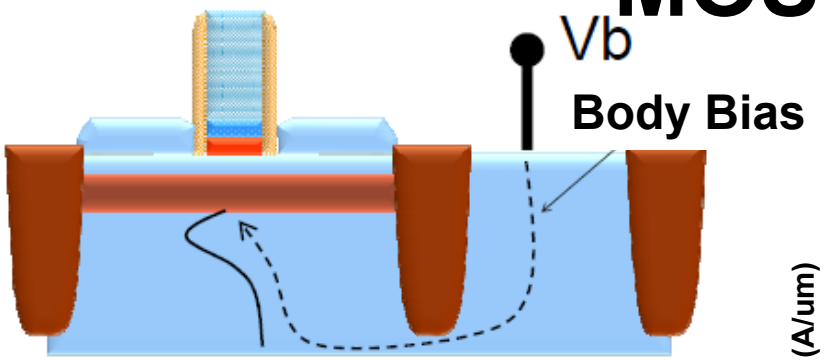
⇒ different technologies needed

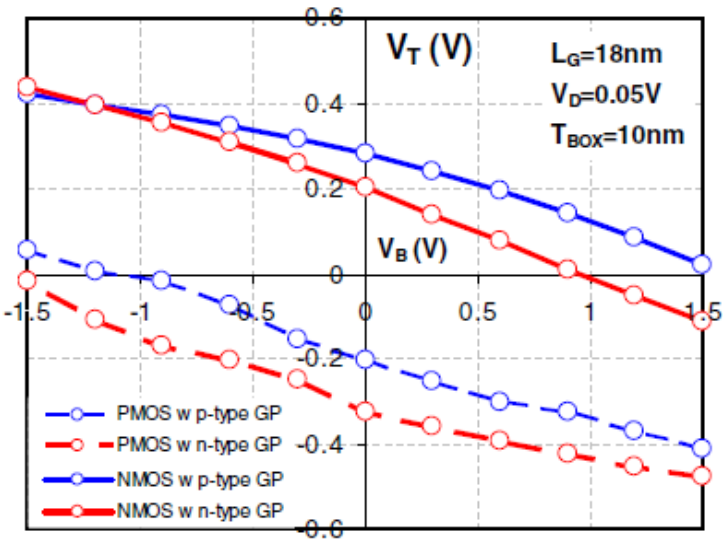
STMicroelectronics T. Skotnicki, 2011 SOI Conf. , Phoenix AZ 4



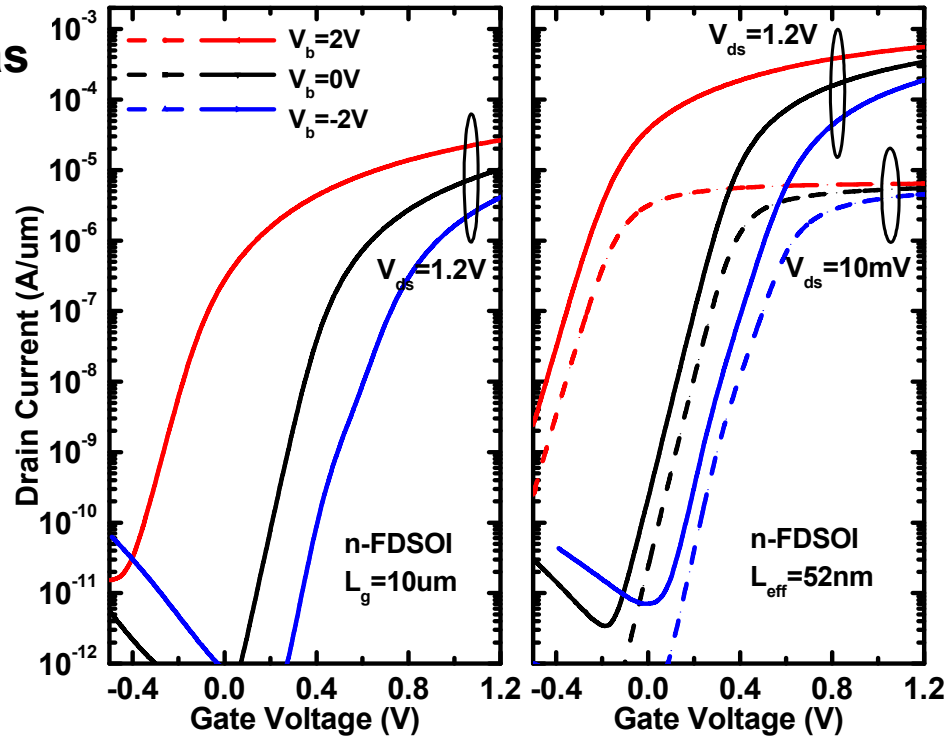
F. Bœuf, 2009 VLSI SC

Back Biasing Tuning in UTBB SOI MOSFETs



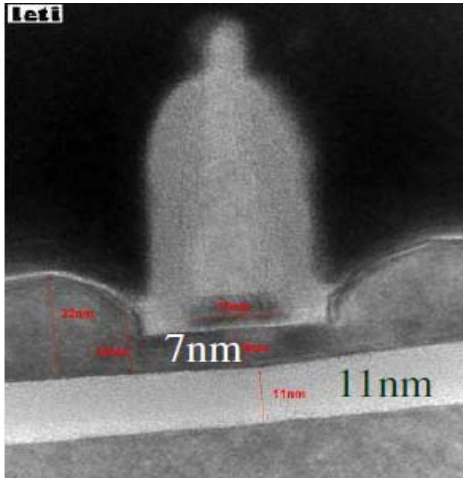


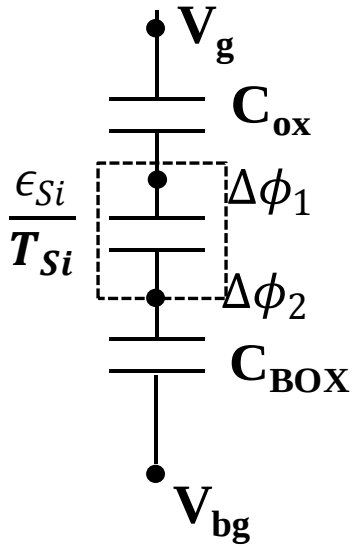
T. Skotnicki, IEDM SC (2010)

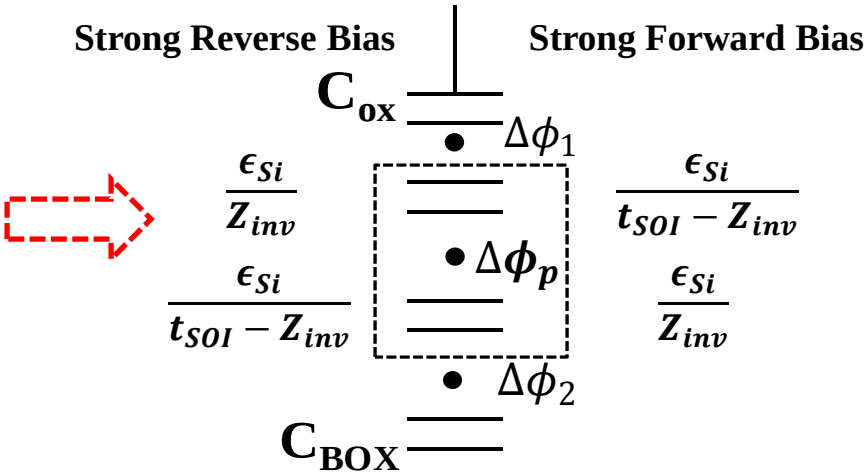


- **Reverse Back Biasing:**
  V_{BG}: NMOS(-), PMOS(+) → V_{TH} ↑
- **Forward Back Biasing:**
  V_{BG}: NMOS(+), PMOS(-) → V_{TH} ↓

(Back Biasing) Body Coefficient



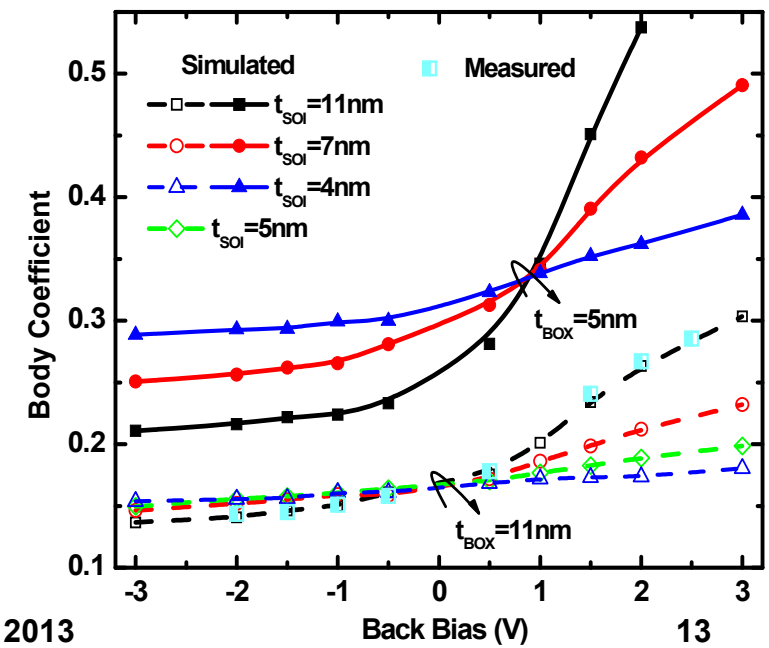




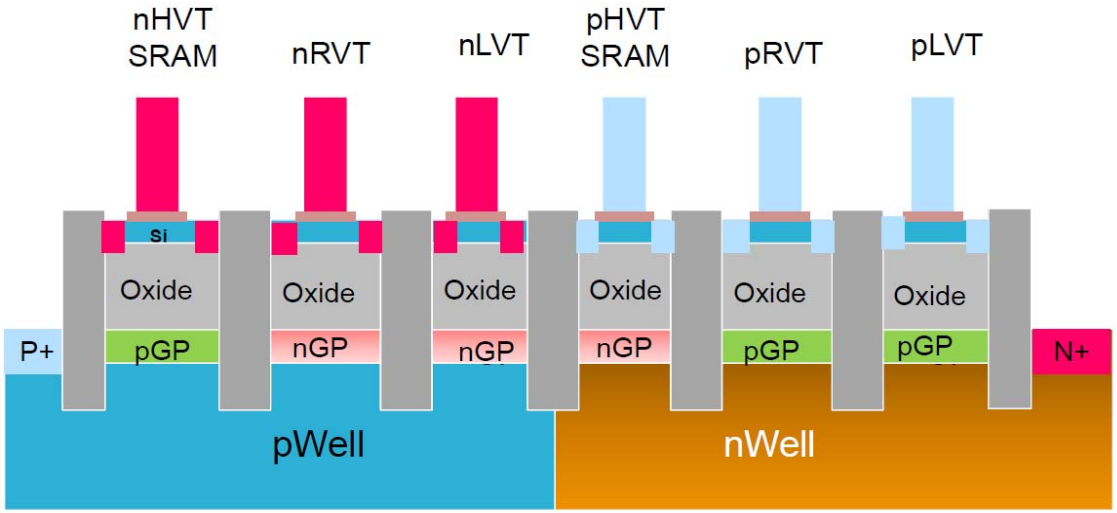
Define coefficient *r* :

$$\gamma = \frac{C_{back}}{C_{front}} = \frac{C_{BOX}//C_{inv,2}}{C_{ox}//C_{inv,1}} = \begin{cases} \dfrac{EOT + \frac{t_{SOI}}{3} - \frac{Z_{inv}}{3}}{t_{BOX} + \frac{Z_{inv}}{3}} & \text{Forward Bias} \\ \dfrac{EOT + \frac{Z_{inv}}{3}}{t_{BOX} + \frac{t_{SOI}}{3} - \frac{Z_{inv}}{3}} & \text{Reverse Bias} \end{cases}$$

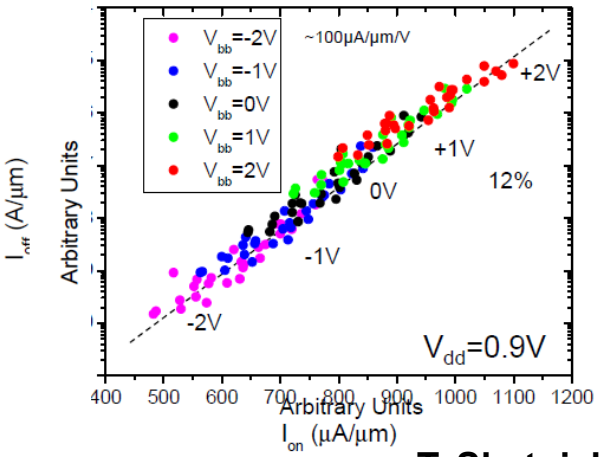
so that $\Delta V_{TH} = r \cdot V_{BG}$



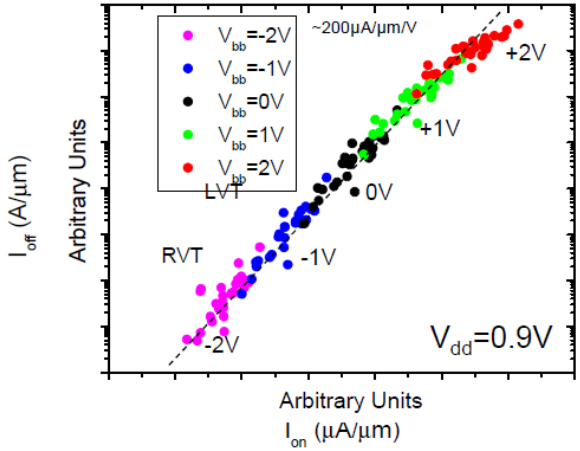
UTBB SOI MOSFET's V_{TH} Engineering



25nm BOX:

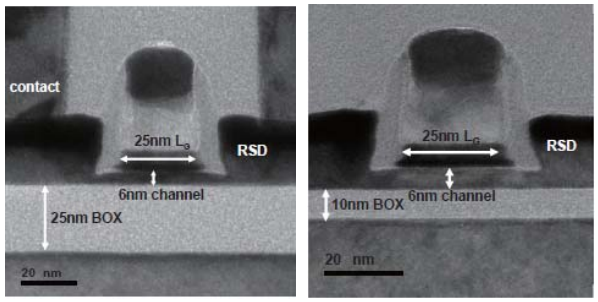


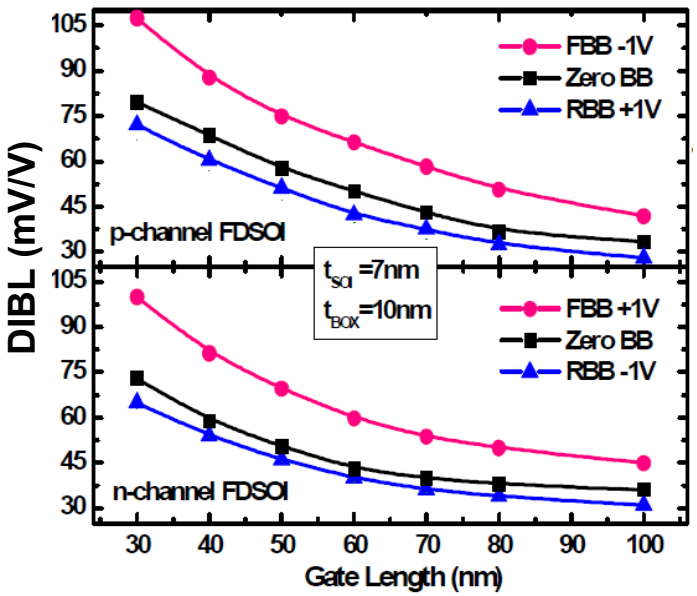
10nm BOX:



T. Skotnicki, IEDM SC (2010)

Impact of Back Biasing on UTBB SOI MOSFET's Electrostatics





N. Xu, VLSI-T (2012)

Q. Liu, VLSI-T (2011)

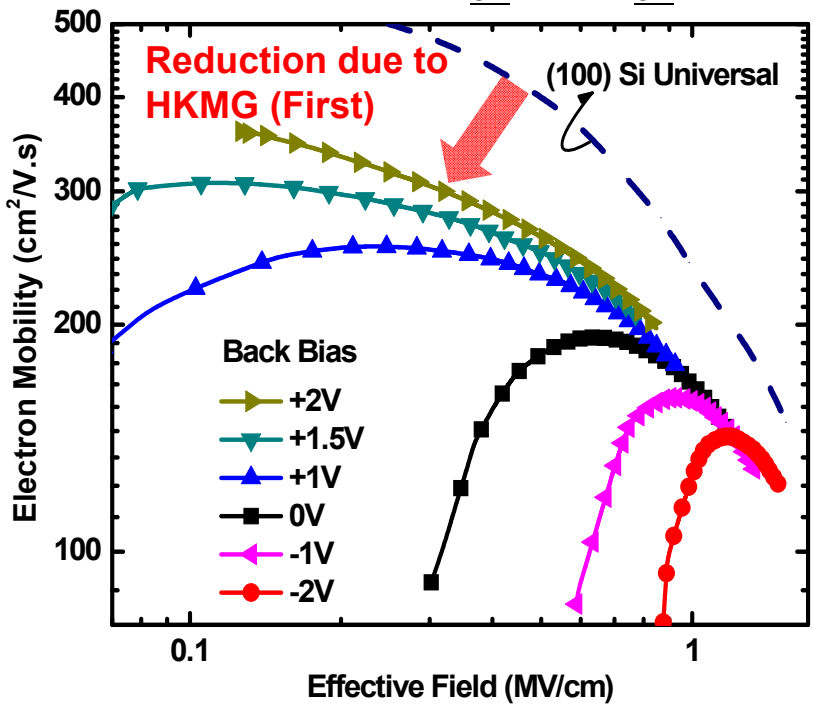
STMicroelectronics' 28nm UTBB FDSOI MOSFETs

T_{BOX}	back bias	I_{on} (μA/μm)	I_{off} (nA/μm)	DIBL (mV/V)	SS (mV/dec)
25nm	-2V	525	0.1	68	90
	-1V	602	0.63	68	89
	0V	682	3.69	70	91
	1V	759	19.9	71	91
	2V	833	126	71	90
10nm	-2V	274	0.009	48	87
	-1V	441	0.26	56	89
	0V	628	10.5	64	91
	1V	807	316	78	93
	2V	958	5040	90	94

- **RBB (or counter-type GP):**
  → better electrostatics
- **FBB (or same-type GP):**
  → worse electrostatics

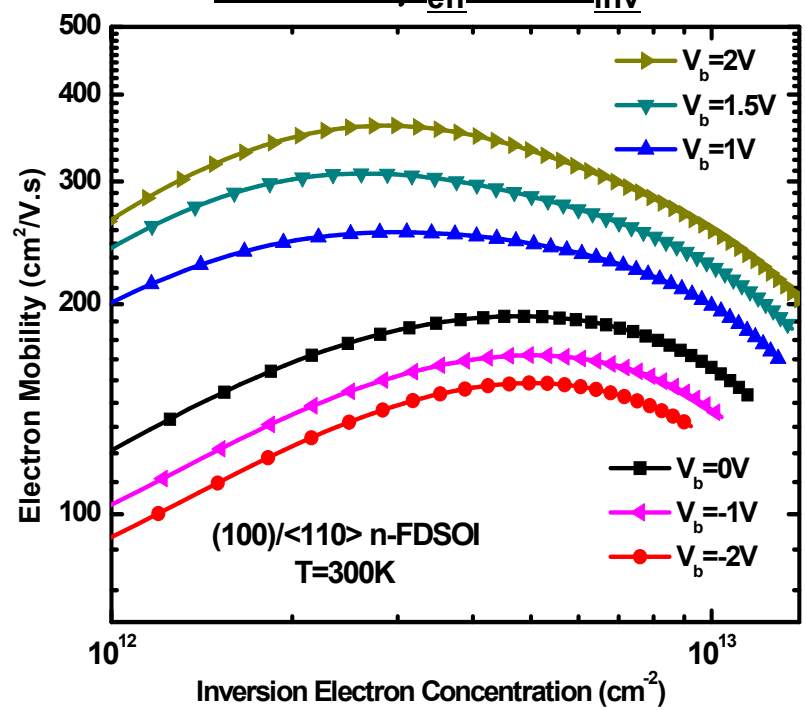
Impact of Back Biasing on UTBB SOI MOSFET's Carrier Mobility

UTBB's μ_{eff} vs. E_{eff}



- still follows universal mobility curve
- However, what matters I_{ON} is μ_{eff} at a certain N_{inv}.

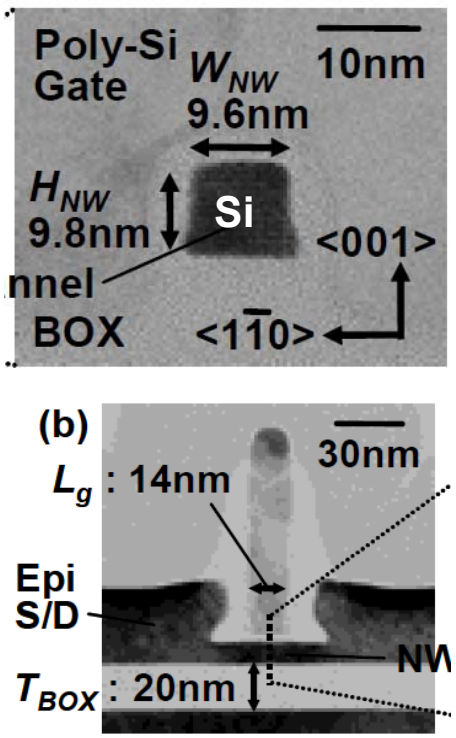
UTBB's μ_{eff} vs. N_{inv}



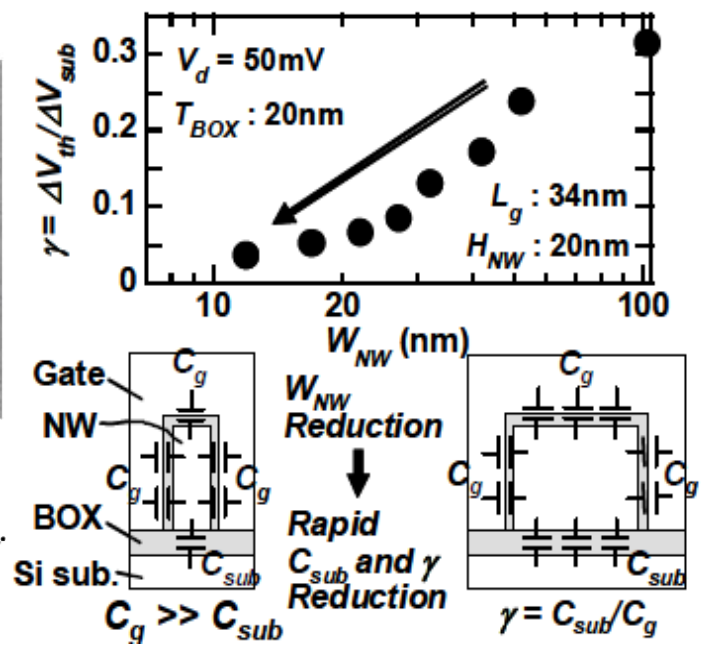
- RBB (or counter-type GP): → lower mobility
- FBB (or same-type GP): → higher mobility

Back Biasing in Tri-Gate MOSFET

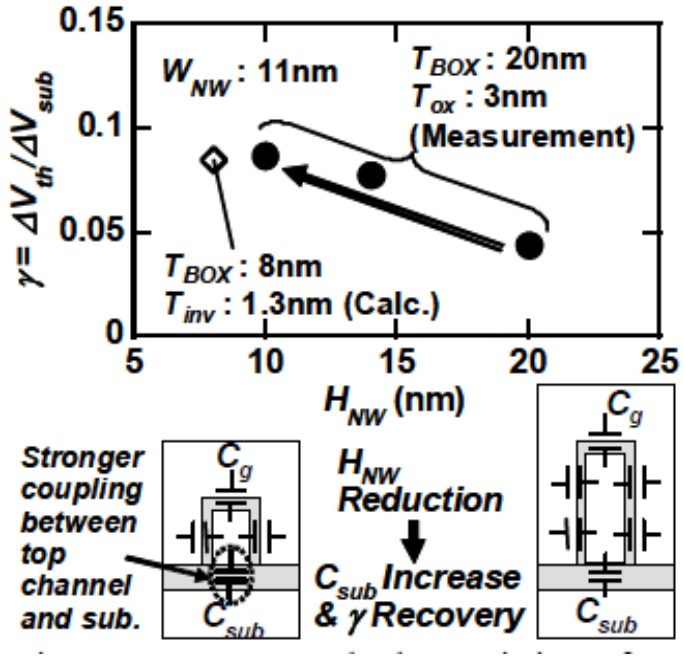
TEM of Nanowire Tri-Gate FET



BB-V_{th} Tuning *vs.* W_{Fin}



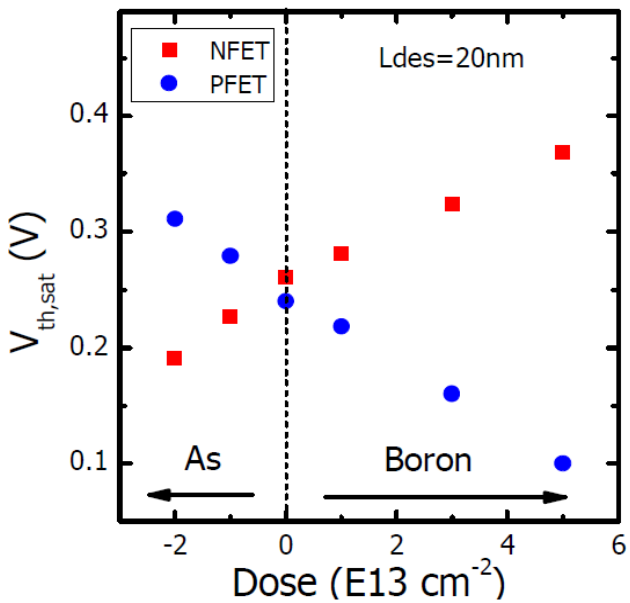
BB-V_{th} Tuning *vs.* H_{Fin}



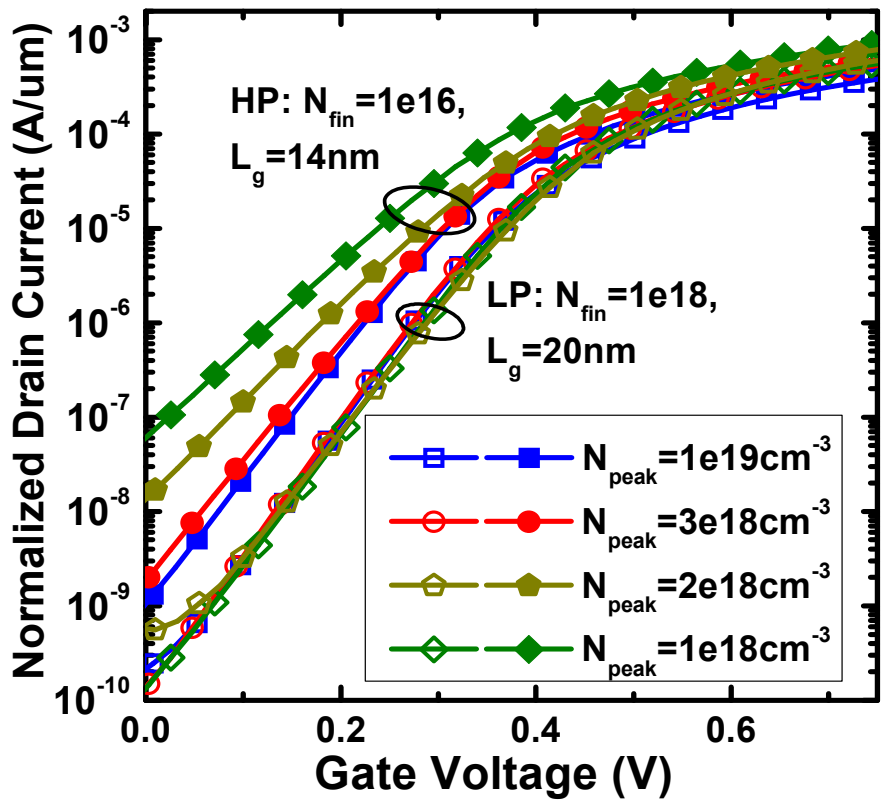
- **Back Biasing will be ineffective to tune V_{TH} when the back surface area is relatively small.**
  → Not an option for typical FinFETs.

M. Saitoh, VLSI-T (2012)

FinFET's V_{TH} Engineering



C.-H. Lin, VLSI-T (2012)

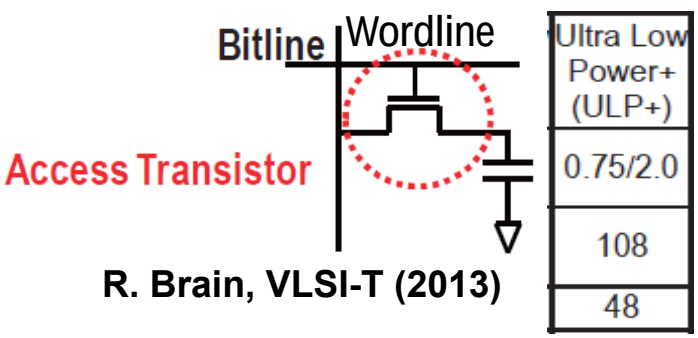


- The V_{TH} tuning ability of channel doping is limited in FinFET, due to the shrink of Si volume as well as the superposition from PTS doping profile.
- Multiple gate length (L_{eff}) has to be used to tune V_{TH}.

State-of-the-Art FinFET's SoC

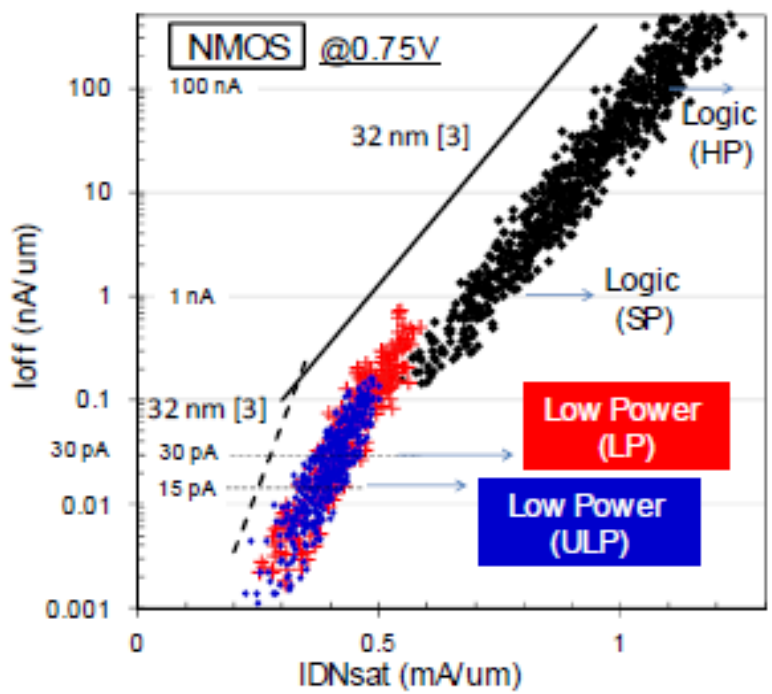
Intel's 20nm TriGate MOSFET

Transistor Type	High Speed Logic		Low Power Logic		High Voltage	
Options	High Performance (HP)	Standard Perf./ Power (SP)	Low Power (LP)	Ultra Low Power (ULP)	1.8 V	3.3 V
Vdd (Volt)	0.75 / 1	0.75 / 1	0.75 / 1	0.75/1.2	1.5/1.8/3.3	3.3 / >5
Gate Pitch (nm)	90	90	90	108	min. 180	min. 450
Lgate (nm)	30	34	34	40	min. 80	min. 280
N/PMOS Idsat/Ioff (mA/um)	1.08/ 0.91 @ 0.75 V, 100 nA/um	0.71 / 0.59 @ 0.75 V, 1 nA/um	0.41 / 0.37 @ 0.75 V 30 pA/um	0.35 / 0.33 @ 0.75 V 15 pA/um	0.92 / 0.8 @ 1.8 V 10 pA/um	1.0 / 0.85 @ 3.3 V 10 pA/um



R. Brain, VLSI-T (2013)

NMOS: I_{off}-I_{dsat}



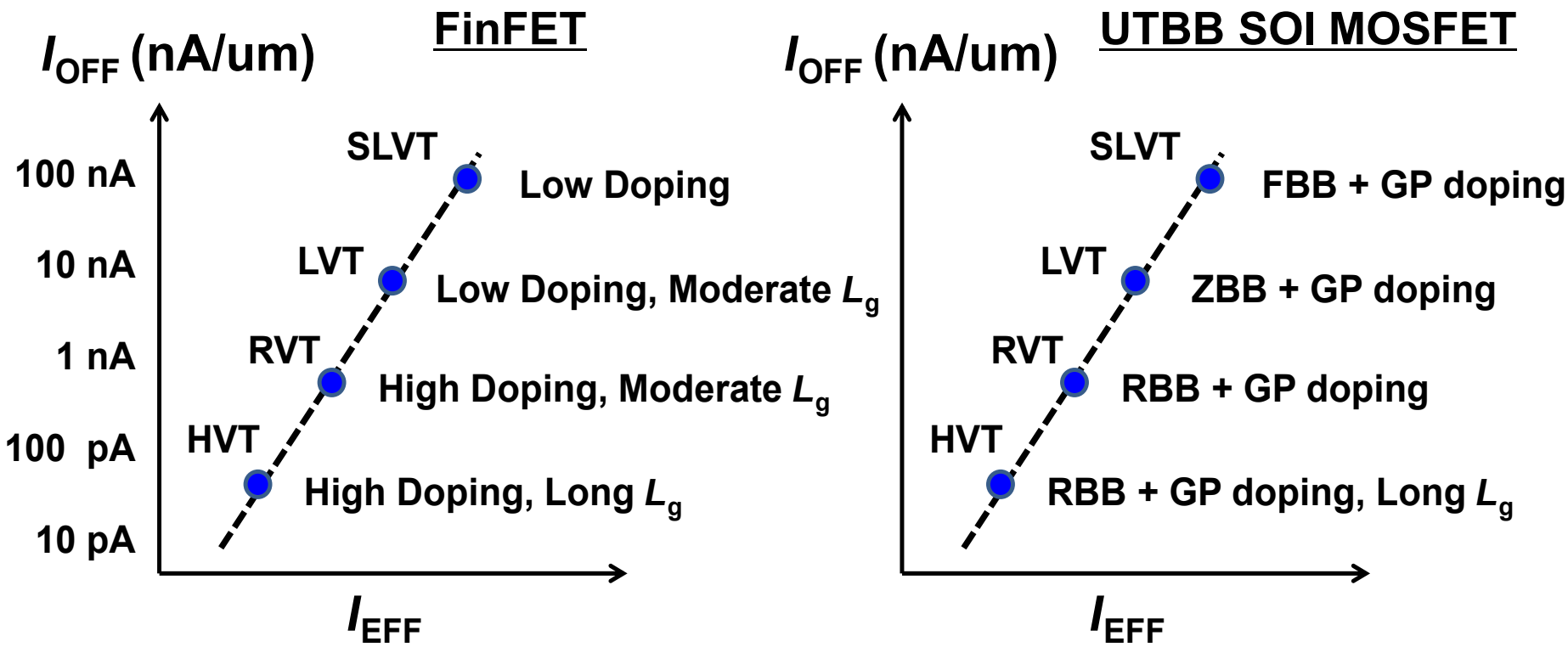
C.-J. Jan, IEDM (2012)

Knobs:

- **gate length (L_g & L_{eff})**
- **Doping (PTS, Fin…)**

Summary of FinFET and UTBB SOI MOSFET's V_{TH} Engineering

- Assuming single gate metal (workfunction) for each type (N or P) of MOSFETs.



References

FinFET Source/Drain

1. L. Pelaz, L. Marques, M. Aboy, P. Lopez, I. Santos, R. Duffy, "Atomistic Process Modeling Based on Kinetic Mone Carlo and Molecular Dynamics for Optimization of Advanced Devices," *IEEE International Electron Device Meeting Tech. Dig.*, pp. 513-516, 2013.
2. R. Duffy, M.J.H. Van Dal, B.J. Pawlak, M. Kaiser, R.G.R. Weemaes *et al*., "Solid Phase Epitaxy versus Random Nucleation and Growth in sub-20nm Wide Fin Field-Effect Transistors," *AIP Applied Physics Letters*, Vol.90, 241912, 2007.
3. Y. Sasaki, K. Okashita, K. Nakamoto, T. Kitaoka, B. Mizuno *et al*., "Conformal Doping for FinFETs and Precise Controllable Shallow Doping for Planar FET Manufacturing by a Novel B2H6/Helium Self-Regulatory Plasma Doping Process," *IEEE International Electron Device Meeting Tech. Dig.,* pp. 917-920, 2008.
4. T. Yamashita, V.S. Basker, T. Standaert, C.-C. Yeh, T. Yamamoto *et al*., "Sub-25nm FinFET with Advanced Fin Formation and Short Channel Effect Engineering," *Symposium on VLSI Technology Dig*., pp.14-15, 2011.
5. M. Choi, V. Moroz, L. Smith, O. Penzin, "14nm FinFET Stress Engineering with Epitaxial SiGe Source/Drain," *International SiGe Technology and Device Meeting Tech. Dig*., 2012.
6. H. Kawasaki, V.S. Basker, T. Yamashita, C.-H. Lin, Y. Zhu *et al*., "Challenges and Solutions of FinFET Integration in an SRAM Cell and a Logic Circuit for 22nm Node and Beyond," IEEE *International Electron Device Meeting Tech. Dig.,* pp. 289-292, 2009.

UTBB SOI V_{TH} Tuning

7. T. Skotnicki, "CMOS Technologies – Trends, Scaling and Issues," *IEEE International Electron Device Meeting Short Course*, 2010.

References

8. Q. Liu, F. Monsieur, A. Kumar, T. Yamamoto, A. Yagishita *et al*., "Impact of Back Bias on Ultra-Thin Body and BOX (UTBB) Devices," *Symposium on VLSI Technology Dig*., pp.160-161, 2011.

9. N. Xu, F. Andrieu, B. Ho, B.-Y. Nguyen, O. Weber *et al*., "Impact of Back Biasing on Carrier Transport in Ultra-Thin-Body and BOX (UTBB) Fully Depleted SOI MOSFETs," *Symposium on VLSI Technology Dig*., pp.113-114, 2012.

FinFET V_{TH} Tuning

10. M. Saitoh, K. Ota, C. Tanaka, K. Uchida, T. Numata, "10nm-Diameter Tri-Gate Silicon Nanowire MOSFETs with Enhanced High-Field Transport and V_{TH} Tunability through Thin BOX," *Symposium on VLSI Technology Dig*., pp.11-12, 2012.

11. C.-H. Lin, R. Kambhampati, R.J. Miler, T.B. Hook, A. Bryant *et al*., "Channel Doping Impact on FinFETs for 22nm and Beyond," *Symposium on VLSI Technology Dig*., pp.15-16, 2012.

12. (Intel's Tri-Gate SoC) C.-H. Jan, U. Bhattacharya, R. Brian, S.-J. Choi, G. Gurello *et al*., "A 22nm SoC Platform Technology Featuring 3-D Tri-Gate and High-k/Metal Gate, Optimized for Ultra Low Power, High Performance and High Density SoC Applications," *IEEE International Electron Device Meeting Tech. Dig*., pp.44-47, 2012.

13. (Intel's Tri-Gate eDRAM) R. Brian, A. Baran, N. Bisnik, H.-P. Chen, S.-J. Choi *et al.,* "A 22nm High Performance Embedded DRAM SoC Technology Featuring Tri-Gate Transistors and MIMCAP COB," *Symposium on VLSI Technology Dig*., pp.16-17, 2013.