Lecture 7

- Thin-Body MOSFET’s Process I
  - SOI vs. Bulk FinFETs
  - Fin Patterning Techniques
  - High-κ/Metal Gate Technologies

Reading: multiple research articles (reference list at the end of this lecture)
SOI vs. Bulk FinFET: Overall Structure

Bulk FinFET

SOI FinFET (w/o BOX)

Gate
Epitaxial Source/drain
Active Fin
Sub-fin leakage path
Junction depth
Thermal conduction path
Junction Isolation
Dielectric Isolation

T. Hook (IBM), FDSOI Workshop (2013)
• Fin heights are defined by the SOI film thickness.
• Higher (SOI) substrate cost; yet cheaper doping/implantation cost.

A. Yagishita (Toshiba), SOI Short Course (2009)
Bulk FinFET Process Flow

- Fin heights are defined by the punch-through stopping (PTS) layer position.

A. Yagishita (Toshiba), SOI Short Course (2009)
Fin Patterning

Spacer Lithography  
a.k.a. Sidewall Image Transfer (SIT)  
or Self-Aligned Double Patterning (SADP)

1. Deposit & pattern sacrificial layer

2. Deposit mask layer (SiO₂ or Si₃N₄)

3. Etch back mask layer to form “spacers”

4. Remove sacrificial layer; etch SOI layer to form fins

• Note that fin pitch is 1/2× that of patterned layer

• Extra lithography steps required to etch the unused fins.
Benefit on Multiple Device Pitch

- By using spacer lithography technique, multiple fin pitches can be implemented using a single lithography step.

- $2^n$ lines after $n^{th}$ lithography!

A. Yagishita (Toshiba), SOI Short Course (2009)
Benefit on Fin Edge Roughness


- Spacer lithography technique provides more uniform fin width than the conventional lithography, due to $\sigma_{\text{litho}} > \sigma_{\text{CVD}}$

Benefit on Gate Edge Roughness

X. Sun, TSM (2010)

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3keV 3E14cm⁻² As implant through 10nm liner
Less diffusion → Worse junction roughness

Tri-Gate \(I_d-V_g\) Curves
Fin Sidewall Damage Removal by H$_2$ Annealing

H$_2$ annealing causes Si atoms remigration at fin sidewall surfaces

- provides smaller surface roughness and lower D$_{it}$.
- reduces shape corners to mitigate "corner effect".

Fin Sidewall Damage Removal by Neutral Beam Etching

- Neutral Beam Etching: negative ions in the plasma can be neutralized by passing through the carbon aperture.
- TEM picture shows more abrupt fin/oxide interface after NBE $\rightarrow$ Lower $D_{it}$
- Higher fin mobility w/ NBE

K. Endo, TED (2006)
SOI vs. Bulk FinFET: Isolation

- Retrograde-well doping required as punch through-stop (PTS) layer.
- HALO is also often adopted.
- Tapered fin shape due to STI process.

Bulk FinFET

- No doping process needed to avoid PT.
- Rectangular fin shape.

T. Hook (IBM), FDSOI Workshop (2013)
Impacts of Retrograde Well Doping

- Even with the finite steepness of retrograde well doping (~15nm/dec in Si), it is still preferred to insert the doping peak around the fin base, causing some level of performance degradation in the fin.
More Issues for Bulk FinFET Isolation

Bulk FinFETs require
- Junction isolation masks and implants
- Well contacts
- Latchup prevention measures
  Second STI
  Heavily doped substrate

- Single PTS doping can not be used for SoC circuits with multi-fin width.
- Additional STI required to separate N and P-bulk FinFET, to avoid CMOS latchup effect.
Steep Retrograde Well Doping in Bulk FinFET

SSRW formation using Si + Si:C epi before STI formation

C-doped Si (Si:C) diffusion block layer

- B for nFET
- As for pFET

Punch-through stopper

Conc.
✓ Thermal stability of Si:C layer
  • Precipitates and clustering of C atoms → Defects in Si + Si:C epi layer
  • C-diffusion

H. Bu (IBM), SOI Workshop (2011)

A. Hokazono,

H. Bu (IBM), SOI Workshop (2011)
Fin Shape Variations in Bulk FinFETs

Rectangular shape

Trapezoidal shape (Intel’s Tri-Gate)

“Hybrid”-shape

Chipworks, 2012

D. Shamiryan, SSE (2009)

Typical STI trench tilt: $70^\circ$ ~ $85^\circ$

Key requirements for bulk fin shape (process perspective):

- Isolation trench refilling
- High aspect-ratio fin patterning

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Impacts of Fin Shape on Electrostatics

assuming same top fin width:

Key requirements for bulk fin shape (device performance/reliability perspective):

- Good electrostatic control
- Low corner electric field, to prevent TDDB or BTI
Impacts of Fin Shape on Current

Charge concentration across a FinFET X-section as increasing gate voltage

A. Arsenov’s group, GSS Website (2012)
Considering Quantum Mechanical + Strain Effect

Simulation Data from Synopsys Inc., (2013)
High-κ/Metal Gate Technology

Gate First / MIPS (Metal-Inserted-Poly-Si Gate)

Gate Last / RMG (Replaced Metal Gate)
## Gate First vs. Gate Last

L. Ragnarsson, IEDM (2009)

<table>
<thead>
<tr>
<th>High-κ Dielectric</th>
<th>First</th>
<th>First $\rightarrow$ Last</th>
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</thead>
<tbody>
<tr>
<td>Metal Gate</td>
<td>First</td>
<td>Last</td>
</tr>
<tr>
<td>Thermal Budget</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>EOT</td>
<td>Thick</td>
<td>Thin</td>
</tr>
<tr>
<td>Mobility</td>
<td>Low</td>
<td>High</td>
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<tr>
<td>Workfunction Control</td>
<td>Bad</td>
<td>Good</td>
</tr>
<tr>
<td>Cost</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Process Complexity</td>
<td>Low</td>
<td>High (CMP)</td>
</tr>
</tbody>
</table>

![Graph showing EWF vs. EOT for Gate-First and Gate-Last processes](graph.png)
Thin-Body MOSFET Gate Process

- Extremely-thin UTB SOI is not compatible with high-κ-last process, due to the Si sacrifice during dummy (poly-Si) gate removal.
- FinFET RMG is challenging, due to the 3-D CMP process.
- Cost is the dominant issue.

IBM’s ETSOI MOSFET

A. Khakifirooz, EDL (2012)

A. Yagishita (Toshiba), SOI Short Course (2009)
References


