Lecture 5

• Thin-Body MOSFET Carrier Transport
  – quantum confinement effects
  – low-field mobility: Orientation and Si Thickness Dependence
• Non-Idealities in Nano-Scale $L_g$ MOSFET Transport
  – Quasi-Ballistic Transport
  – Apparent Mobility
  – Series Resistance

Reading:
- multiple research articles (reference list at the end of this lecture)
Due to the anisotropic $E$-$k$ relationships, quantum confinement and carrier mobility are surface orientation-dependent in a MOSFET.

- (100) surface is good for N-MOSFET performance.
- (110) surface is good for P-MOSFET performance.
Inversion Thickness in FinFETs

- Electrons: (100) sidewall provides the smallest $T_{\text{inv}}$
- Holes: (110) sidewall provides the smallest $T_{\text{inv}}$
- Production FinFETs are oriented with (110) sidewalls and <110> channel directions. → P-FinFETs should show better electrostatic integrity than N-FinFETs, with the same geometry/doping.
Threshold Voltage Dependence on Si Body Thickness

- Quantum confinement creates strong sub-band energy splitting, causing reduced DOS and enhanced threshold voltage, apparently.
- For UTB SOI MOSFETs, the critical body thickness appears at ~4nm.
- For FinFETs, the critical fin width appears <10nm.
Recalculation of $E_{\text{eff}}$ in Thin-Body MOSFETs: Single Channel

- By taking into account the bottom surface electric field, universal mobility curves can be generalized to thin-body MOSFETs.
- Quantum confinement effects (i.e. induced sub-band splitting) play an important role in determining $E_{\text{eff}}$.

\[ E_{\text{eff}} = \frac{Q_{\text{dep}} + \eta Q_{\text{inv}}}{\varepsilon_{\text{Si}}} + \frac{\varepsilon_{\text{OX}}}{\varepsilon_{\text{Si}}} \frac{V_{\text{BG}}}{t_{\text{BOX}}} \]

Extension of Universal Mobility Curves to Double Channel MOSFETs

- **FinFET:**
  \( E_{\text{eff}} \) is largely reduced due to the symmetric double gate coupling.

- **UTBB SOI MOSFET:**
  \( E_{\text{eff}} \) can be extended to negative direction if the bottom channel is turned on.

H. Yoshimoto, IEDM (2007)
Thin-Body MOSFET’s Carrier Scatterings: Electrons

As $T_{Si}$ decreases:
- Average effective mass // current:
  - (100): (110):
- Inter-valley scattering rates:
- Intra-valley scattering rates:
Experimental Results on Electron Mobility vs. Si Body Thickness

Si Experimental Data

- (100) surface: electron mobility first degrades with reducing $T_{Si}$, until $\sim 3.5$nm where appears a “bump” region.
- (110) surface: electron mobility keeps degrading with reducing $T_{Si}$.

K. Uchida, IEDM (2008)
Thin-Body MOSFET’s Carrier Scatterings: Holes

Wavefunction Overlap Integral

- (001) surface: hole mobility keeps degrading with reducing $T_{Si}$.
- (110) surface: hole mobility first degrades with reducing $T_{Si}$, then increases from decreased $m^*$ and slowly-growing form factor.

Average Transport $m^*$

L. Donetti, SSE (2010)

Impacts of Fin Orientation and Thickness on FinFET Carrier Mobility

M. Poljak, ESSDERC (2010)

N-FinFET (Electrons)

P-FinFET (Holes)

M. Poljak, ESSDERC (2010)
Experimental Results on FinFET Carrier Mobility vs. Fin Orientations

- **P-FinFETs:** expt. agree with simu. trends.
- **N-FinFETs:** (100) and (110) sidewalls show comparable electron mobility values, which is different to planar or simu. Trends.
  → likely due to sub-optimized fin sidewall roughness

J. Kavalieros, VLSI-T Short Course (2008)

C. D. Young, SSE (2012)
High-κ-induced Scatterings in Thin-Body MOSFETs

Interface Charge-induced scattering potentials

F. Driussi, TED (2009)

\[ \phi_{\text{unschr}}(\vec{q}, z) = \frac{e}{\vec{q}(\varepsilon_{\text{Si}} + \varepsilon_{\text{ox}})} e^{-\vec{q}|z|} \]

\[ M_{n,n'}(\vec{q}, z_0) = \frac{e}{A} \int_{0}^{\infty} \phi(\vec{q}, z, z_0) \xi_n(z) \xi_{n'}(z) dz \]
FinFETs vs. Planar UTB MOSFETs
Carrier Mobility in Scaled Nodes

NMOS: Electron Mobility

PMOS: Hole Mobility

Techbar Node:
20nm
14/16nm
10/12nm

Unstrained
Longi.
Trans.
Vertical

N. Xu, EDL (2012)
Source/Drain Series Resistance ($R_{S/D}$) in Short-$L_g$ MOSFETs

$I_D = \frac{I_{D0}}{1 + \frac{I_{D0}R_s}{(V_{GS} - V_T)}}$

D. Fleury, VLSI-T (2009)

22nm-$L_{eff}$ Bulk N-MOSFET

$R_{sd} \approx 107 - 32V_{gs}$ (Ω.µm)

J. Kavalieros, VLSI-T (2006)

Tri-Gate MOSFET

D. Fleury, VLSI-T (2009)

J. Kavalieros, VLSI-T (2006)
Quasi-Ballistic Transport

After M. Lundstrom (Purdue Univ.)

**Diffusive Limit (Long-Channel)**

$L >> \lambda$

(Mean Free Path)

**Ballistic Limit (nm-Channel)**

$L << \lambda$

Carrier’s thermal injection velocity (w/o scatterings)

$$v_{inj} = \sqrt{\frac{2k_BT}{\pi m^*}} \frac{\zeta_{1/2}(\eta_F)}{\zeta_0(\eta_F)}$$

Drain current

$$I_{DS} = C_{ox} (V_{GS} - V_T) v_T \left( \frac{1 - e^{-qV_{DS}/k_BT}}{1 + e^{-qV_{DS}/k_BT}} \right)$$

Under small $V_{DS}$

$$I_{DS} = WC_{ox} \frac{v_T}{2k_BT/q} (V_{GS} - V_T)V_{DS}$$

The “ballistic mobility”

$$\mu_B = \left[ \frac{v_T L}{2k_BT/q} \right]$$

The total channel mobility

$$\frac{1}{\mu} = \frac{1}{\mu_{drift}} + \frac{1}{\mu_{bal}}$$
Apparent Carrier Mobility

Si Bulk MOSFET

\[ \frac{1}{\mu_{\text{bal}}} = \frac{1}{\mu_{\text{exp}}} - \frac{1}{\mu_{\text{bal}}} \]

*V. Cros, IEDM (2007)

Illustration for HALO-induced S/D Edge Defects

Si UTBB SOI MOSFET

*V. Xu, VLSI-T (2011)

Extracted interface trap distribution in a High-\(\kappa\) MOSFET

*C. C. Lu, SSE (2010)
Diffusive vs. Ballistic Transport: Where We Are?

Modeling for nano-$L_g$ MOSFET Current

\[ v_T = \frac{2k_BT}{\pi \eta k_BT} \left( \frac{F_{1/2}(\eta)}{\ln(1 + e^\eta)} \right), \eta = \frac{E_F - E_C}{k_BT} \]  
\[ v_{inj} = v_T \times (1-r)/(1+r) \]  
\[ I_{don} = W^L \mu_{dd} V_{gs} Q_s \]  
\[ I_{ddlin} = W^L \mu_{dd} V_{ds} \frac{Q_s}{L} \]  
\[ I_{balin} = W^L v_{inj} Q_s \]  
\[ I_{lim} = W^L v_{inj} Q_s \frac{qV_{ds}}{2k_BT} \]  
\[ I_{sat} = W^L v_{sat} Q_s \]  
\[ 1/I_d = 1/I_{dd} + 1/\min(I_{bal}, I_{sat}) \]  
\[ v_{lim} = \min(v_{sat}, v_{inj}) \]  
\[ \frac{\partial}{\partial V_{gs}} \left( \frac{L}{\mu_{on}} - \frac{L}{\mu_{lim}} \right) = \frac{1}{v_{lim}} \]  

Measurement from 22nm-$L_{eff}$ Bulk N-MOSFET

\[ \frac{\partial}{\partial V_{gs}} \left( \frac{L}{\mu_{on}} - \frac{L}{\mu_{lim}} \right) = \frac{1}{v_{lim}} \]  
\[ \frac{\mu_{on}}{L} = \frac{I_{don}}{WQ_s V_{gs}} \]  
\[ \frac{\mu_{lim}}{L} = \frac{I_{ddlin}}{WQ_s V_{ds}} \]  
\[ v_{lim} = \frac{1}{v_{inj}} \text{ or } \frac{1}{v_{sat}} \]  

D. Fleury, VLSI-T (2009)

- Consider drift, saturation and thermal injection velocities.
- The limiting velocity shows negative dependence vs. temperature, indicating its drift (or saturation) nature.

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Nuo Xu EE 290D, Fall 2013
References


References


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