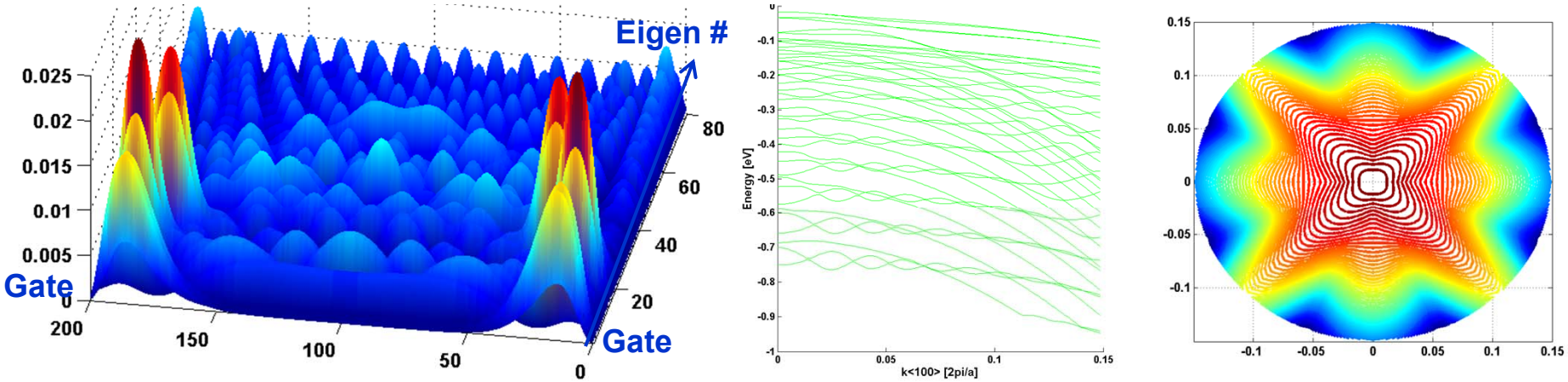


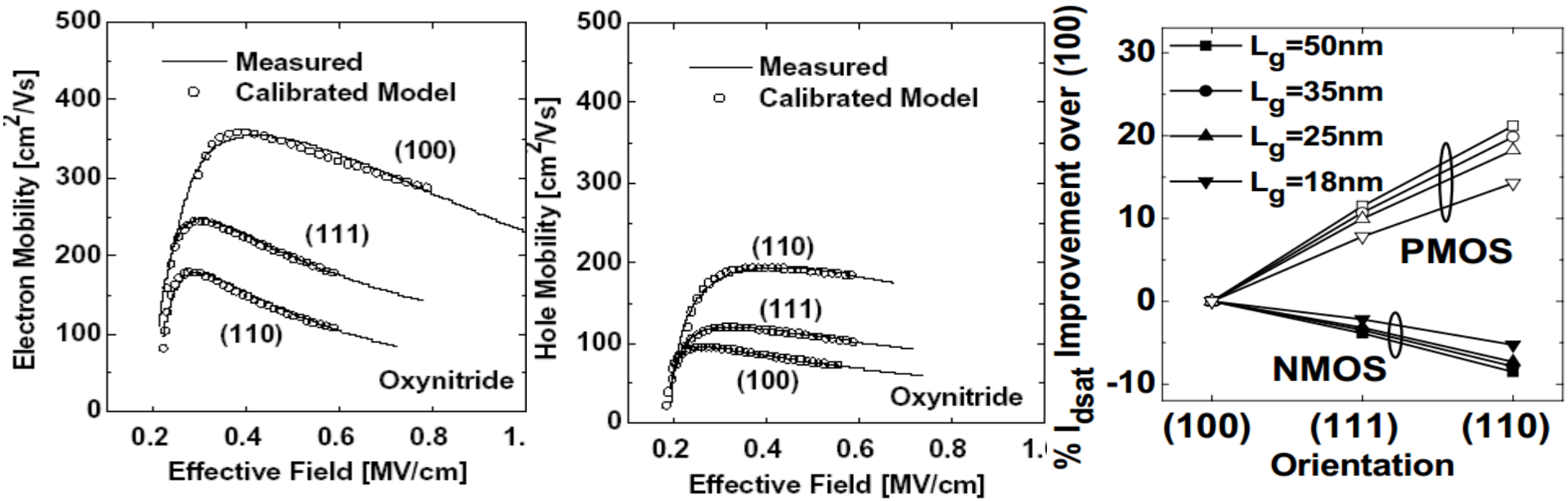
Hole's Wavefunctions, *E-k* and Equi-Energy Contours from a P-FinFET

Lecture 5

- Thin-Body MOSFET Carrier Transport
  - quantum confinement effects
  - low-field mobility: Orientation and Si Thickness Dependence
- Non-Idealities in Nano-Scale L_g MOSFET Transport
  - Quasi-Ballistic Transport
  - Apparent Mobility
  - Series Resistance

Reading:
- multiple research articles (reference list at the end of this lecture)

Orientation Dependence of Inversion Thickness and Carrier Mobility

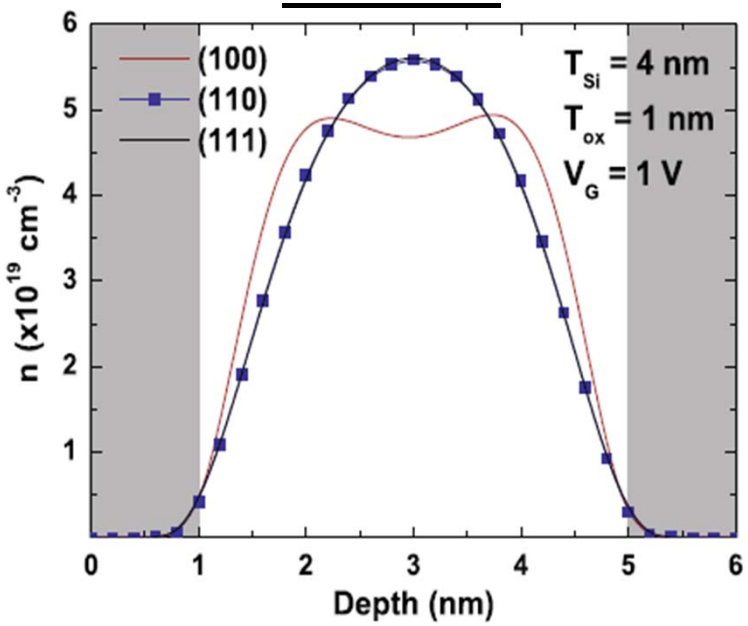


L. Chang, TED (2004)

- Due to the anisotropic *E-k* relationships, quantum confinement and carrier mobility are surface orientation-dependent in a MOSFET.
- (100) surface is good for N-MOSFET performance.
- (110) surface is good for P-MOSFET performance.

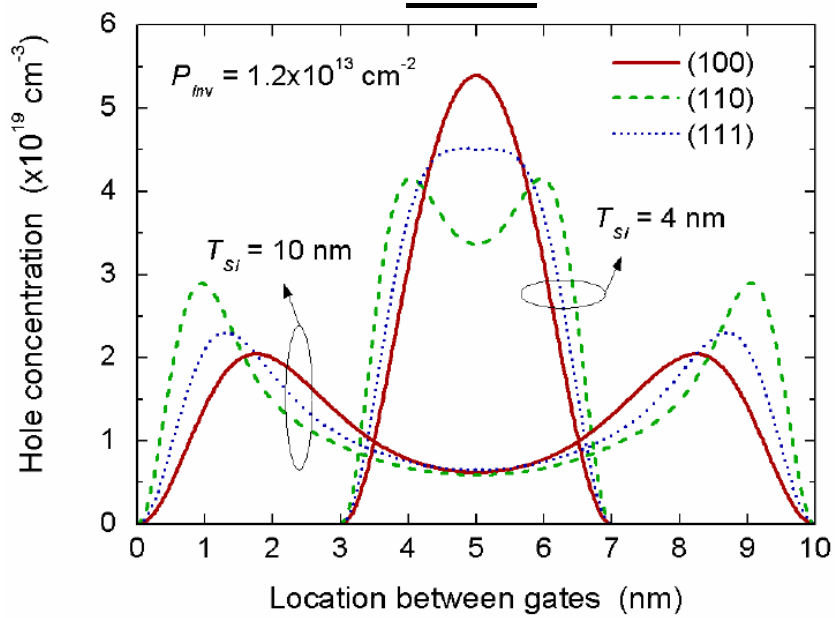
Inversion Thickness in FinFETs

Electrons



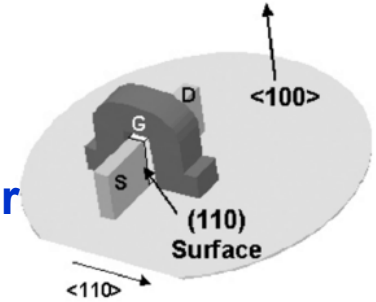
N. Samedro, SSE (2010)

Holes



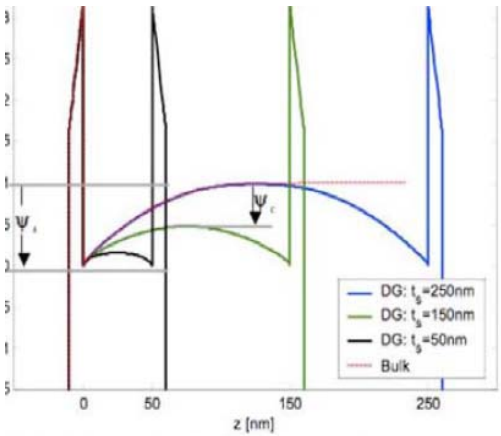
M. Poljak, ESSDERC (2010)

- **Electrons: (100) sidewall provides the smallest T_{inv}.**
- **Holes: (110) sidewall provides the smallest T_{inv}.**
- **Production FinFETs are oriented with (110) sidewalls and <110> channel directions. → P-FinFETs should show better electrostatic integrity than N-FinFETs, with the same geometry/doping.**



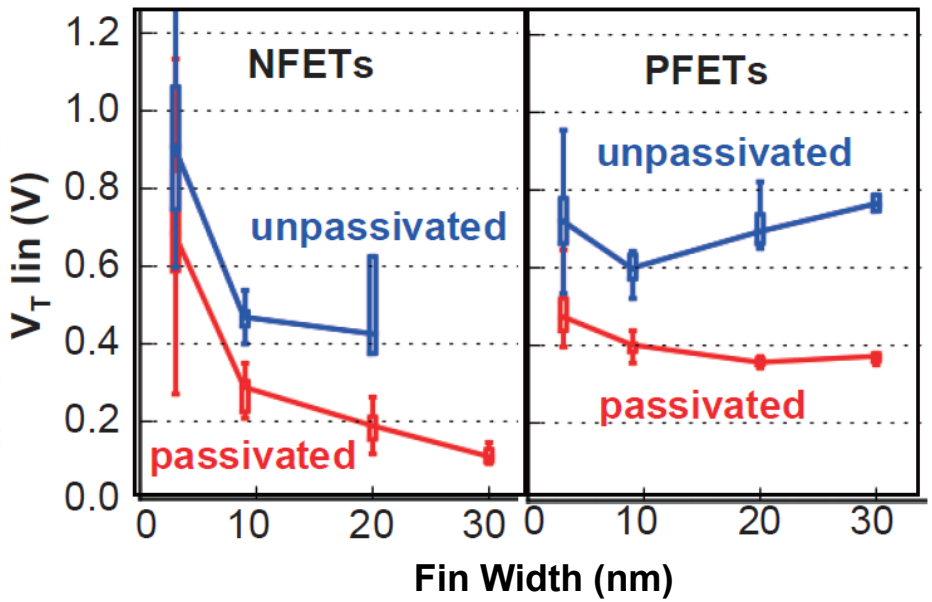
Threshold Voltage Dependence on Si Body Thickness

Electrical and Geometrical Confinement



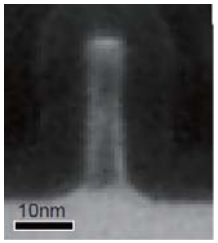
Extreme case:

$$E_{n-1} = \frac{\hbar^2}{2m^*}\left(\frac{n\pi}{t_{SOI}}\right)^2$$

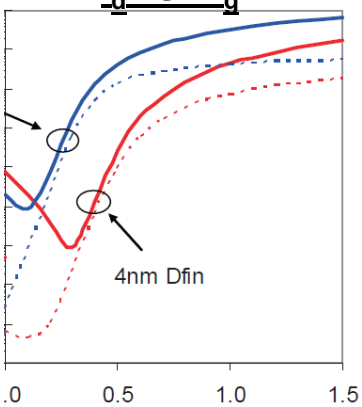


J. B. Chang, VLSI-T (2011)

TEM

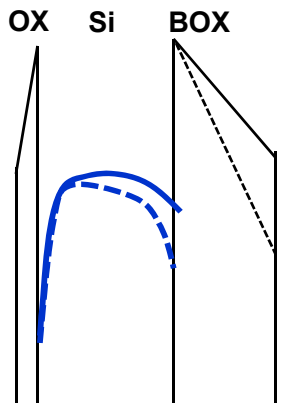


I_d vs. V_g

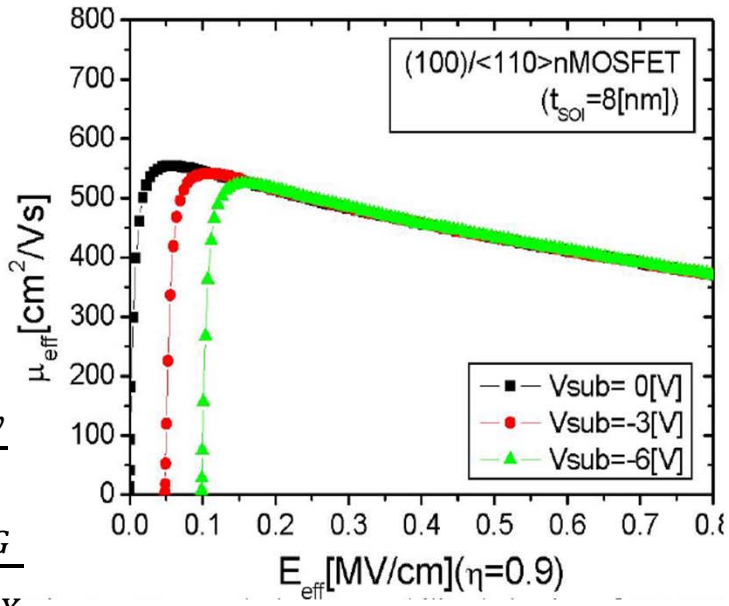


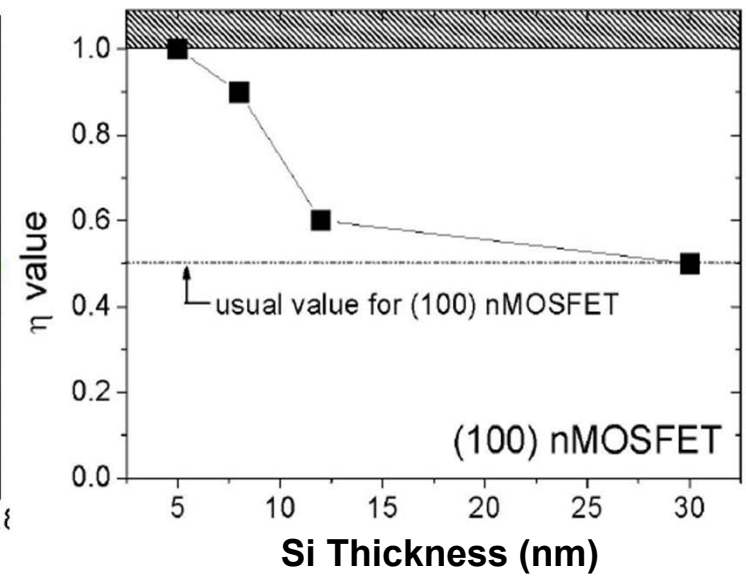
- **Quantum confinement creates strong sub-band energy splitting, causing reduced DOS and enhanced threshold voltage, apparently.**
- **For UTB SOI MOSFETs, the critical body thickness appears at ~4nm.**
- **For FinFETs, the critical fin width appears <10nm.**

Recalculation of E_{eff} in Thin-Body MOSFETs: Single Channel



$$E_{eff} = \frac{Q_{dep} + \eta Q_{inv}}{\varepsilon_{Si}} + \frac{\varepsilon_{OX}}{\varepsilon_{Si}} \cdot \frac{V_{BG}}{t_{BOX}}$$





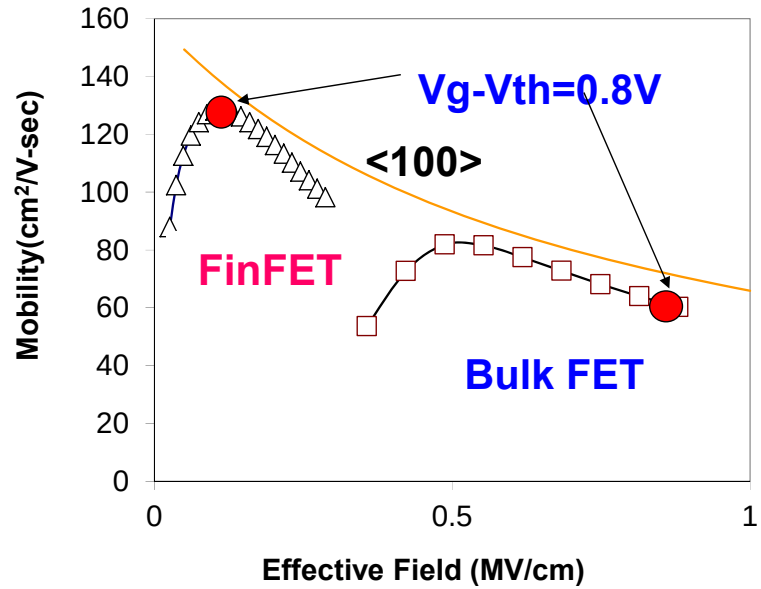
K. Shimizu, SOI (2006)

- By taking into account the bottom surface electric field, universal mobility curves can be generalized to thin-body MOSFETs.
- Quantum confinement effects (*i.e.* induced sub-band splitting) play an important role in determining E_{eff}.

Extension of Universal Mobility Curves to Double Channel MOSFETs

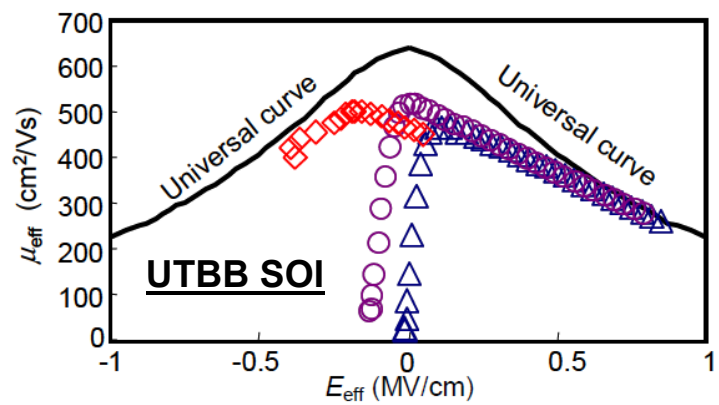
- **FinFET:**

E_{eff} is largely reduced due to the symmetric double gate coupling.



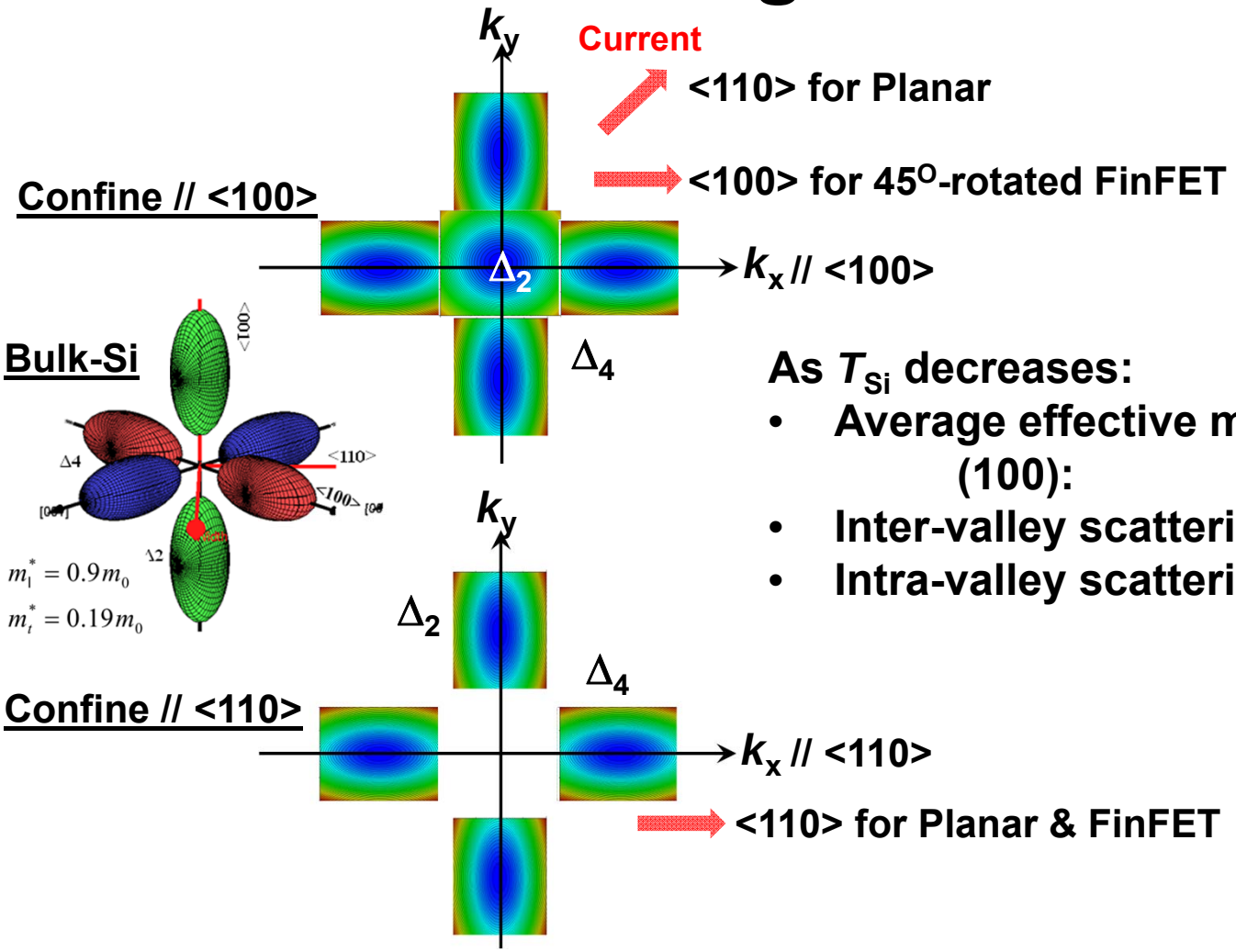
- **UTBB SOI MOSFET:**

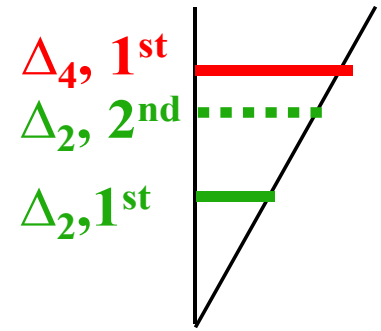
E_{eff} can be extended to negative direction if the bottom channel is turned on.



H. Yoshimoto, IEDM (2007)

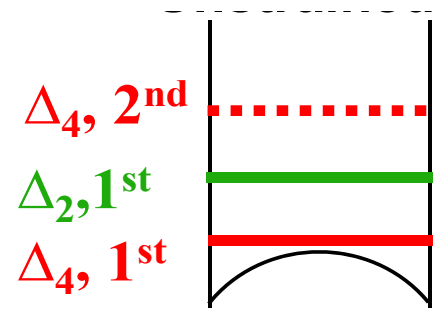
Thin-Body MOSFET's Carrier Scatterings: Electrons





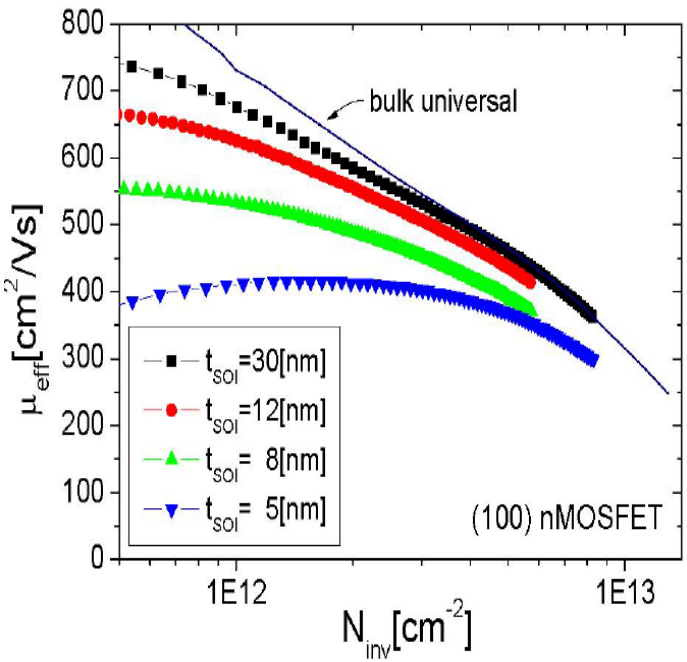
As T_{Si} decreases:

- Average effective mass // current:
  (100): (110):
- Inter-valley scattering rates:
- Intra-valley scattering rates:

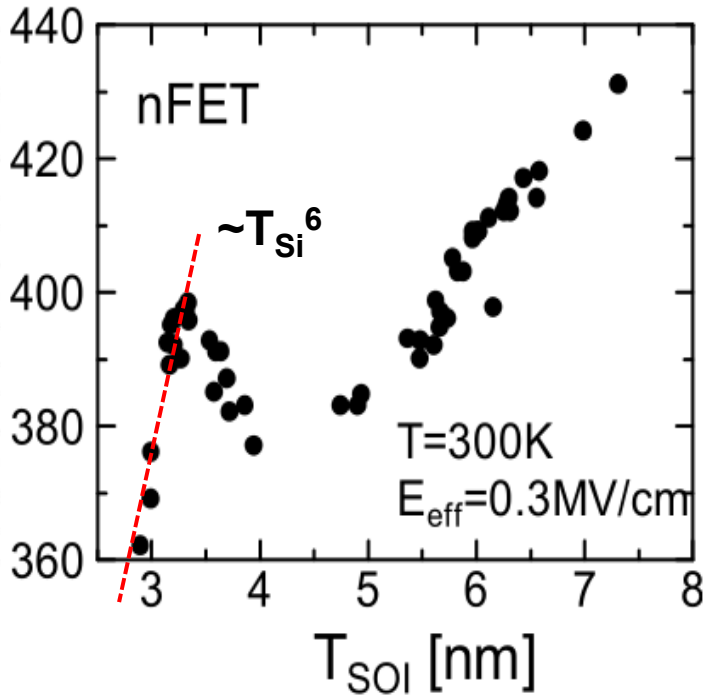


Experimental Results on Electron Mobility *vs*. Si Body Thickness

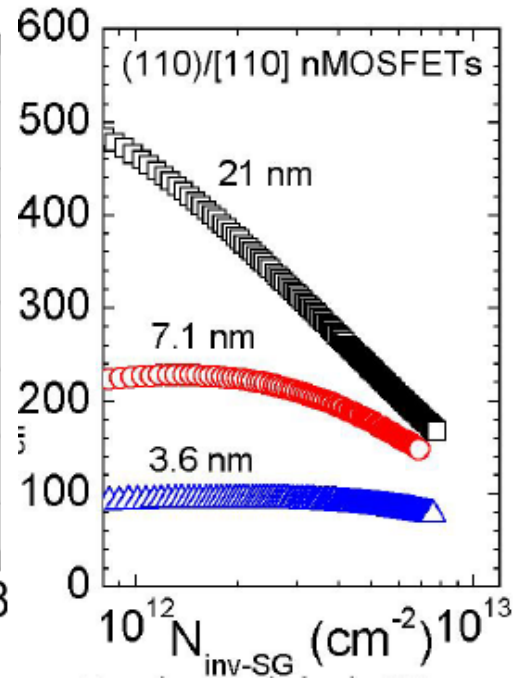
Si Experimental Data



K. Shimizu, SOI (2006)



K. Uchida, IEDM (2008)

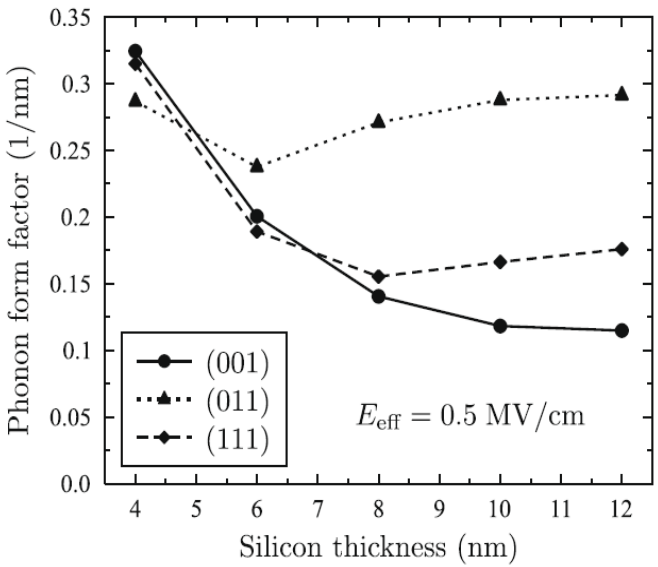


K. Shimizu, IEDM (2007)

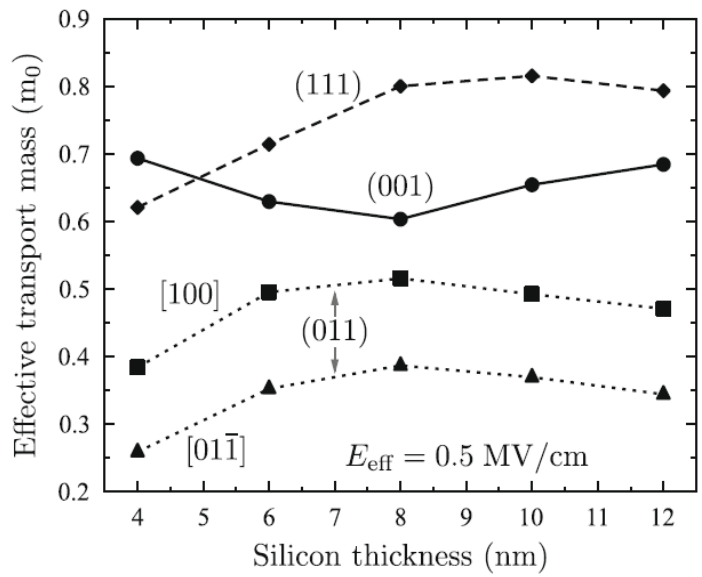
- **(100) surface: electron mobility first degrades with reducing T_{Si}, until ~3.5nm where appears a "bump" region.**
- **(110) surface: electron mobility keeps degrading with reducing T_{Si}.**

Thin-Body MOSFET's Carrier Scatterings: Holes

Wavefunction Overlap Integral

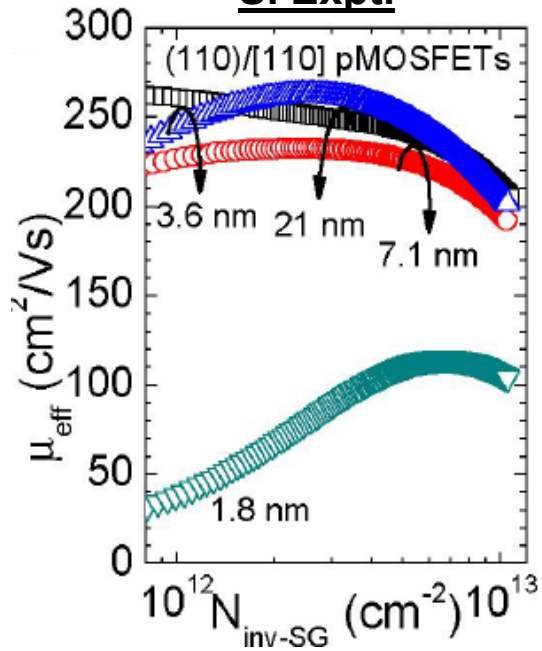


Average Transport m*



L. Donetti, SSE (2010)

Si Expt.



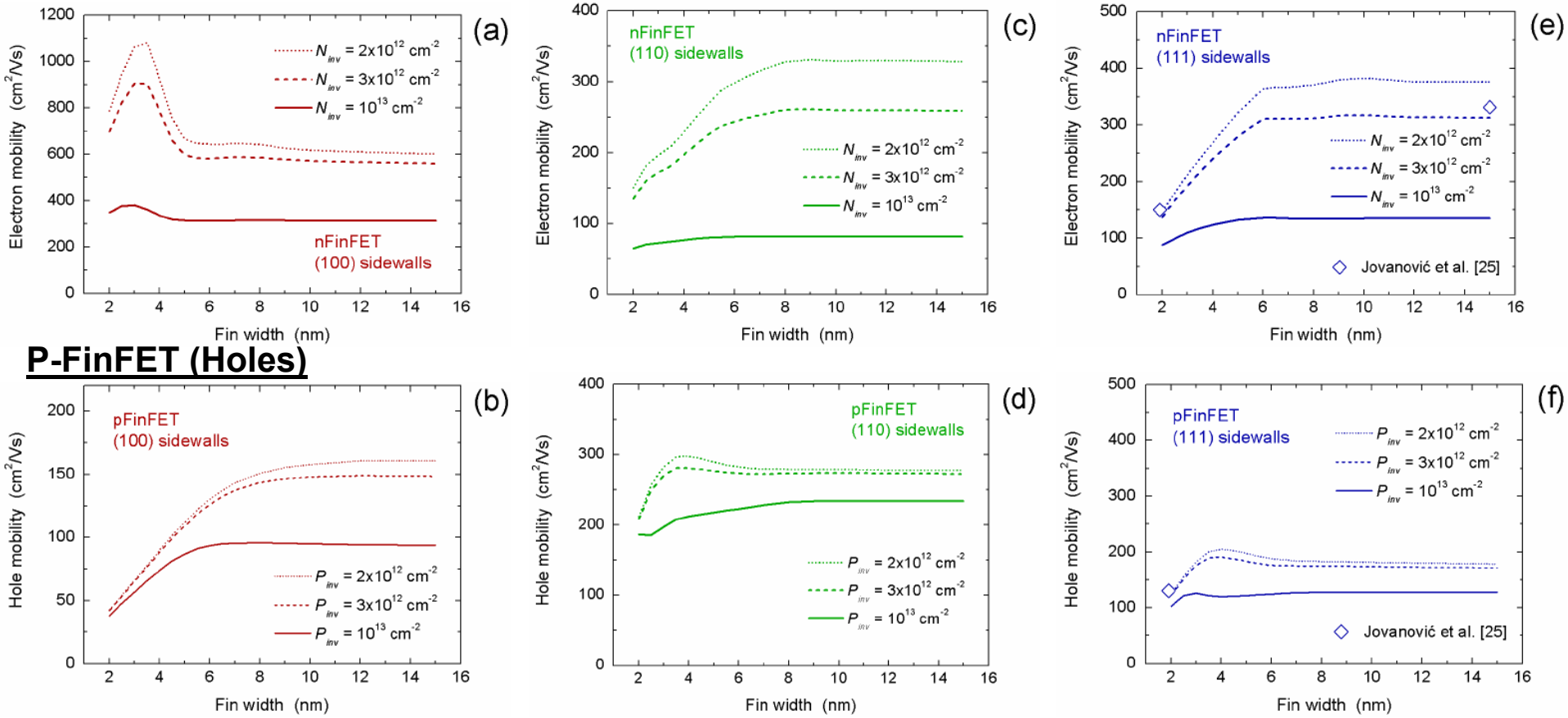
K. Shimizu, IEDM (2007)

- **(100) surface: hole mobility keeps degrading with reducing T_{Si}.**
- **(110) surface: hole mobility first degrades with reducing T_{Si}, then increases from decreased m* and slowly-growing form factor.**

Impacts of Fin Orientation and Thickness on FinFET Carrier Mobility

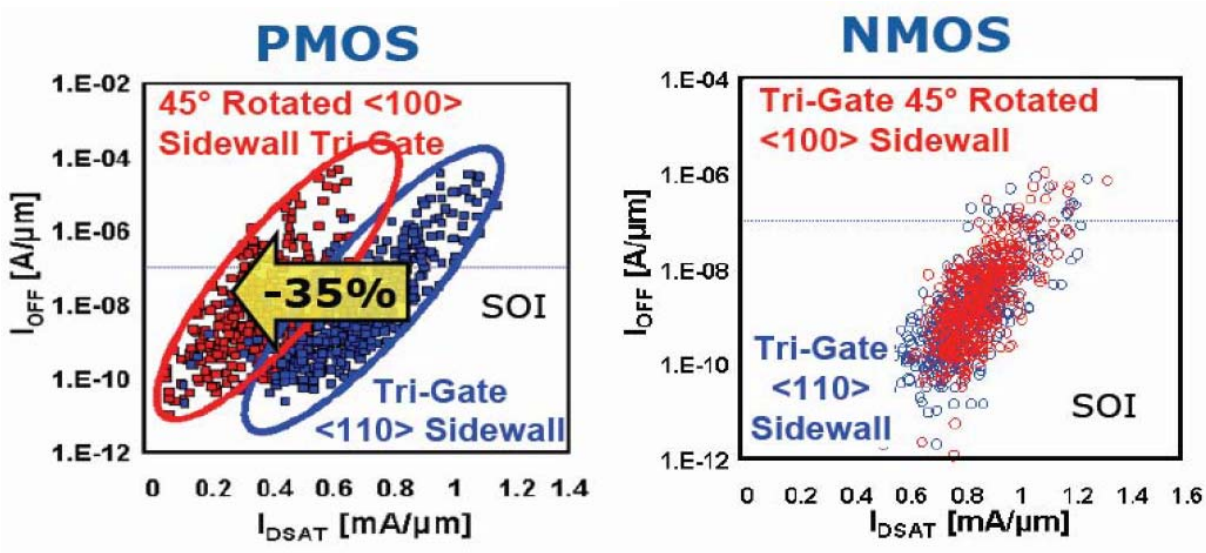
N-FinFET (Electrons)

P-FinFET (Holes)



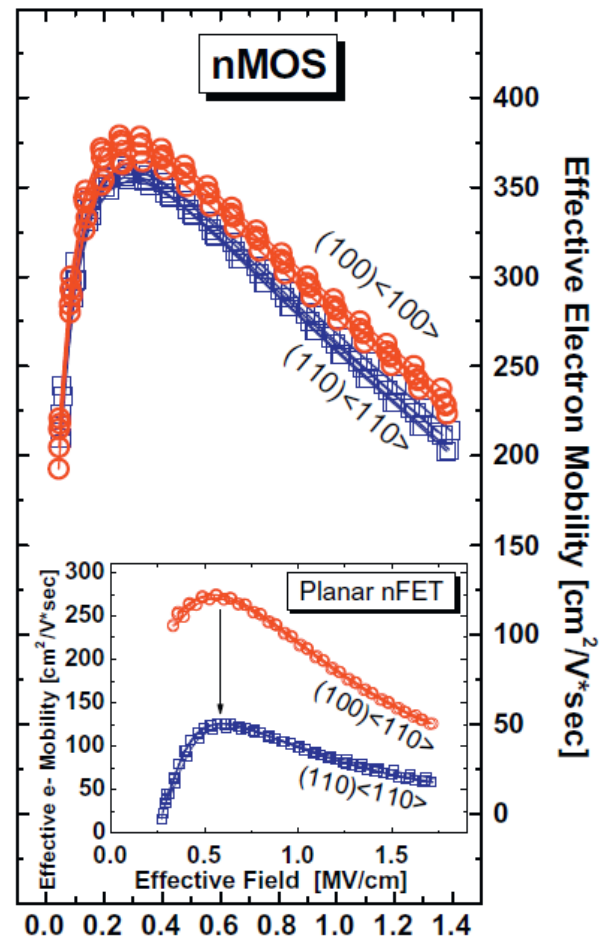
M. Poljak, ESSDERC (2010)

Experimental Results on FinFET Carrier Mobility *vs*. Fin Orientations



J. Kavalieros, VLSI-T Short Course (2008)

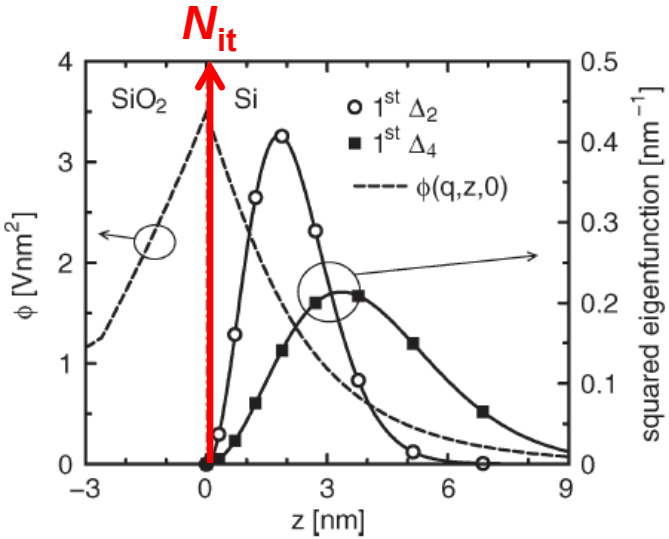
- **P-FinFETs: expt. agree with simu. trends.**
- **N-FinFETs: (100) and (110) sidewalls show comparable electron mobility values, which is different to planar or simu. Trends.**
  → likely due to sub-optimized fin sidewall roughness



C. D. Young, SSE (2012)

High-κ-induced Scatterings in Thin-Body MOSFETs

Interface Charge-induced scattering potentials

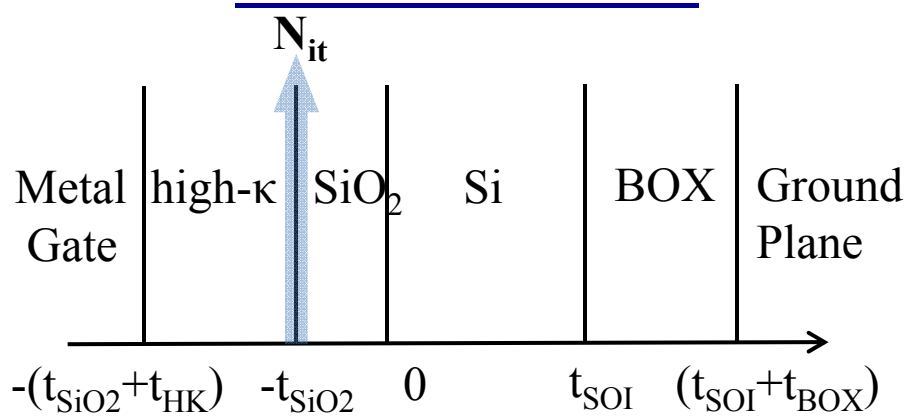


F. Driussi, TED (2009)

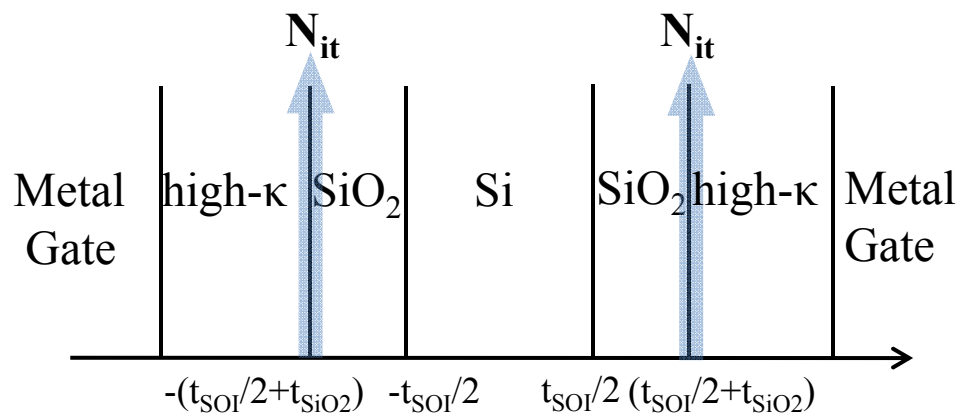
$$\phi_{unscr}(\vec{q},z) = \frac{e}{\vec{q}(\varepsilon_{Si}+\varepsilon_{ox})} e^{-\vec{q}|z|}$$

$$M_{n,n'}(\vec{q},z_0) = \frac{e}{A}\int_0^{\infty} \phi(\vec{q},z,z_0)\,\xi_n(z)\xi_{n'}(z)dz$$

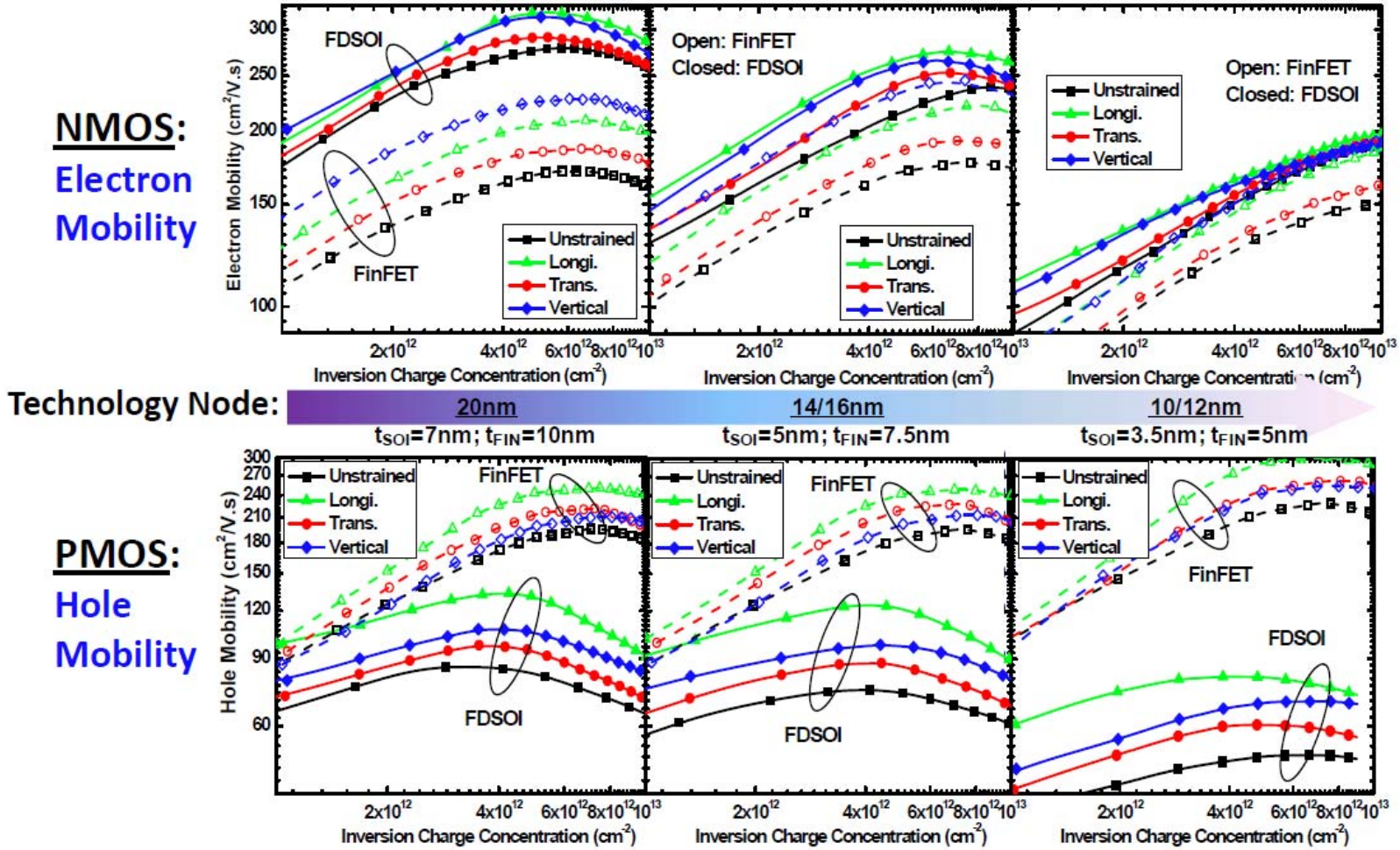
Planar UTB MOSFET



Double-gate FinFET

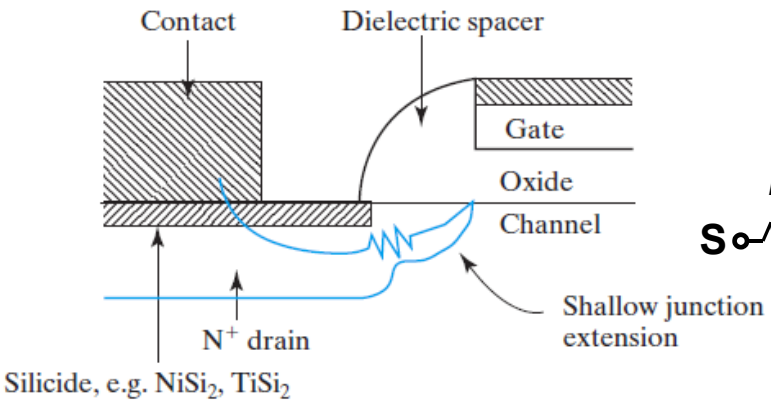


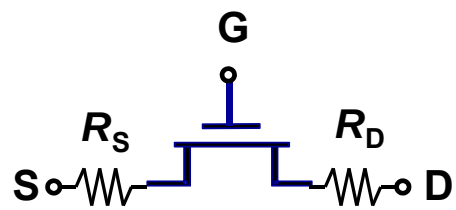
FinFETs *vs*. Planar UTB MOSFETs Carrier Mobility in Scaled Nodes



N. Xu, EDL (2012)

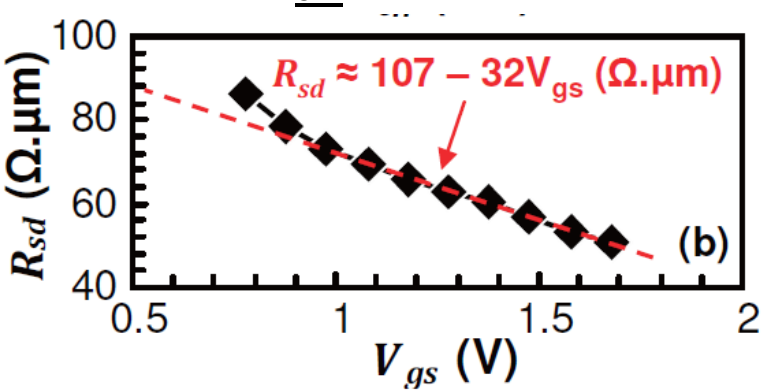
Source/Drain Series Resistance ($R_{S/D}$) in Short-L_g MOSFETs





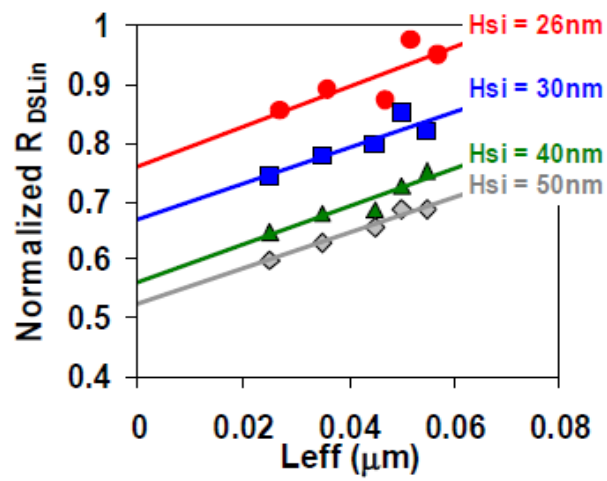
$$I_D = \frac{I_{D0}}{1 + \frac{I_{D0} R_s}{(V_{GS} - V_T)}}$$

22nm-L_{eff} Bulk N-MOSFET



D. Fleury, VLSI-T (2009)

Tri-Gate MOSFET



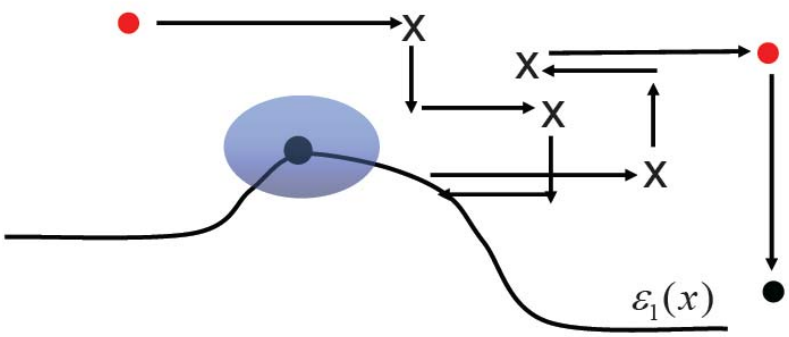
J. Kavalieros, VLSI-T (2006)

Quasi-Ballistic Transport

After M. Lundstrom (Purdue Univ.)

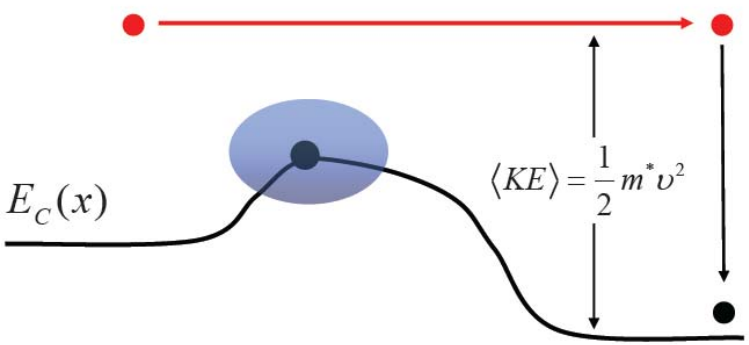
Diffusive Limit (Long-Channel)

$L >> \lambda$ **(Mean Free Path)**



Ballistic Limit (nm-Channel)

$L << \lambda$



Carrier's thermal injection velocity (w/o scatterings)

$$v_{inj} = \sqrt{\frac{2k_B T}{\pi m^*} \frac{\Im_{1/2}(\eta_F)}{\Im_0(\eta_F)}}$$

Drain current

$$I_{DS} = C_{ox}\left(V_{GS} - V_T\right)\upsilon_T \left(\frac{1 - e^{-qV_{DS}/k_B T}}{1 + e^{-qV_{DS}/k_B T}}\right)$$

Under small V_{DS}

$$I_{DS} = WC_{OX} \frac{\upsilon_T}{2k_B T/q}\left(V_{GS} - V_T\right)V_{DS}$$

The "ballistic mobility"

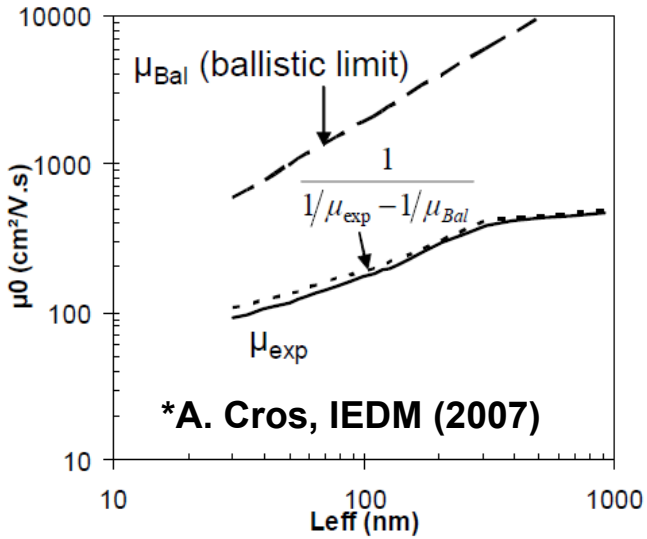
$$\mu_B \equiv \left[\frac{\upsilon_T L}{2k_B T/q}\right]$$

The total channel mobility

$$\frac{1}{\mu} = \frac{1}{\mu_{drift}} + \frac{1}{\mu_{bal}}$$

Apparent Carrier Mobility

Si Bulk MOSFET



Si UTBB SOI MOSFET

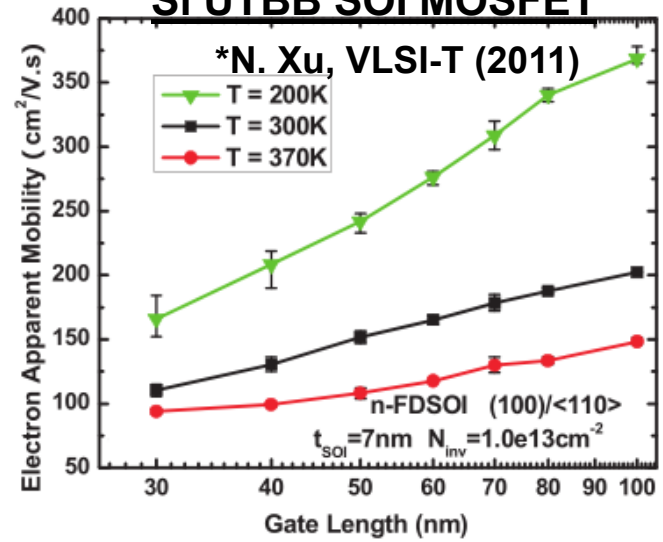
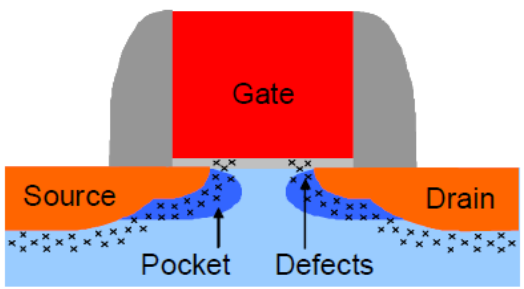
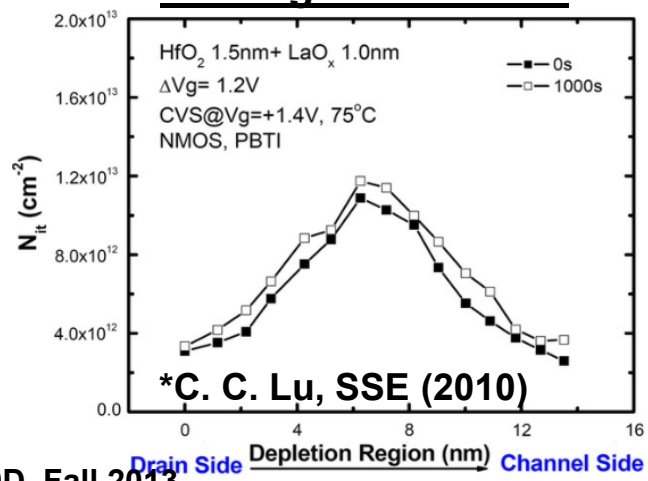


Illustration for HALO-induced S/D Edge Defects



Extracted interface trap distribution in a High-κ MOSFET

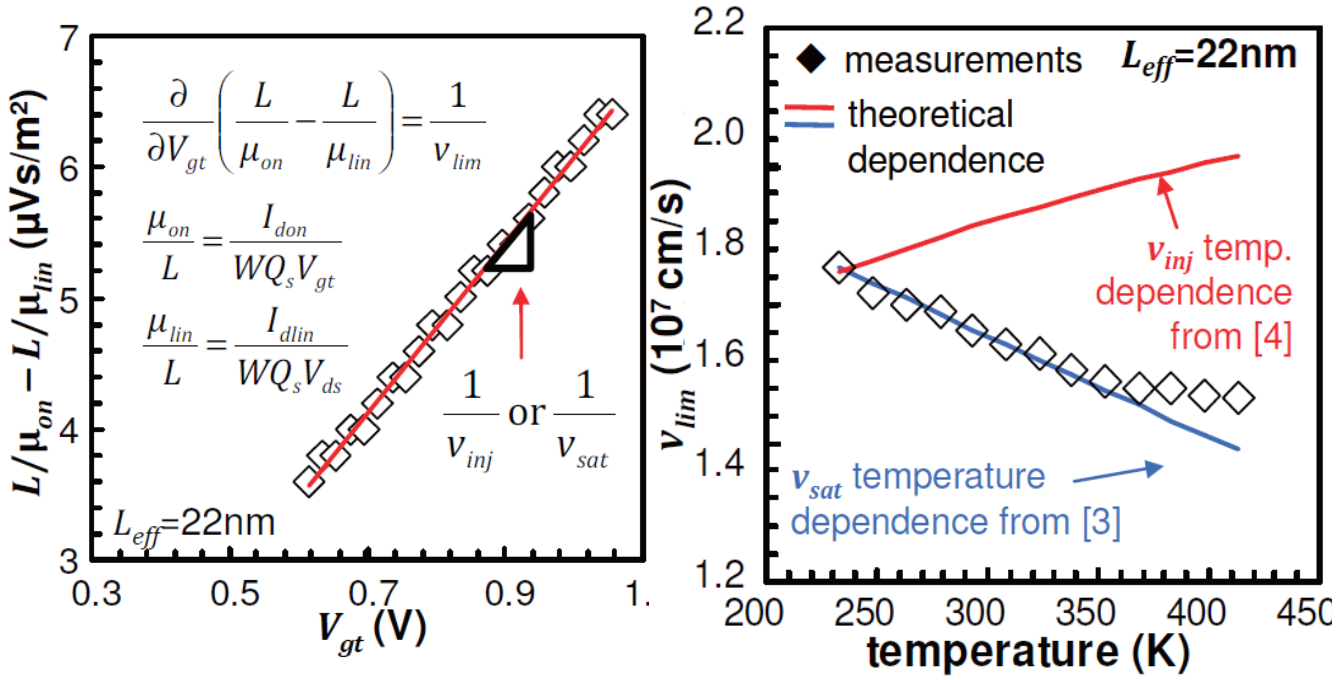


Diffusive *vs*. Ballistic Transport: Where We Are?

Modeling for nano-L_g MOSFET Current

$v_T = \sqrt{\frac{2k_BT}{\pi m_t^*}\left\{\frac{F_{1/2}(\eta)}{\ln(1+e^{\eta})}\right\}}, \eta = \frac{E_F\text{-}E_C}{k_BT}$		(1)
$v_{inj} = v_T \times (1-r)/(1+r)$		(2)
$I_{ddon} = W\frac{\mu_{dd}V_{gt}}{L}Q_s$	(3)	$I_{ddlin} = W\frac{\mu_{dd}V_{ds}}{L}Q_s$ (4)
$I_{balon} = Wv_{inj}Q_s$	(5)	$I_{ballin} = Wv_{inj}Q_s\frac{qV_{ds}}{2k_BT}$ (6)
$I_{sat} = Wv_{sat}Q_s$		(7)
$1/I_d = 1/I_{dd} + 1/\min(I_{bal}, I_{sat})$		(8)
$v_{lim} = \min(v_{sat}, v_{inj})$		(9)
$\frac{\partial}{\partial V_{gt}}\left(\frac{L}{\mu_{on}} - \frac{L}{\mu_{lin}}\right) = \frac{1}{v_{lim}}$		(10)

Measurement from 22nm-L_{eff} Bulk N-MOSFET



D. Fleury, VLSI-T (2009)

- **Consider drift, saturation and thermal injection velocities.**
- **The limiting velocity shows negative dependence *vs*. temperature, indicating its drift (or saturation) nature.**

References

1. J. B. Chang, M. Guillorn, P. M. Solomon, C.-H. Lin, S. U. Engelamnn, *et al*., "Scaling of SOI FinFETs Down to Fin Width of 4 nm for the 10 nm Technology Node," *Symposium on VLSI Technology Digest*, pp. 12-13, 2011.
2. K. Shimizu, G. Tsutsui, T. Hiramoto, "Experimental Study on Mobility Universality in (100) Ultra Thin Body nMOSFET with SOI Thickness of 5nm," *IEEE SOI Conference Digest*, pp. 159-160, 2006.
3. H. Yoshimoto, N. Sugii, D. Hisamoto, S. Saito, R. Tsuchiya, S. Kimura, "Extension of Universal Mobility Curve to Multi-Gate MOSFETs," *IEEE International Electron Device Meeting Tech. Digest*, pp. 703-706, 2007.
4. K. Shimizu, T. Hiramoto, "Mobility Enhancement in Uniaxially Strained (110) Oriented Ultra-Thin Body Single- and Double-Gate MOSFETs with SOI Thickness of Less Than 4 nm," *IEEE International Electron Device Meeting Tech. Digest*, pp. 715-718, 2007.
5. K. Uchida, M. Saitoh, S. Kobayashi, "Carrier Transport and Stress Engineering in Advanced Nanoscale Transistors From (100) and (110) Transistors to Carbon Nanotube FETs and Beyond," *IEEE International Electron Device Meeting* Tech. Digest, 2008.
6. L. Donetti, F. Gamiz, N. Rodriguez, F. Jimenez-Molinos, J. B. Roldan, "Hole Transport in DG SOI Devices: Orientation and Silicon Thickness Effects," *Solid-State Electronics*, Vol.54, pp.191-195, 2010.
7. M. Poljak, T. Suligoj, V. Jovanovic, "Modeling Study on Carrier Mobility in Ultra-Thin Body FinFETs with Circuit-Level Implications," *the* 36th *European Solid-State Device Research Conference (ESSDERC) Digest*, pp. 242-245, 2010.

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