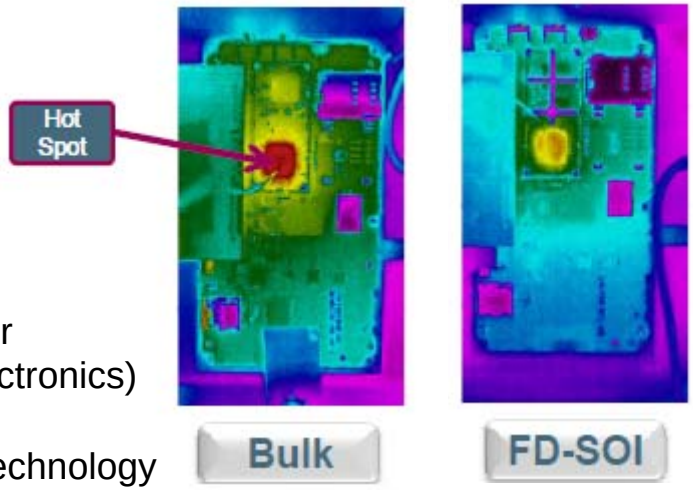
Courtesy of
L. Le Pailleur
(STMicroelectronics)



Live demo of *NovaThor*™ *L8580* – FDSOI Technology

Lecture 3

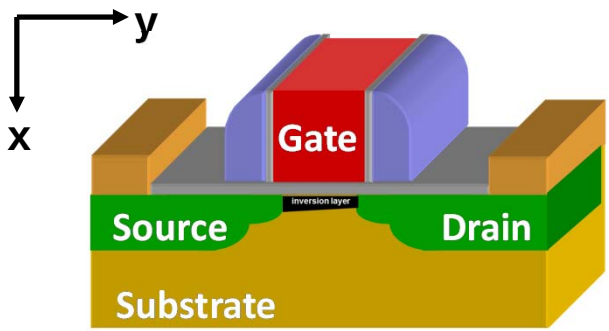
- Thin-Body MOSFET Electrostatics
  - Improved short-channel effect
  - Subthreshold Swing
  - Effective Drive Current (I_{EFF})

<u>Reading</u>:

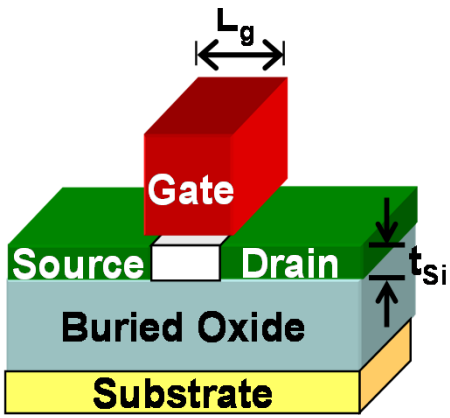
- multiple research articles (reference list at the end of this lecture)

Thin-Body MOSFET Electrostatics: *Qualitatively*

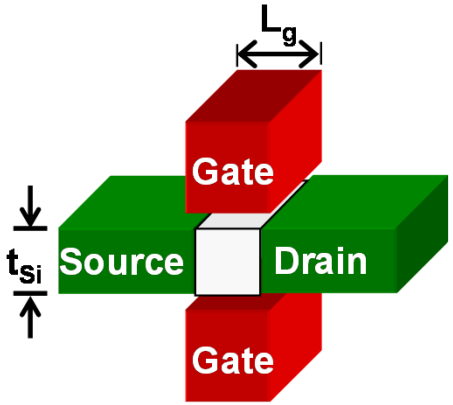
Planar Bulk FET



Ultra-Thin Body
Fully Depleted SOI
Extremely Thin SOI ...



FinFET



- **Potential Profiles along x:**

Planar Bulk MOSFET's Scale Length: *A More Rigorous Solving*

Steps:

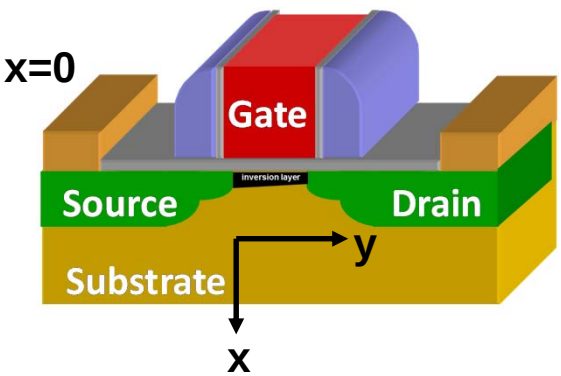
R.-H. Yan, T-ED (1992)

1. Solve 2-D Poisson's equation:

$$\frac{\partial^2\varphi}{\partial x^2}+\frac{\partial^2\varphi}{\partial y^2}=\frac{qN_A}{\varepsilon_{Si}}$$

with boundary conditions as:

$$\begin{cases}\dfrac{\partial\varphi}{\partial x}=-\dfrac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\dfrac{V_G-V_{FB}-\varphi}{t_{ox}} & \text{at } x=0\\[2ex] \dfrac{\partial\varphi}{\partial x}=0 & \text{beyond } X_{dep}\end{cases}$$



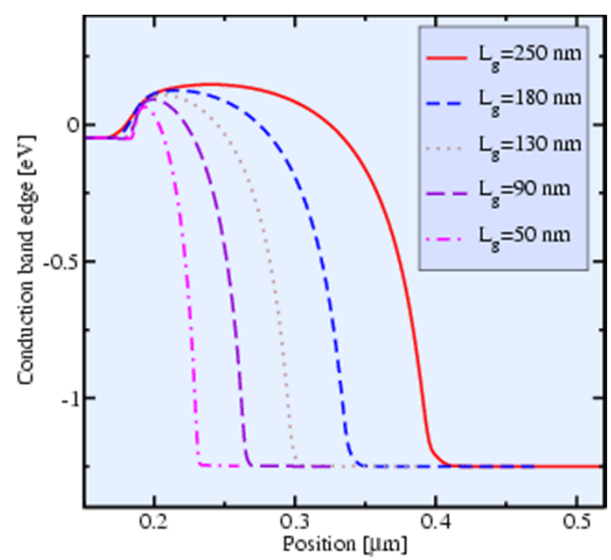
2. One can get parabolic potential profile along *x*:

$$\varphi(x,y)=\varphi(y)+A_1\big(\varphi(y)\big)\cdot x+A_2\big(\varphi(y)\big)\cdot x^2$$

3. Evaluate φ at surface:

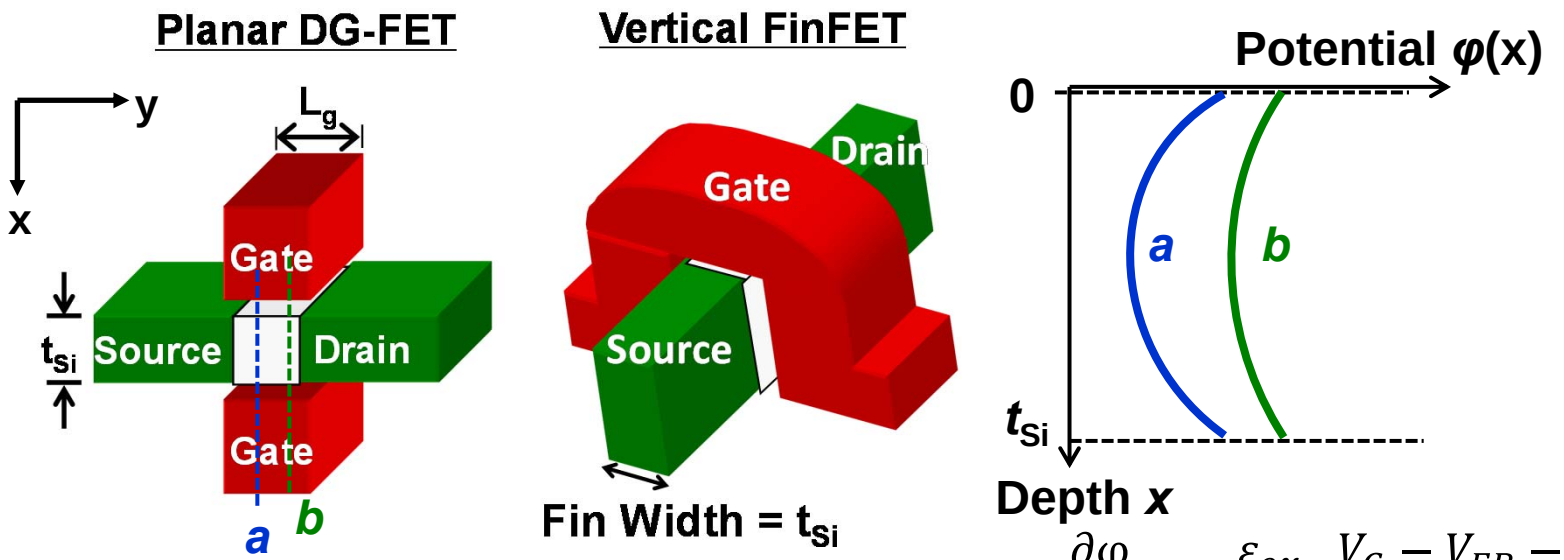
$$\frac{\partial^2\varphi}{\partial y^2}+\frac{V_G-V_{FB}-\varphi}{l^2}=\frac{qN_A}{\varepsilon_{Si}}$$

where $l=\sqrt{\dfrac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}X_{dep}}$ **is called the *Scale Length***



Double Gate FinFET

K. Suzuki, T-ED (1993)



1. Solve 2-D Poisson's equation:

$$\frac{\partial^2\varphi}{\partial x^2}+\frac{\partial^2\varphi}{\partial y^2}=\frac{qN_A}{\varepsilon_{Si}}$$ **with boundary conditions as:** $$\frac{\partial\varphi}{\partial x}=0 \text{ at } x=\frac{t_{Si}}{2}$$ $$\frac{\partial\varphi}{\partial x}=-\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{V_G-V_{FB}-\varphi}{t_{ox}} \text{ at } x=0,t_{Si}$$

2. Assume parabolic potential profile along *x*:

$$\varphi(x,y)=\varphi(y)+A_1\big(\varphi(y)\big)\cdot x+A_2\big(\varphi(y)\big)\cdot x^2$$

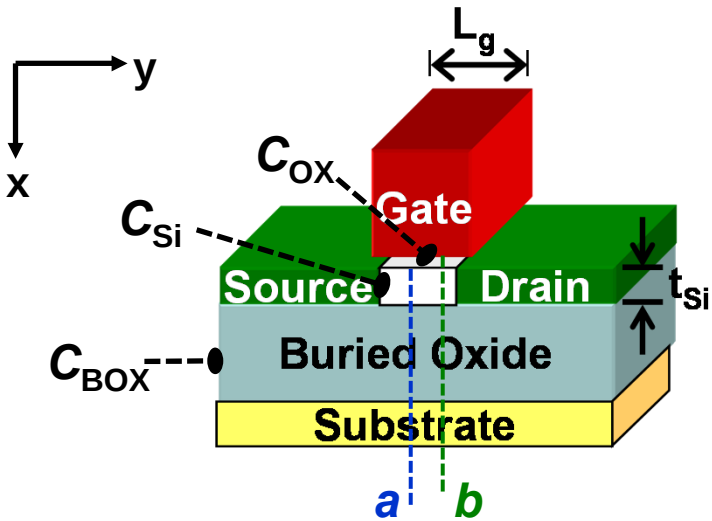
3. Evaluate φ at center of the fin by substituting $x=\frac{t_{Si}}{2}$:

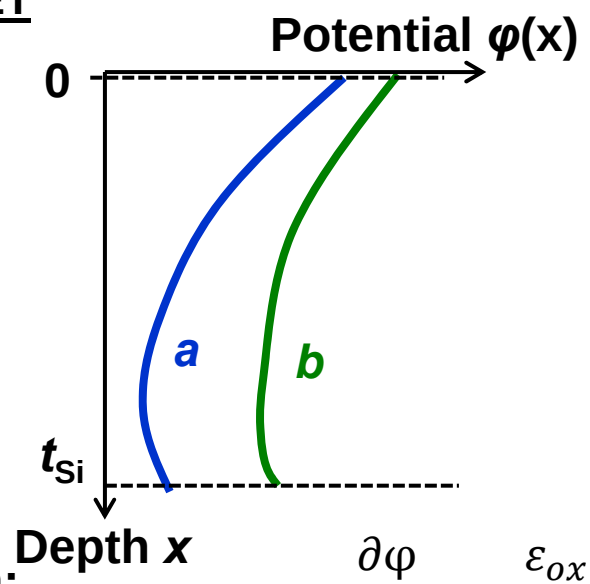
$$\frac{\partial^2\varphi_c}{\partial y^2}+\frac{V_G-V_{FB}-\varphi_c}{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}}t_{ox}t_{Si}(1+\frac{\varepsilon_{ox}}{4\varepsilon_{Si}}\cdot\frac{t_{Si}}{t_{ox}})}=\frac{qN_A}{\varepsilon_{Si}}$$

Planar Ultra-Thin-Body SOI MOSFET

K. K. Young, T-ED (1989)

UTB (Fully-Depleted) SOI MOSFET





1. Solve 2-D Poisson's equation:

$$\frac{\partial^2\varphi}{\partial x^2}+\frac{\partial^2\varphi}{\partial y^2}=\frac{qN_A}{\varepsilon_{Si}}$$

with boundary conditions as:

$$\frac{\partial\varphi}{\partial x}=-\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{V_G-V_{FB}-\varphi}{t_{ox}}$$

$$\frac{\partial\varphi}{\partial x}=-\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{V_{Sub}-V_{FB}-\varphi}{t_{BOX}}$$

2... 3...

$$\frac{\partial^2\varphi}{\partial y^2}-\frac{\varphi}{\dfrac{t_{Si}{}^2\left(1+2\,{}^{C_{Si}}/_{C_{BOX}}\right)}{2\left(1+{}^{C_{ox}}/_{C_{Si}}+{}^{C_{ox}}/_{C_{BOX}}\right)}}=\frac{qN_A}{\varepsilon_{Si}}$$

where $C_{Si}={}^{\varepsilon_{Si}}/_{t_{Si}}$

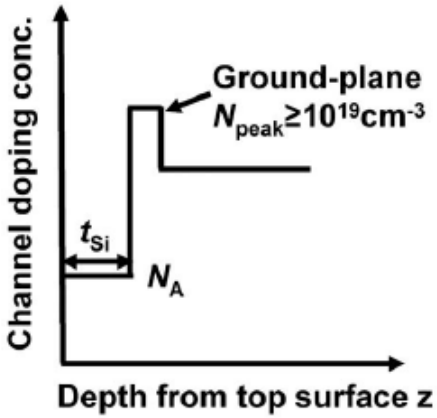
$C_{BOX}=\varepsilon_{ox}/t_{BOX}$

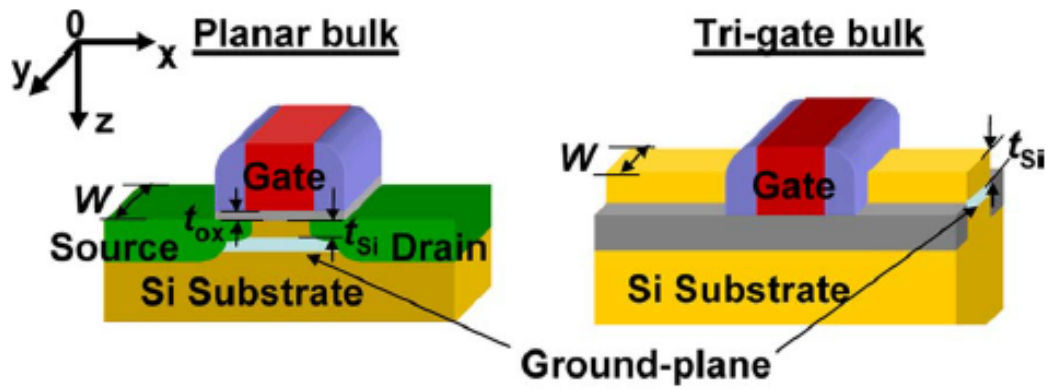
$C_{ox}=\varepsilon_{ox}/t_{ox}$

3-D Bulk Tri-Gate MOSFET

X. Sun, T-ED (2009)

Retrograde doping





Need to solve 3-D Poisson's equation:

$$\frac{d^2\Phi}{dx^2} + \frac{d^2\Phi}{dy^2} + \frac{d^2\Phi}{dz^2} = \frac{qN_A}{\varepsilon_{\mathrm{Si}}}$$

Scale length (*λ*) as a function of *z:*

$$\lambda = \sqrt{\frac{1 + \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}}\frac{z}{t_{\mathrm{ox}}} - \frac{z^2}{t_{\mathrm{Si}}^2} - \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}}\frac{z^2}{t_{\mathrm{ox}}t_{\mathrm{Si}}}}{\frac{8}{W^2}\left(\frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}}\frac{z}{t_{\mathrm{ox}}} - \frac{z^2}{t_{\mathrm{Si}}^2} - \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}}\frac{z^2}{t_{\mathrm{ox}}t_{\mathrm{Si}}}\right) + \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}}\frac{2}{t_{\mathrm{ox}}t_{\mathrm{Si}}} + \frac{2}{t_{\mathrm{Si}}^2}}}$$

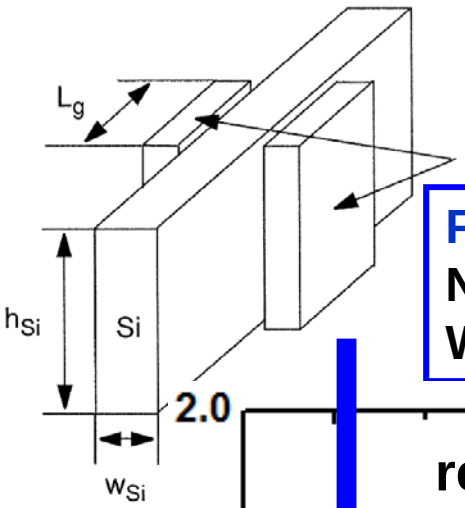
The "weak spot" locates at:

$$z_{\mathrm{peak}} = \frac{1}{\frac{2\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}}\frac{t_{\mathrm{ox}}}{t_{\mathrm{Si}}^2} + \frac{2}{t_{\mathrm{Si}}}}$$

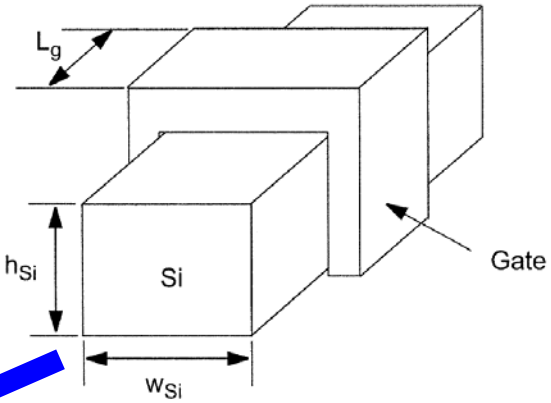
Tri-Gate MOSFET Aspect Ratio Design

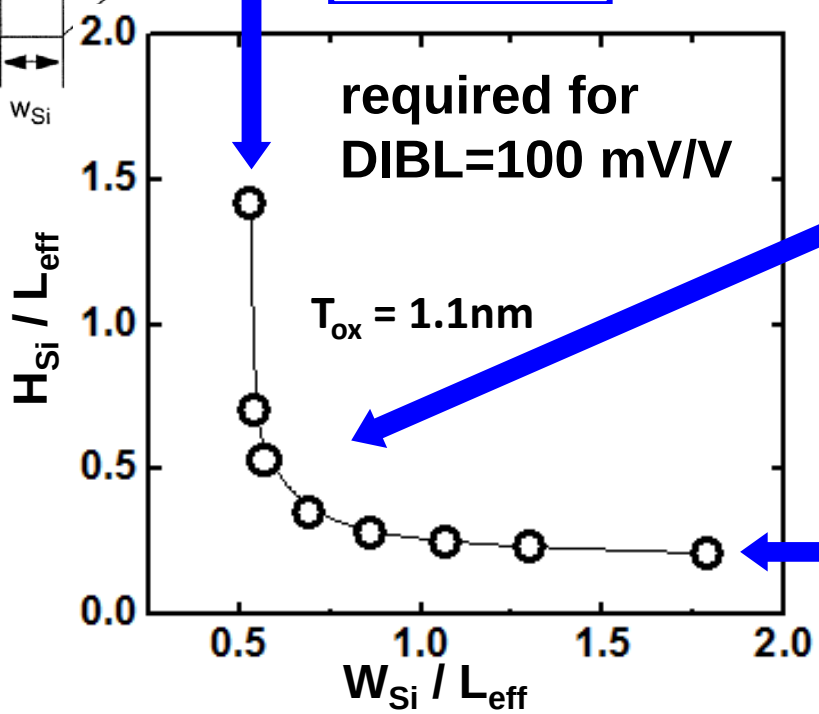
J.-W. Yang, T-ED (2005)

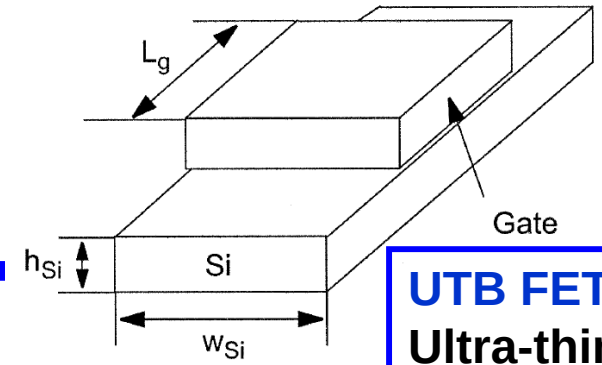
Tri-Gate FET
Relaxed fin dimensions
$W_{Si} > L_g/2$; $H_{Si} > L_g/5$



FinFET
Narrow fin
$W_{Si} \sim L_g/2$



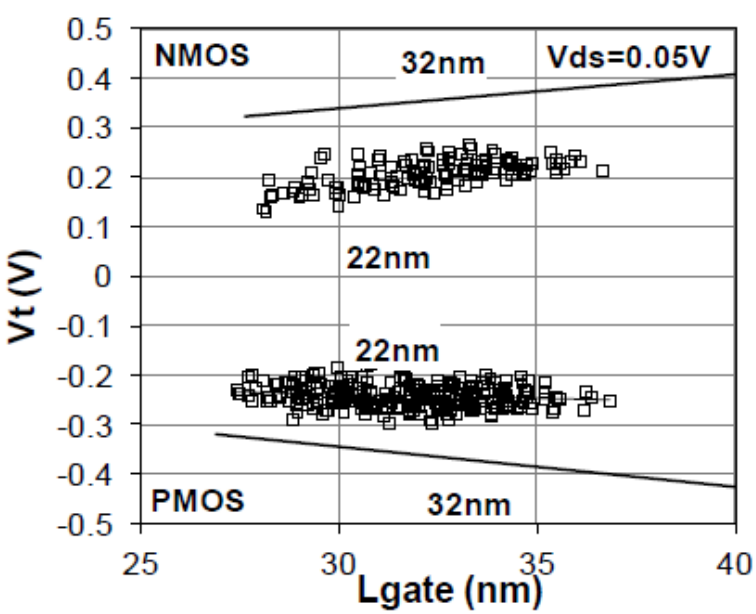


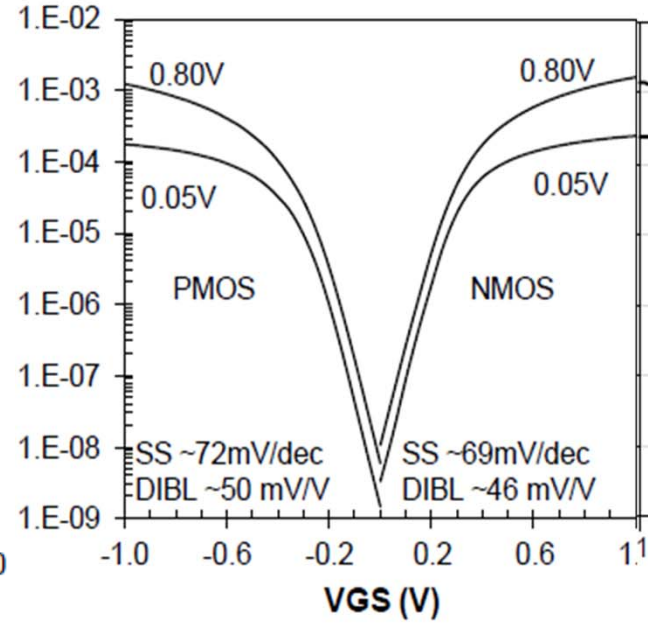


UTB FET
Ultra-thin SOI
$H_{Si} \sim L_g/5$

State-of-the-Art Thin-Body MOSFET's *DIBL and V_{TH} Roll-offs*

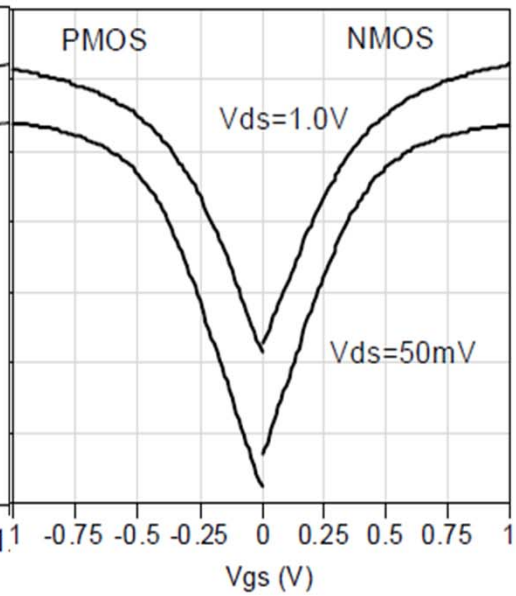
Intel's 22nm Tri-Gate FETs





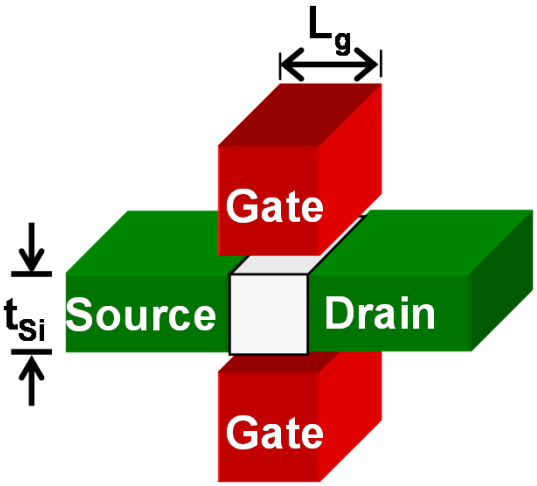
C. Auth, VLSI-T (2012)

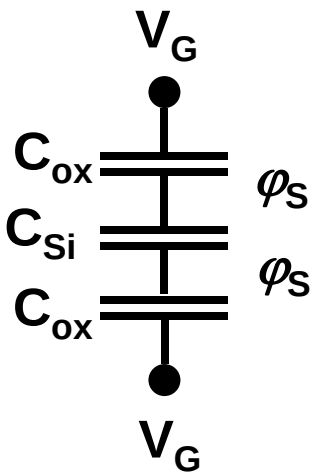
Intel's 32nm Planar FETs



P. Packan, IEDM (2009)

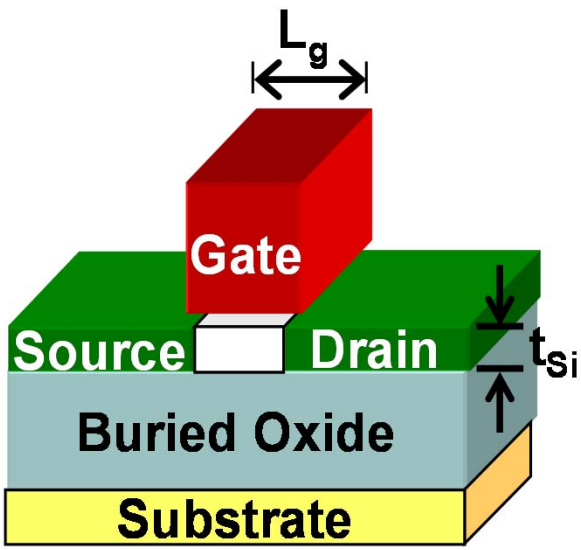
Long-L_g SS: FinFET

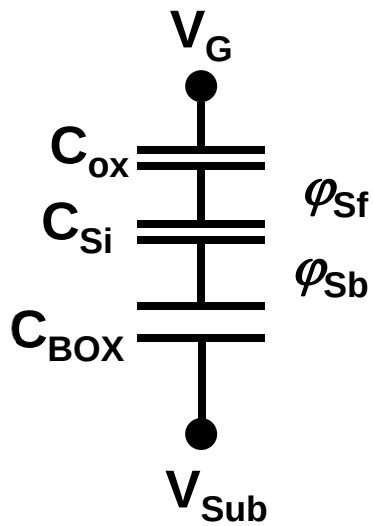




$$SS \equiv \frac{dV_G}{dlog_{10}I_D} = \frac{d\varphi_S}{dlog_{10}I_D} \cdot \frac{dV_G}{d\varphi_S}$$

Long-L_g SS: UTB SOI MOSFET

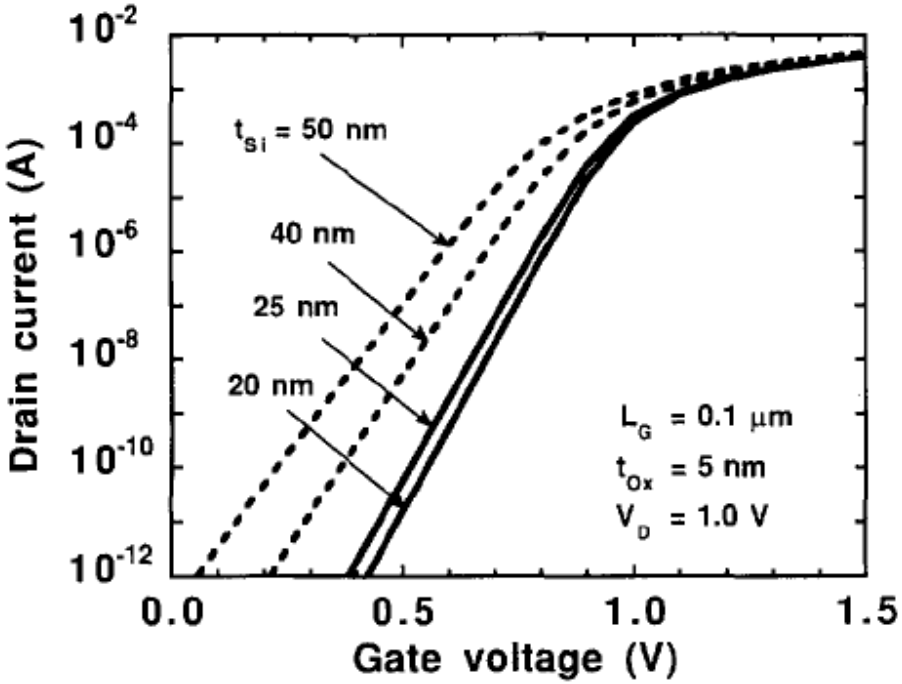




$$SS \equiv \frac{dV_G}{dlog_{10}I_D} = \frac{d\varphi_S}{dlog_{10}I_D} \cdot \frac{dV_G}{d\varphi_S}$$

Impact of t_{Si} on Short-L_g SS: FinFET

Simulation Results from DG FinFET

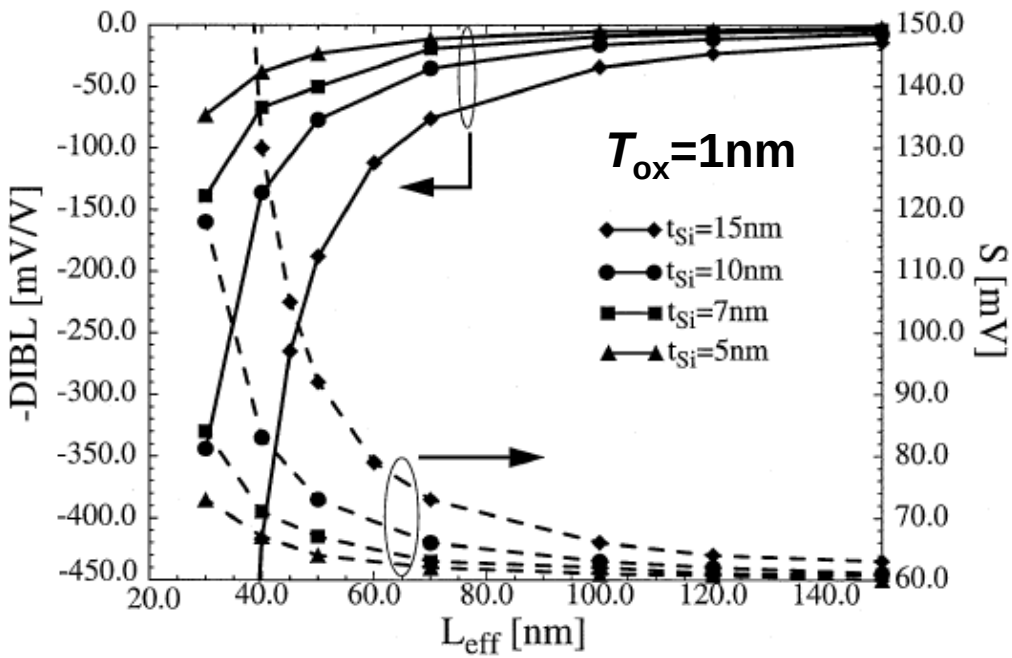


K. Suzuki, TED (1993)

- **SS degradation due to the increased junction capacitance as well as the reduced gate coupling as t_{Si} increases.**

Impact of t_{Si} on Short-L_g SS: UTB SOI MOSFET

Simulation Results from UTB SOI MOSFET



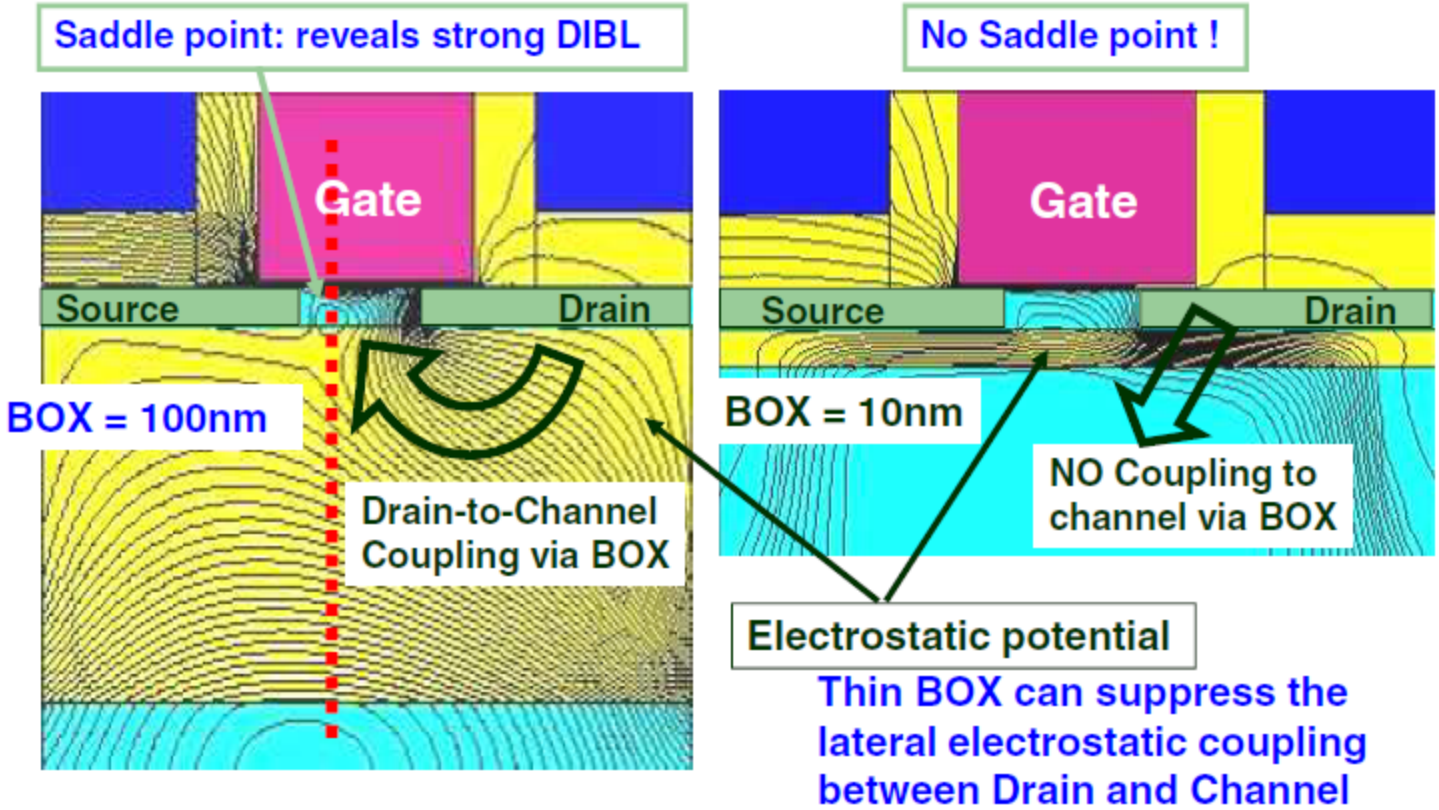
V. P. Trivedi, T-ED (2003)

- **SS degradation due to the increased junction capacitance as well as the DIBL-induced back channel conduction.**

- **Short-L_g SS for UTB SOI MOSFET (assumes top channel conduction):**

$$SS(Lg) = kT/q \cdot ln10/(1 - \frac{17 t_{Si} t_{ox}}{{L_g}^2})$$

Impact of t_{BOX} on Short-L_g UTB SOI MOSFET Electrostatics



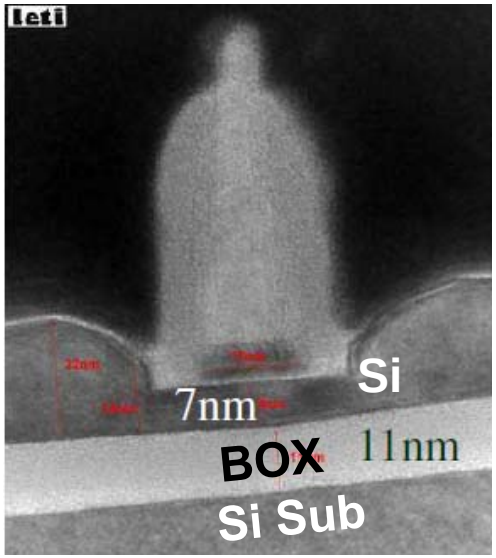
Modification to the existing SS and scale length model:

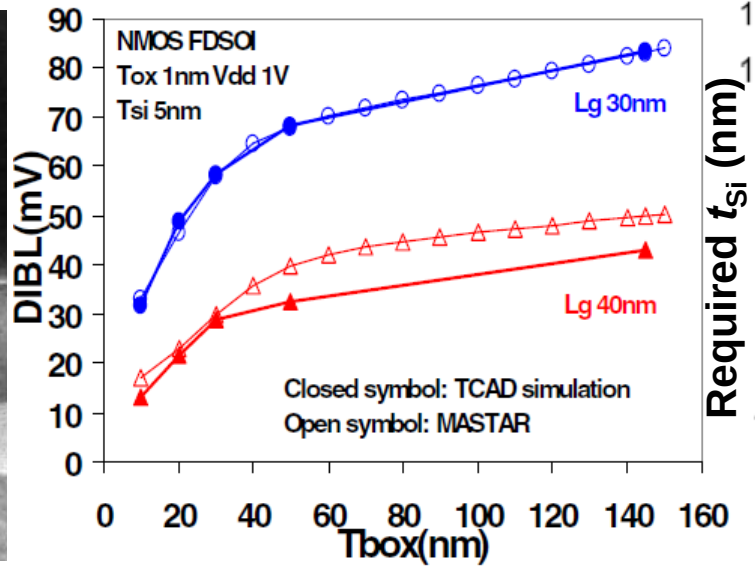
$$t_{Si,eff} = t_{Si} + \lambda t_{BOX} \quad \textbf{where} \quad \lambda = 0.2 \cdot [1 + \tan(1.5\frac{t_{BOX}}{L_g} - 1)] \cdot (\frac{L_g}{t_{BOX}} + 0.09)$$

T. Skotnicki, IEDM Short Course (2010)

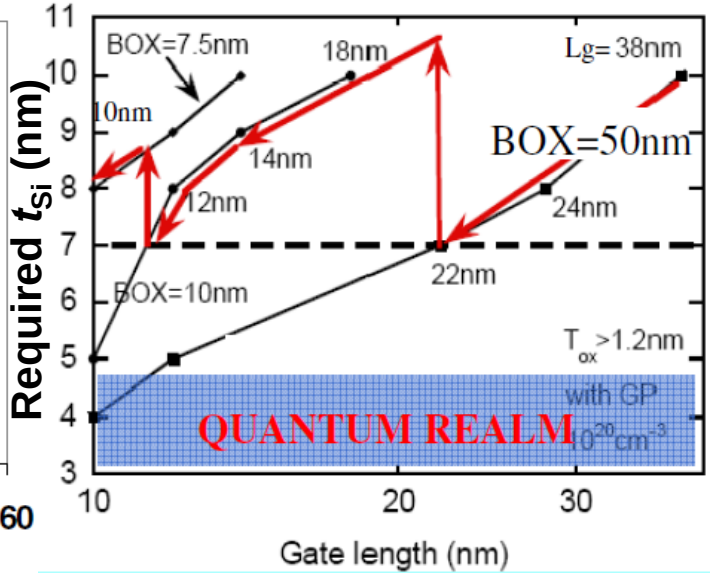
UTB"B": An Ultra Thin-Body & BOX SOI MOSFET

TEM Source: CEA-Leti





TCAD Results after O. Faynot (CEA-Leti)



- **Volume-production-ready** UTBB SOI MOSFETs have been successfully demonstrated, thanks to the advanced SOI substrate technology.
- **t_{BOX} serves as an extra knob** to further improve the electrostatics by reducing the scale length, alleviating BOX fringe field coupling and strong quantum confinement effect.

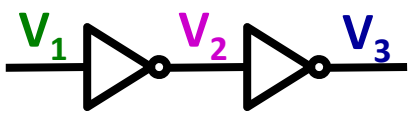
T. Skotnicki, IEDM Short Course (2010)

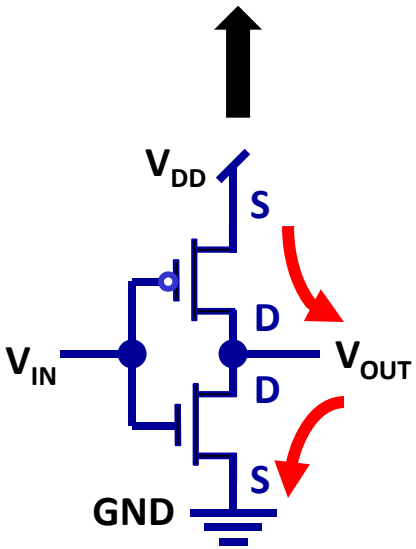
Effective Drive Current (I_{EFF})

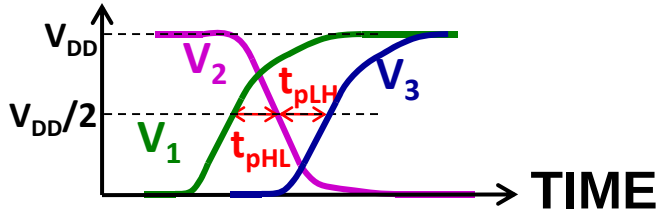
*Courtesy of T.-J. King Liu

M. H. Na, IEDM (2002)

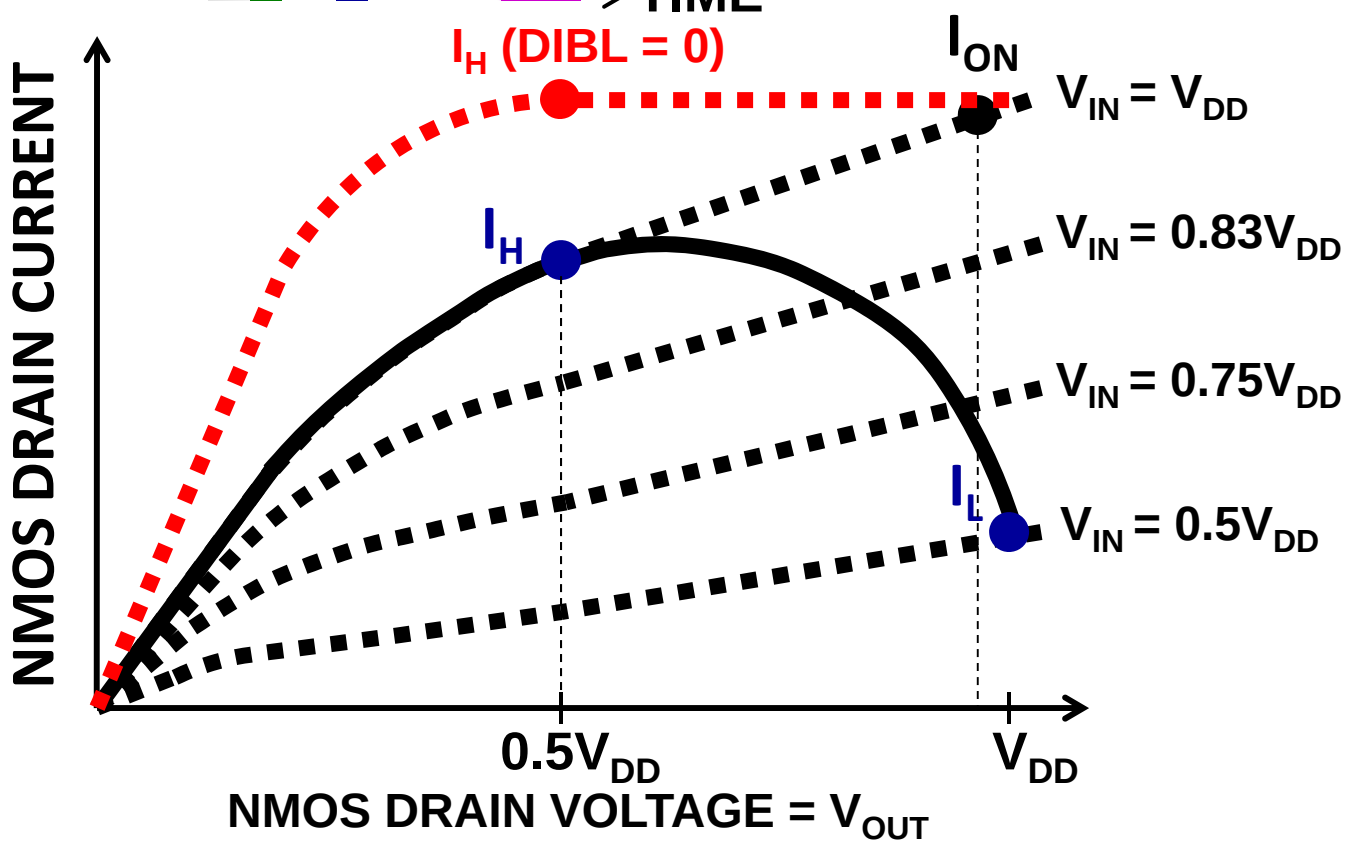
CMOS inverter chain:







$$I_{EFF} = \frac{I_H + I_L}{2}$$



I_{EFF} Dependence on DIBL

$$I_{EFF} = \frac{I_H + I_L}{2}$$

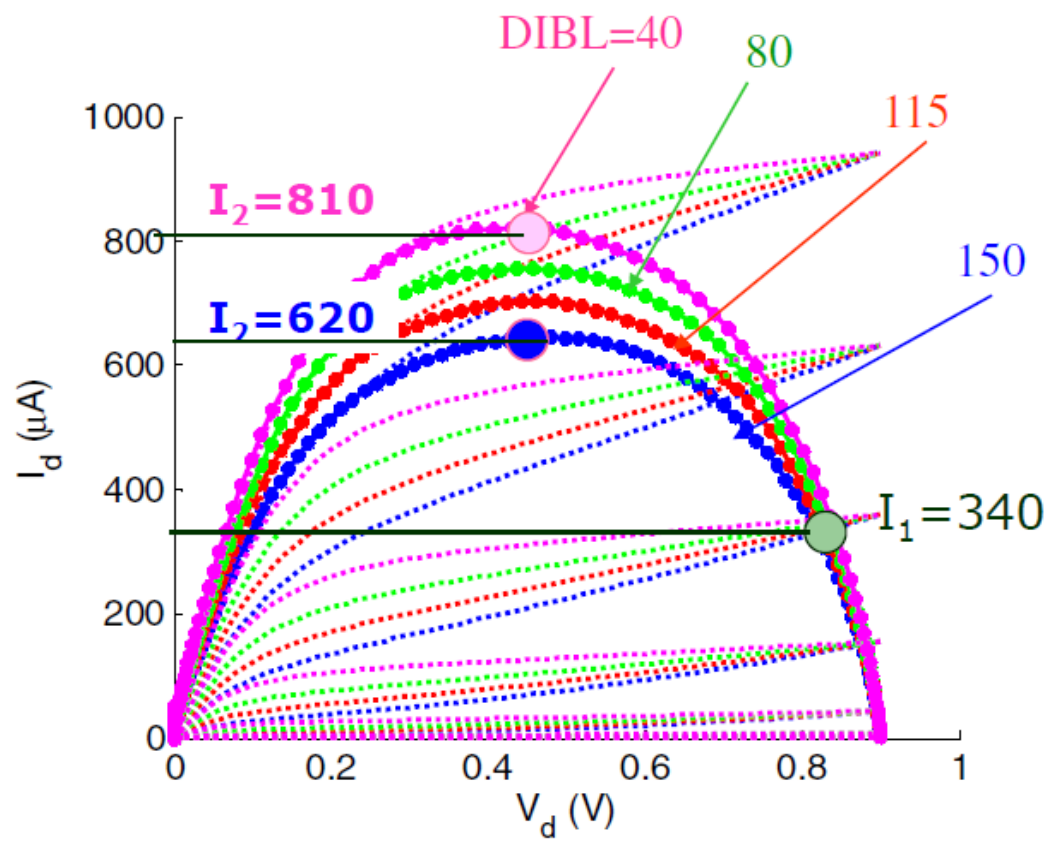
- It is necessary to include DIBL into I_{OFF} *vs.* I_{ON} plots, to better benchmark <u>digital</u> technologies → I_{OFF} *vs.* I_{EFF}

$I_{eff} \approx (340+810)/2=575$

$I_{eff} \approx (340+620)/2=480$

$\Delta f/f=\Delta Ieff/Ieff=95/480$
$=20\%$

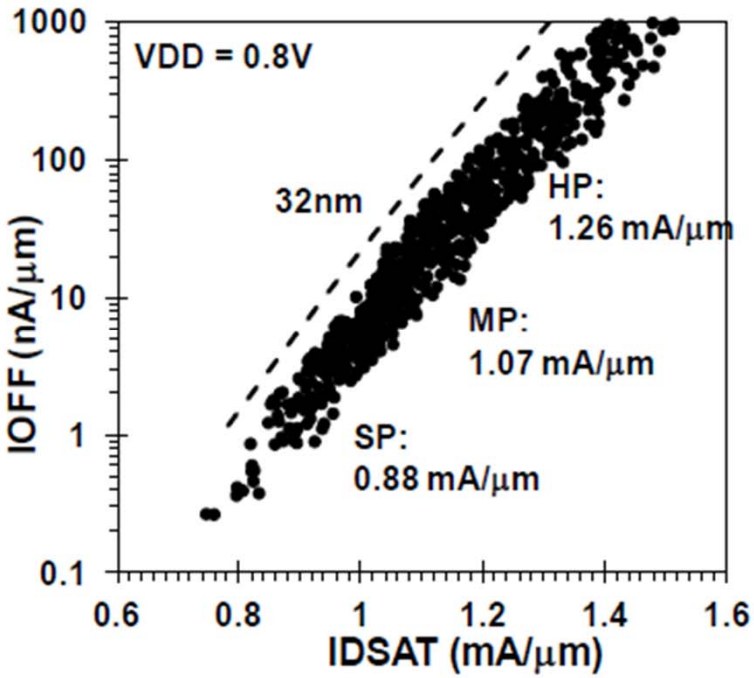
Lower DIBL
=
Higher Performance

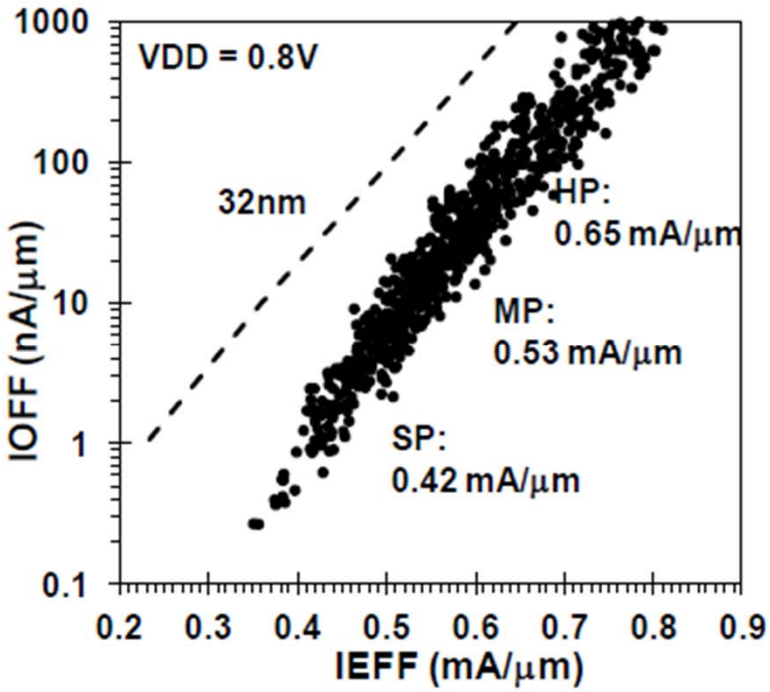


T. Skotnicki, IEDM Short Course (2010)

State-of-the-Art Thin-Body MOSFET's I_{OFF} *vs.* I_{ON} & I_{EFF} Plots

Intel's 22nm Tri-Gate N-FETs

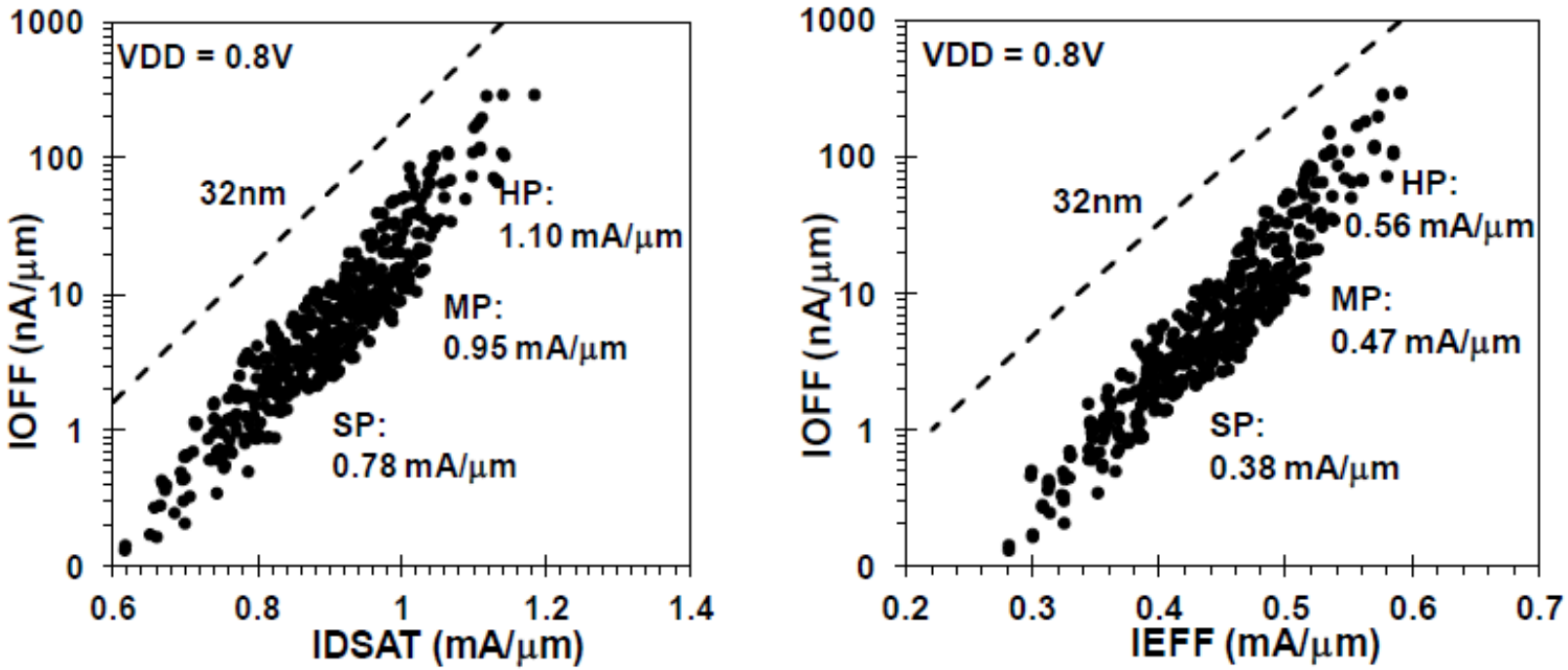




C. Auth, VLSI-T (2012)

State-of-the-Art Thin-Body MOSFET's I_{OFF} *vs.* I_{ON} & I_{EFF} Plots

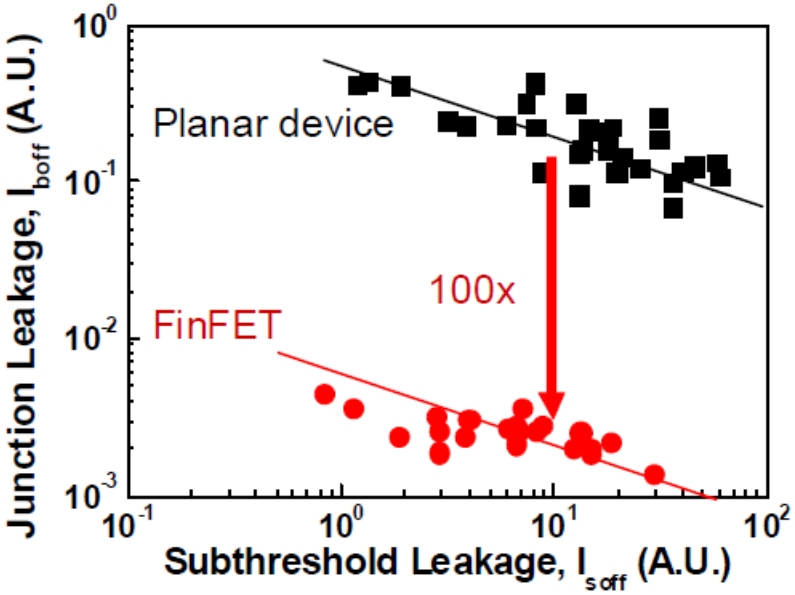
Intel's 22nm Tri-Gate P-FETs



C. Auth, VLSI-T (2012)

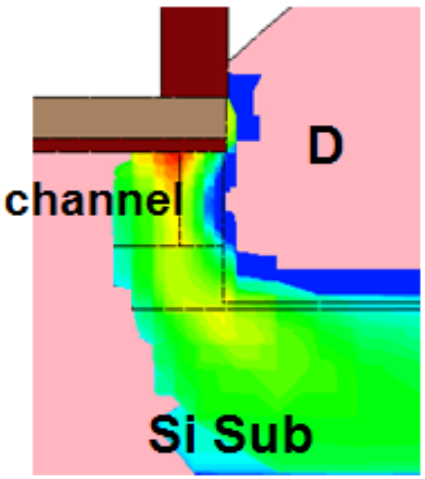
Reduced Band-to-Band-Tunneling (BTBT) in FinFET

TSMC's L_g=25nm MOSFETs



C. C. Wu, IEDM (2010)

BTBT Generation Rates



- **Due to reduced doping concentration in the fin (channel) region, BTBT-induced current (reverse PN leakage and GIDL) is suppressed.**

Summary

- **How good a thin-body MOSFET is, <u>regarding electrostatics</u>?**

Long Channel → ***Very Short Channel***

To Improve:	**DIBL**	**SS**		**DIBL**	**SS**
Planar SOI MOSFET: t_{Si}, t_{BOX}					
UTB					
UTBB					
FinFET: W_{Fin}, H_{Fin}					
Double Gate (Tall)					
Tri-Gate (Flat)					

References

Thin-Body MOSFET Electrostatics

1. K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, Y. Arimoto, "Scaling Theory for Double-Gate SOI MOSFET's," *IEEE Transactions on Electron Devices*, Vol.40, Issue 12, pp. 2326-2329, 1993.

2. R.-H. Yan, A. Ourmazd, K.F. Lee, "Scaling the Si MOSFET: from Bulk to SOI to Bulk," *IEEE Transactions on Electron Devices,* Vol. 39, Issue 7, pp. 1704-1710, 1992.

3. K. K. Young, "Short-Channel Effect in Fully Depleted SOI MOSFET's," *IEEE Transactions on Electron Devices*, Vol.36, Issue 2, pp. 399-402, 1989.

4. X. Sun, T.-J. King Liu, "Scale-Length Assessment of the Bulk Trigate MOSFET Design," *IEEE Transactions on Electron Devices*, Vol.56, Issue 11, pp. 2840-2842, 2009.

5. J.-W. Yang, J. G. Fossum, "On the Feasiability of Nano-scale Triple Gate CMOS Transistors," *IEEE Transactions on Electron Devices*, Vol.52, Issue 6, pp. 1159-1164, 2005.

6. V. P. Trivedi, J. G. Fossum, "Scaling Fully Depleted SOI CMOS," *IEEE Transactions on Electron Devices*, Vol.50, Issue 10, pp.2095-2103, 2003.

7. T. Skotnicki, "CMOS Technology Scaling: Trends, Scaling and Issues," *IEEE International Electron Device Meeting*, Short Course, 2010.

Effective Drive Current

8. M. H. Na, E. J. Nowak, W. Haensch, J. Cai, "The Effective Drive Current in CMOS Inverters," *IEEE International Electron Devices Meeting Technical Digest*, pp. 121-124, 2002.

References

Industry CMOS Platforms

9. (Intel 32nm HP) P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier *et al*., "High Performance 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors," *IEEE International Electron Devices Meeting Technical Digest*, pp. 659-662, 2009.

10. (Intel 22nm TriGate) C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier *et al*., "A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors," *Symposium on VLSI Technology* Digest, pp. 131-132, 2012.

11. (TSMC FinFET) C. C. Wu, D. W. Lin, A. Keshavarzi, C. H. Huang, C. T. Chan *et al*., "High Performance 22/20nm FinFET CMOS Devices with Advanced High-k/Metal Gate Scheme," *IEEE International Electron Devices Meeting Technical Digest*, pp. 600-603, 2010.