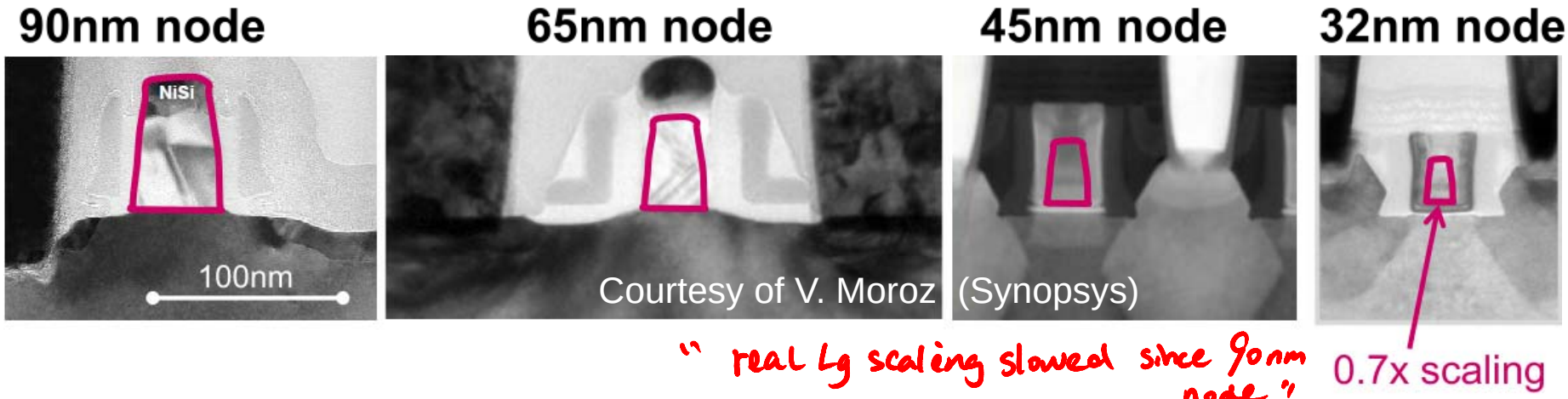


Lecture 2

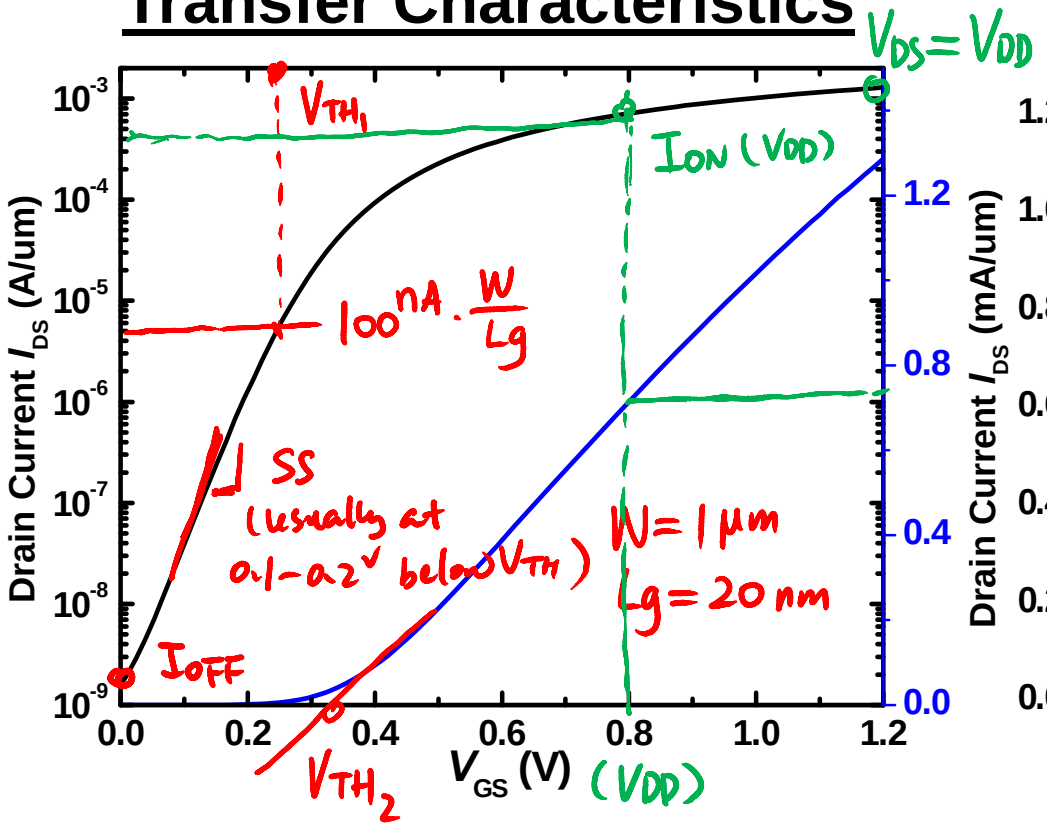
- Short-Channel MOSFET Electrostatics
  - MOSFET Performance Metrics
  - Short-Channel Effects

Reading:

- Taur & Ning, "Fundamentals of Modern VLSI Devices," Cambridge Univ. Press, 1998.
- multiple research articles (reference list at the end of this lecture)

Simple MOSFET Performance Metrics

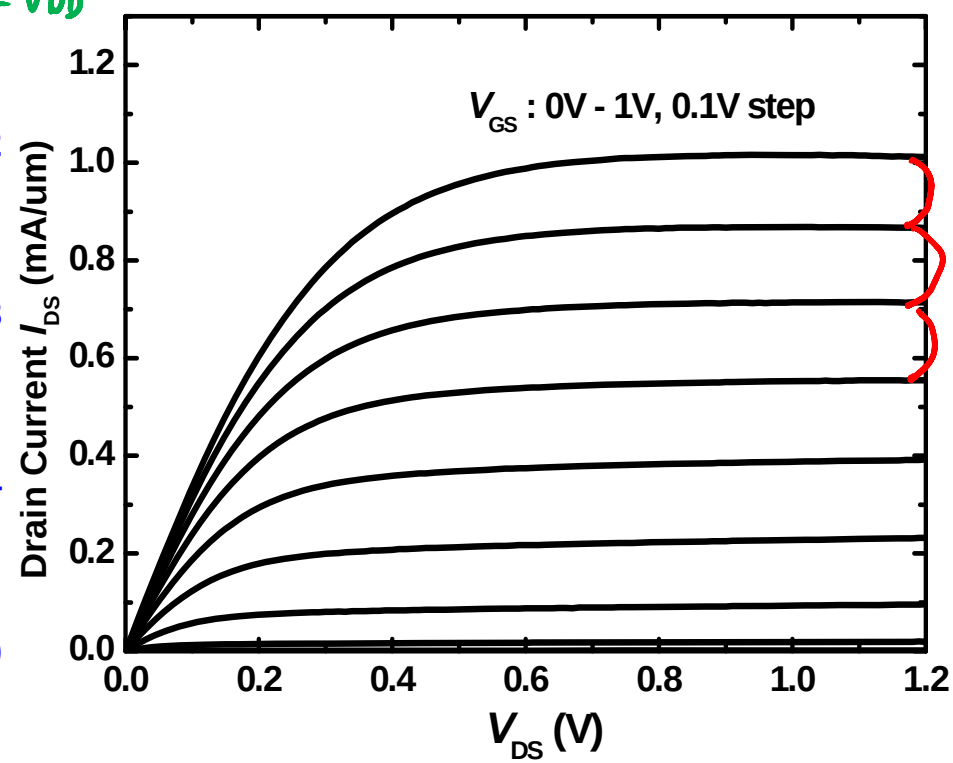
Transfer Characteristics



: I_{OFF}, I_{ON}, V_{TH}, SS

(1. const. current definition
2. Extrapolation

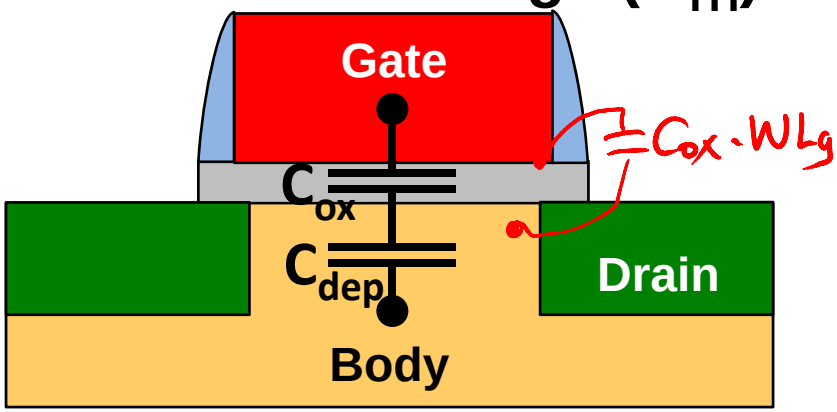
Output Characteristics



: V_{EA}, G_{ds} ($\frac{1}{R_{out}}$), $I_{ds} \propto (V_{GS} - V_{TH})^{\alpha}$

Review of Long Channel MOSFET

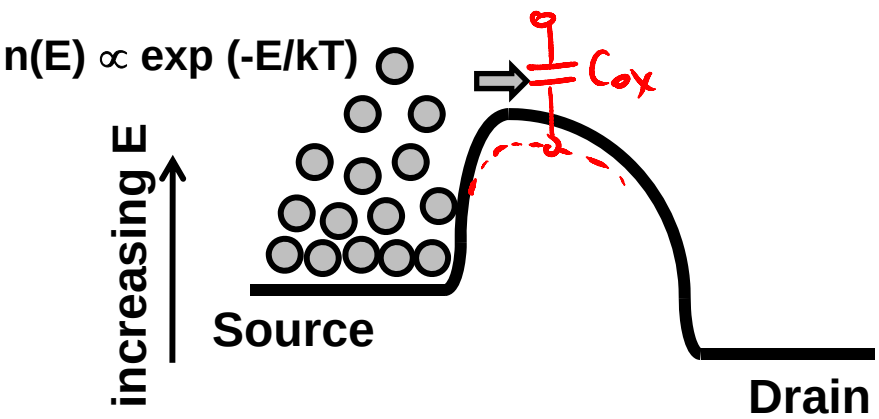
- **Threshold Voltage (V_{TH})**

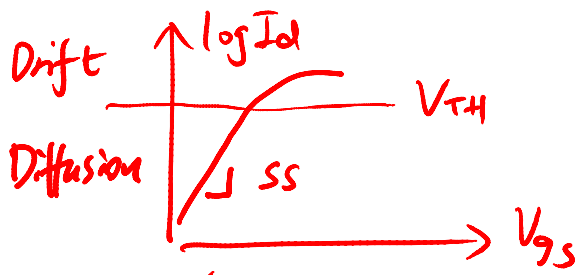


Work Func. difference between Metal & Si (Gate)

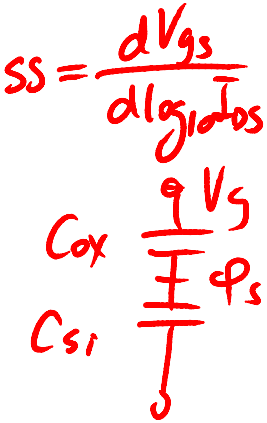
$$V_{TH} = V_{FB} + \underbrace{2\phi_F}_{\text{voltage drop on Si}} + \underbrace{\frac{Q_{dep}}{C_{ox}}}_{V_{ox}:\ \text{voltage drop at } C_{ox}}$$

- **Sub-threshold Swing (SS)**





$$SS = \frac{dV_{gs}}{d\log_{10} I_{ds}} = \frac{dV_{gs}}{d\phi_s} \cdot \frac{d\phi_s}{d\log_{10} I_{ds}}$$

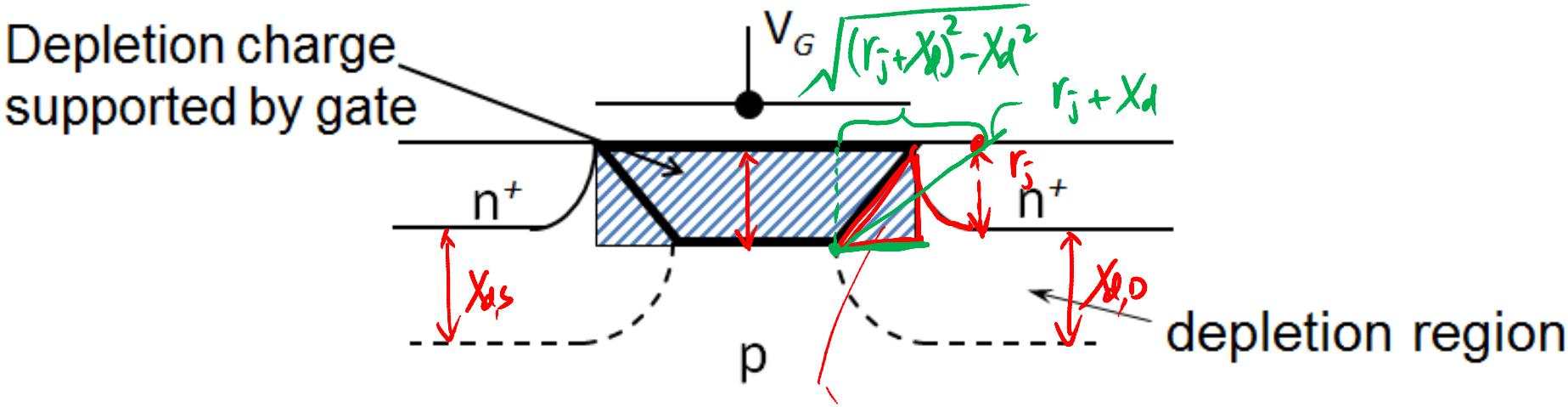


$$\Downarrow \quad \frac{C_{si} + C_{ox}}{C_{ox}} \cdot \frac{k_B T}{q} \ln 10$$

$$\Downarrow \quad I \propto \exp\left(\frac{q\phi_s}{kT}\right)$$

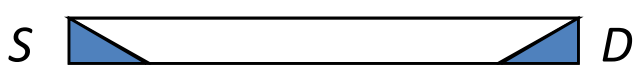
$$\Rightarrow \frac{k_B T}{q} \ln 10 \cdot \left(1 + \frac{C_{dep}}{C_{ox}}\right)$$

Short Channel Effect (SCE)



- **The smaller L_g is, the greater percentage of depletion charge balanced by the S/D PN junctions**

<u>Long Channel</u>:



<u>Short Channel</u>:

- **1st Order Analysis**

$$S_\Delta = \left[\sqrt{(r_j+X_d)^2-X_d^2}-r_j\right]\cdot X_d/2$$

$$\frac{\Delta Q_{dep}}{Q_{dep}} = \frac{S_{\Delta,S}+S_{\Delta,D}}{\left(\frac{X_D+X_S}{2}\right)\cdot L_g} = \frac{\left(\sqrt{1+\frac{X_d}{r_j}}-1\right)\cdot r_j}{L_g}$$

Quantitative Derivation of SCE: Yau's Model

L.-D. Yau, SSE (1974)

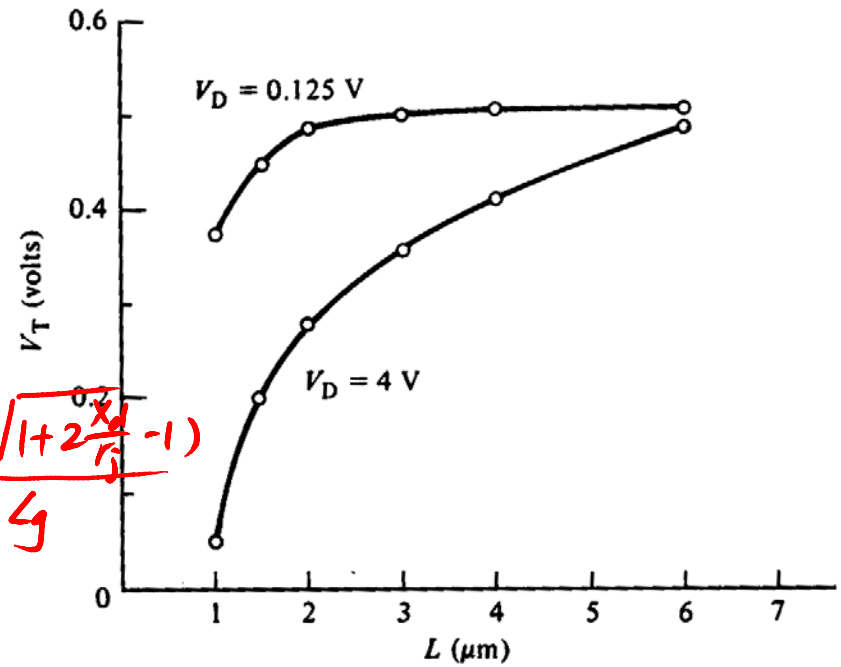
- **Depletion charge (Q_{dep}) reduction:**

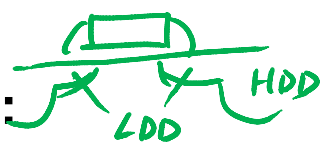
$$\Delta Q_{dep} = r_j\left(\sqrt{1+2\frac{X_d}{r_j}}-1\right)\cdot X_d \cdot W \cdot qN_{sub}$$

- **Threshold Voltage Lowering:**

$$\Delta V_{TH} = -\frac{\Delta Q_{dep}}{C_{ox}\cdot(W\cdot L_g)} = -\frac{qN_{sub}X_d r_j\left(\sqrt{1+2\frac{X_d}{r_j}}-1\right)}{C_{ox}\cdot L_g}$$

$\sim L_g^{-1}, X_d, r_j$





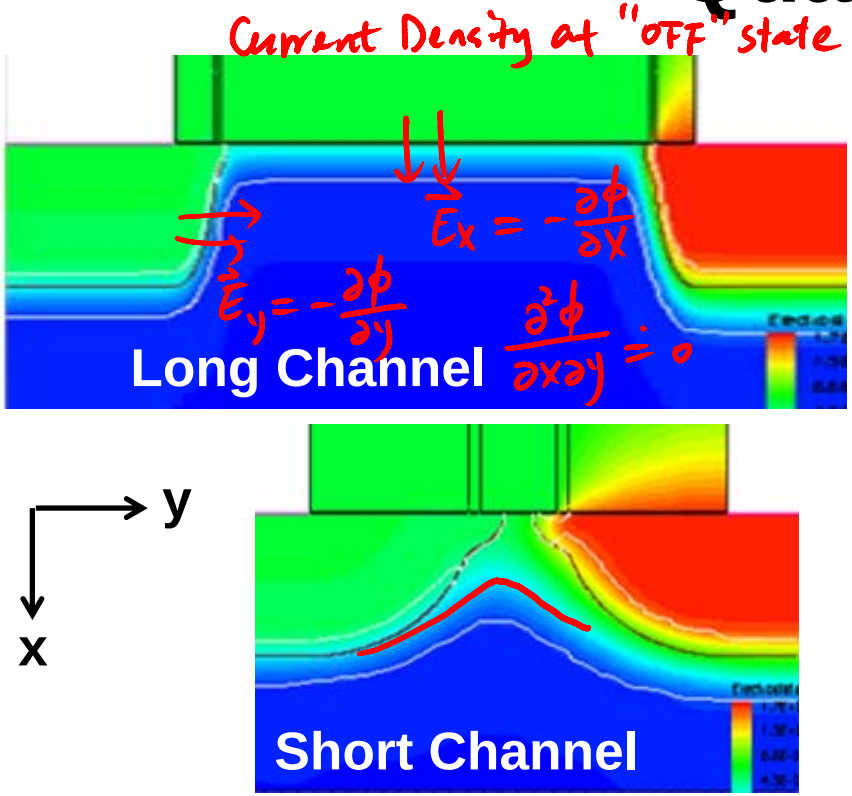
"lightly-doped source/drain"

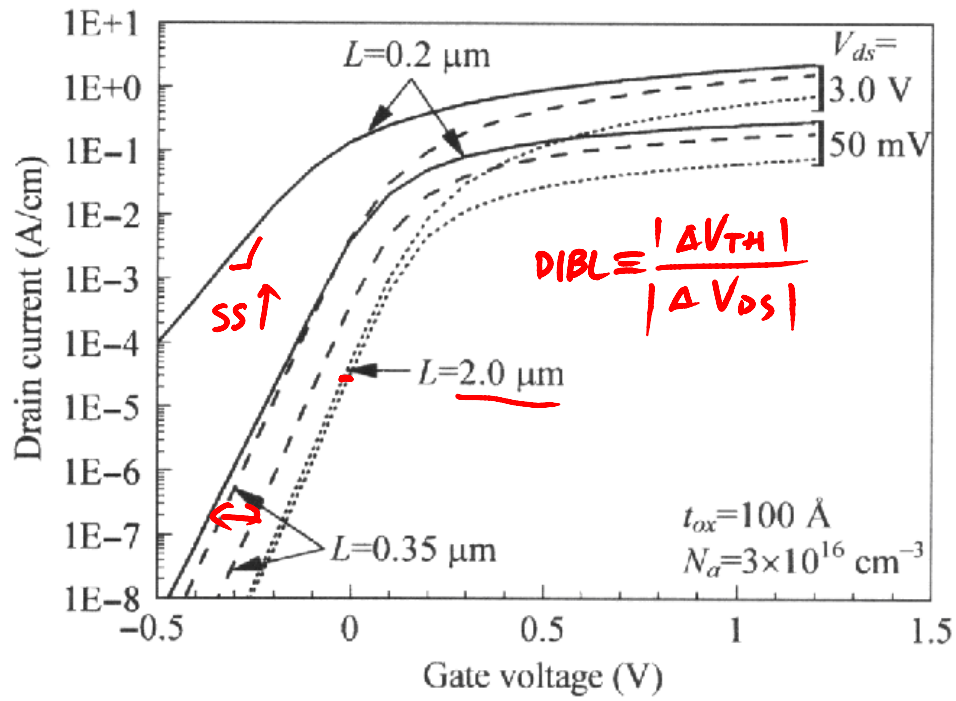
- **Yau's model's assumptions:**
  - **Uses geometry relations instead of solving Poisson's equation**
  - **Assumes channel potential is linear along lateral (*i.e.* channel) direction**

→ USJ : Ultra-shallow junction

$r_j \sim 4nm$ for planar bulk

Drain Induced Barrier Lowering (DIBL) - Qualitative





C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Figure 7-5

In short-L_g MOSFET:

- **x- and y- components of the electric field are coupled**
  → Drain bias will affect the barrier at source/channel
  → More band bending at given gate bias → V_T decreases

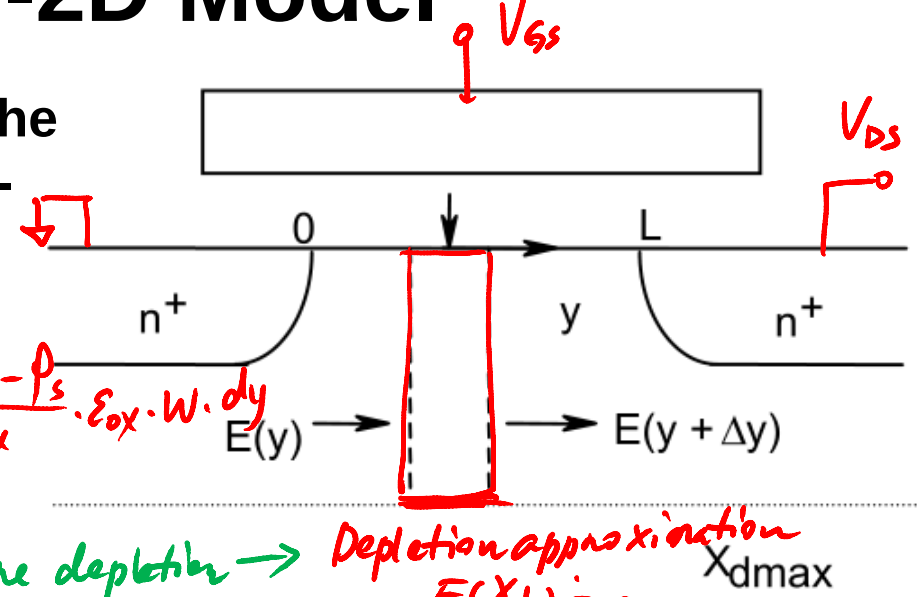
want to get $\phi_s(y)$ vs. V_{DS}, L_g...

$E_c = -\frac{\partial \phi_s}{\partial x(y)}$

Derivation for DIBL - A Quasi-2D Model

Steps:

1. Develop Poisson's equation in the channel region, including x- and y-components.



Gauss' law:

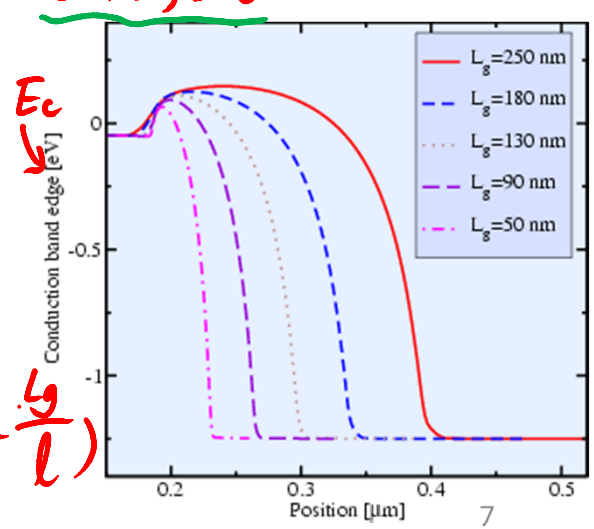
$$-E(y)\cdot X_d\cdot \varepsilon_s\cdot W + E(y+dy)\, X_d\, \varepsilon_s\, W - \frac{V_g - V_{FB} - \phi_s}{T_{ox}}\cdot \varepsilon_{ox}\cdot W\cdot dy = dy\cdot W\cdot X_d\cdot qN_{sub}$$

No mobile charge inside the depletion region → Depletion approximation $E(X_d) \doteq 0$

Boundary Conditions: 1. $\phi_s(0) = V_{bi}$ 2. $\phi_s(L_g) = V_{bi} + V_{DS}$

2. Solve φ_S as a function of position (y)

$$\varphi_s(y) = V_{sL} + (V_{bi} + V_{DS} - V_{sL})\frac{\sinh(y/l)}{\sinh(L/l)} + (V_{bi} - V_{sL})\frac{\sinh((L-y)/l)}{\sinh(L/l)}$$



3. Calculate the peak of φ_S, which corresponds to V_{TH}. $\equiv V_g \Big|_{\frac{\partial \phi_s}{\partial y} = 0}$

$$V_{sL} = V_{GS} - V_T$$

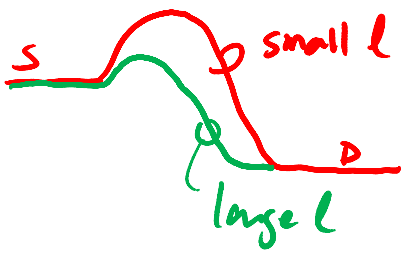
$$\Delta V_{TH} \doteq V_{DS}\cdot \exp\left(-\frac{L_g}{l}\right)$$

→ "screening" length

Scale Length – A Simplified Knob

1. **Tells how closely a MOSFET approaches a "short-channel" device.**

$$l \equiv \sqrt{\frac{\varepsilon_S T_{Ox} X_{d\max}}{\varepsilon_{Ox}}} = \sqrt{3 T_{Ox} X_{d\max}}$$



→ how a MOSFET is capable to "screen" E-field at its OFF state.

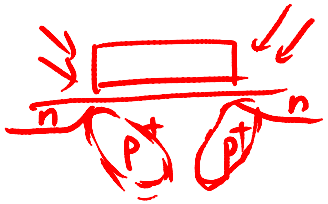
2. **Provides the guideline to scale a MOSFET while maintaining its electrostatic integrity.**

e.g. **for Planar Technology:**

Bulk

1. high-k
2. N_{sub} ↑ ⇒ HALO (problematic)

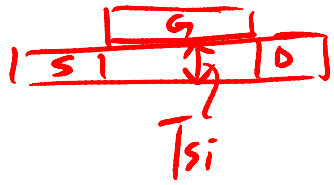
⇓ Retro-grade well



X_d ↓ P-sub

Ultra-Thin-Body

$l = \sqrt{3 T_{ox} \cdot T_{si}}$



Double-Gated FinFET

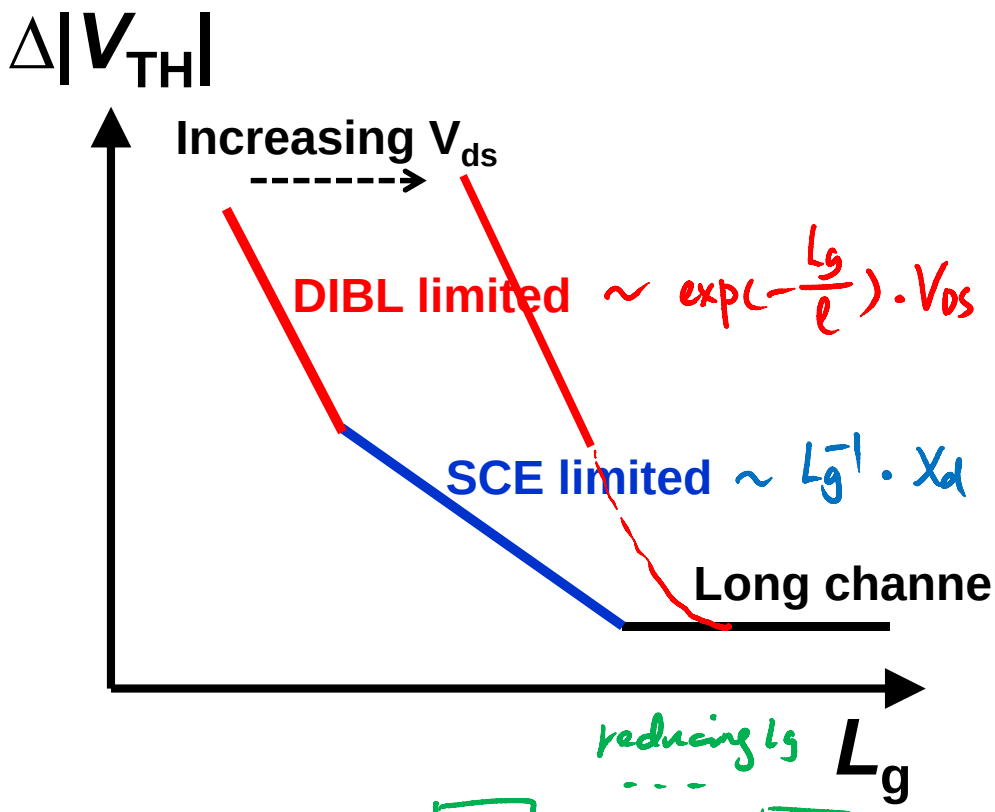
"symmetric"

$T_{ox} \rightarrow \frac{T_{ox}}{2}$

due to $C_{ox} \rightarrow 2 \cdot C_{ox}$

$l = \sqrt{\frac{3}{2} T_{ox} \cdot T_{si}}$

V_{TH} *vs.* L_g Plots: SCE + DIBL



→ 2 regions: caused by SCE
DIBL

→ different trends vs. L_g, V_{DS}

at high V_{DS} or small L_g:

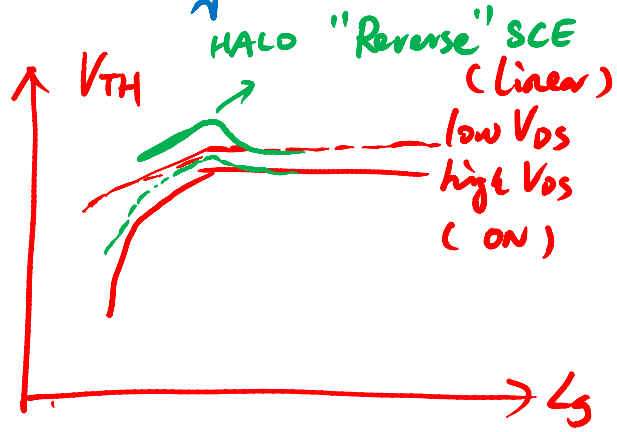
$\Delta V_T(\text{DIBL}) \gg \Delta V_T(\text{SCE})$

DIBL limited $\sim \exp(-\frac{L_g}{\ell}) \cdot V_{DS}$

SCE limited $\sim L_g^{-1} \cdot X_d$, where $X_d \sim \sqrt{\phi_{bi} + V_{DS}}$

reducing L_g

"self-adaptive"



State-of-the-Art MOSFET's V_{TH} *vs.* L_g Plots

Estimation: good DIBL requires $\leq 100 \frac{mV}{V}$.

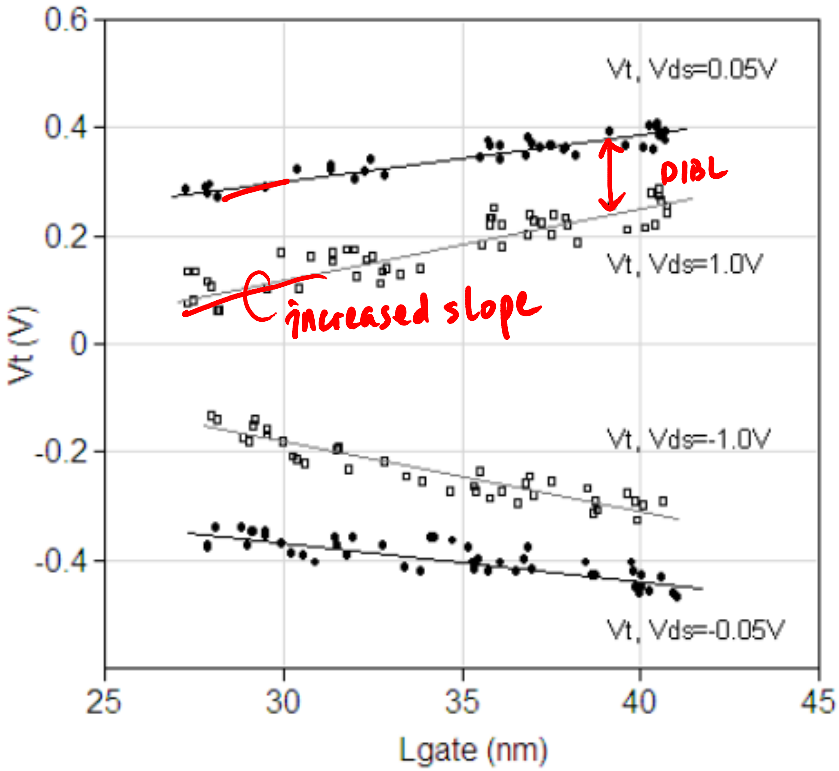
$\Delta V_{TH} = V_{DS} \cdot \exp(-\frac{L_g}{\ell})$

$\therefore \frac{-L_g}{\ell} = \ln(\frac{\Delta V_{TH}}{V_{DS}}) \leq \ln(0.1)$

$L_g \geq \ln 10 \cdot \ell$

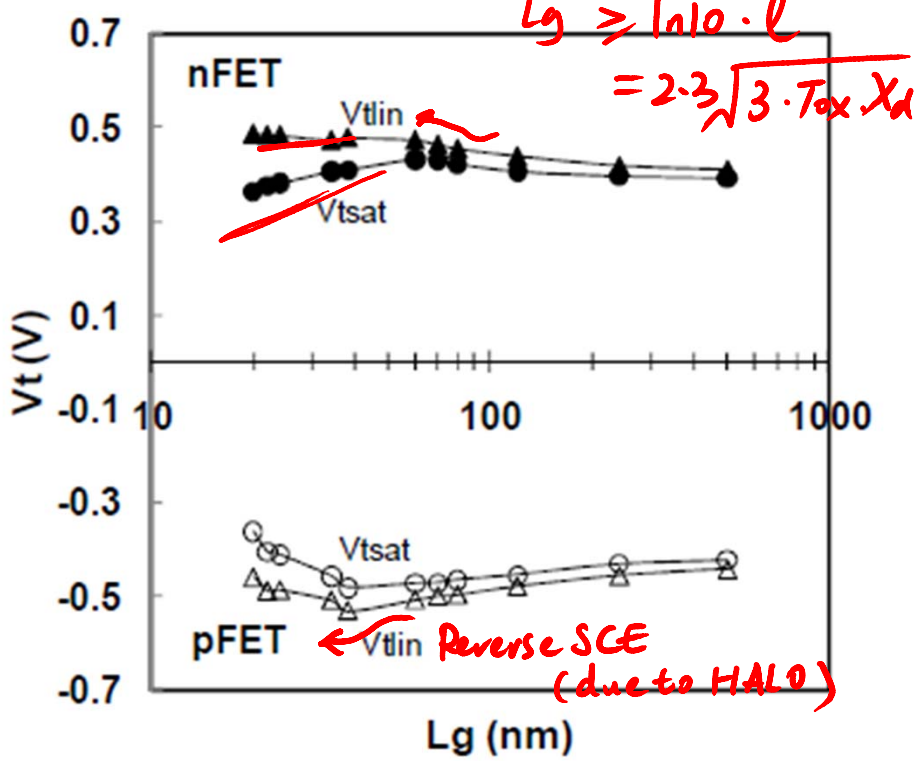
$= 2.3\sqrt{3 \cdot T_{ox} X_d}$

Intel's 32nm Bulk



P. Packan, IEDM (2009)

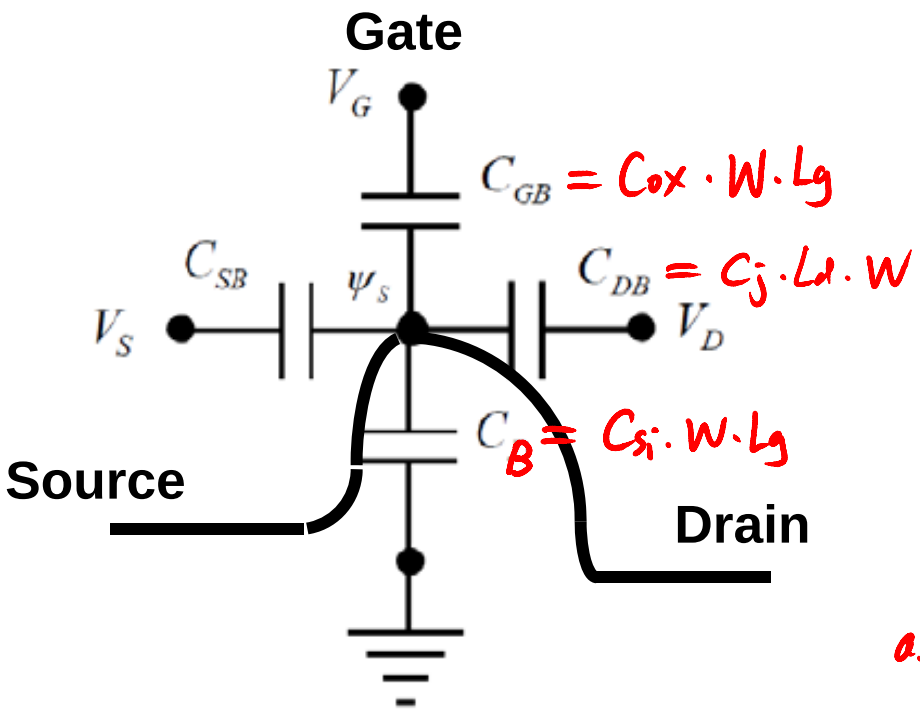
Samsung's 20nm Bulk



H.-J. Cho, IEDM (2011)

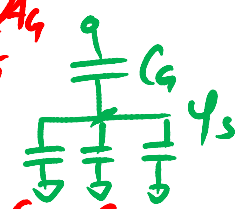
Sub-threshold Swing Degradation

- **A 2-D Capacitor Network Model** **(after Prof. M. Lundstrom)**



long-channel swing

$$SS = 2.3 \frac{kT}{q} \cdot \frac{(C_{dep} + C_{ox}) \cdot \cancel{A_G}}{C_{ox} \cdot \cancel{A_G}}$$



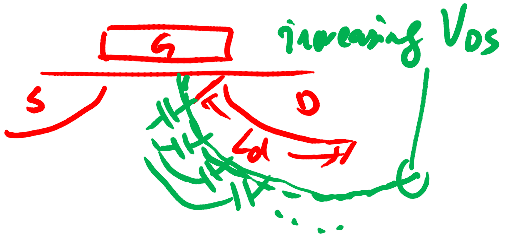
short-channel:

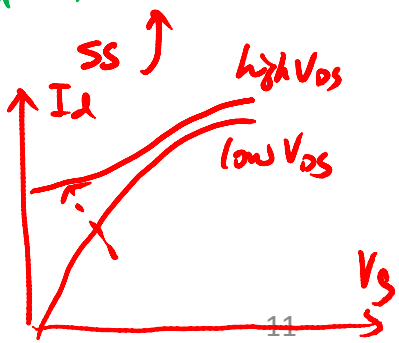
$$SS' = 2.3 \frac{kT}{q} \cdot \frac{C_S + C_D + C_G + C_B}{C_G}$$

$$= 60\ mV/dec \cdot \left(1 + \frac{C_{dep}}{C_{ox}} + \frac{2C_j \cdot L_d}{C_{ox} \cdot L_g}\right)$$

- **Impact of L_g Scaling on SS**

as $L_g \downarrow$ or $V_{DS} \uparrow$ ($\Rightarrow L_d \uparrow$)

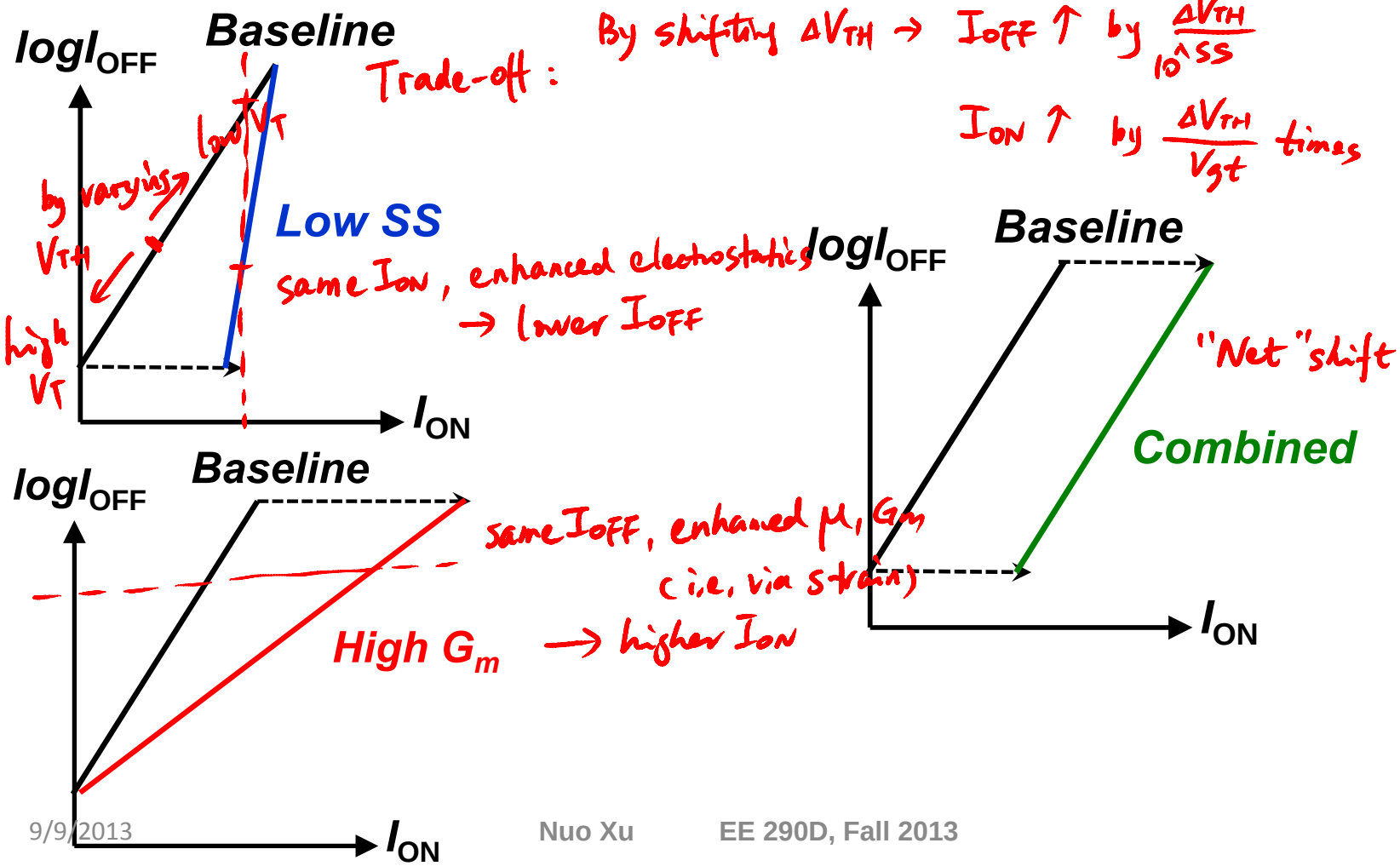




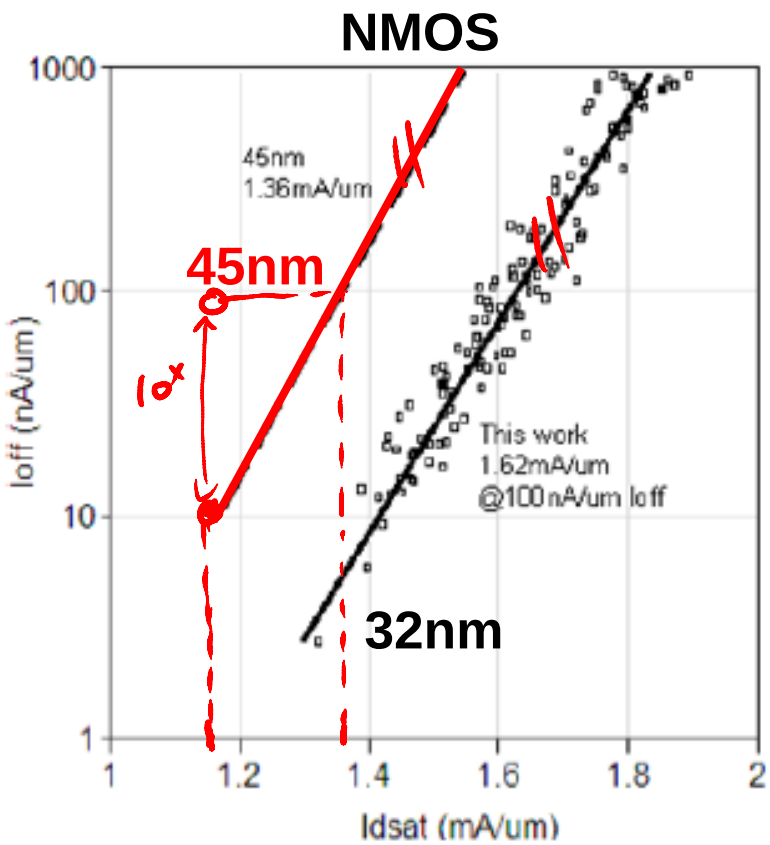
SCE → DIBL → SS ↑ → punch-through

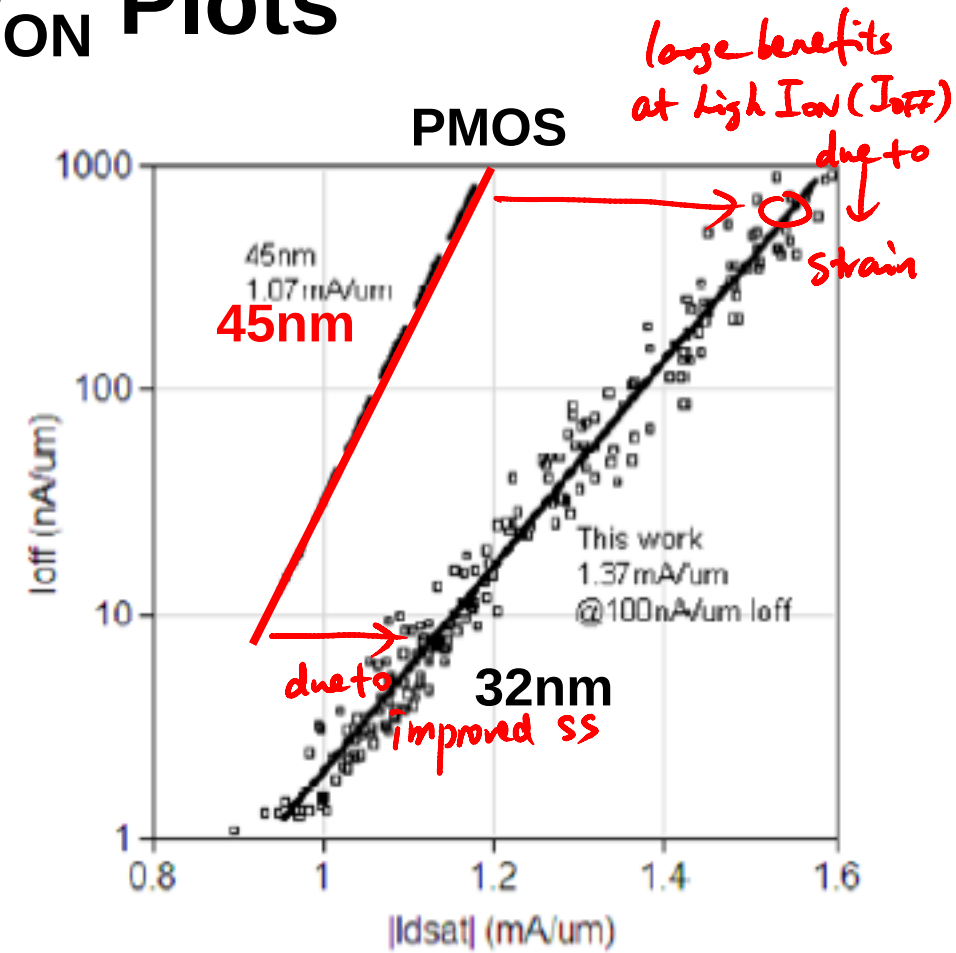
I_{OFF} vs. I_{ON} Plots

- Generated by "shifting" a device's V_{TH} under a fixed V_{DD}
- To benchmark the effectiveness of technology advancement.



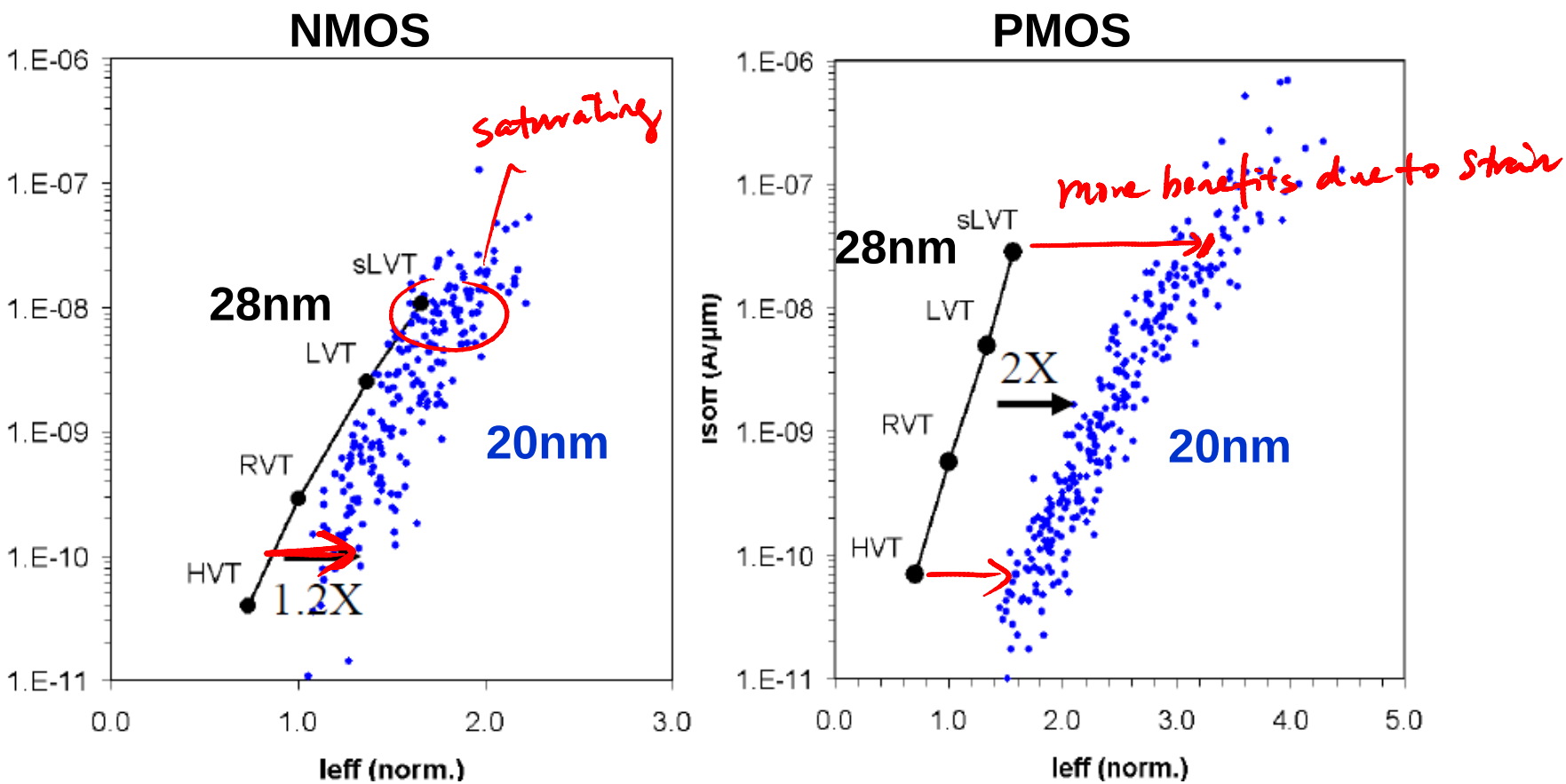
Intel's 32nm Bulk CMOS I_{OFF} *vs.* I_{ON} Plots





P. Packan, IEDM (2009)

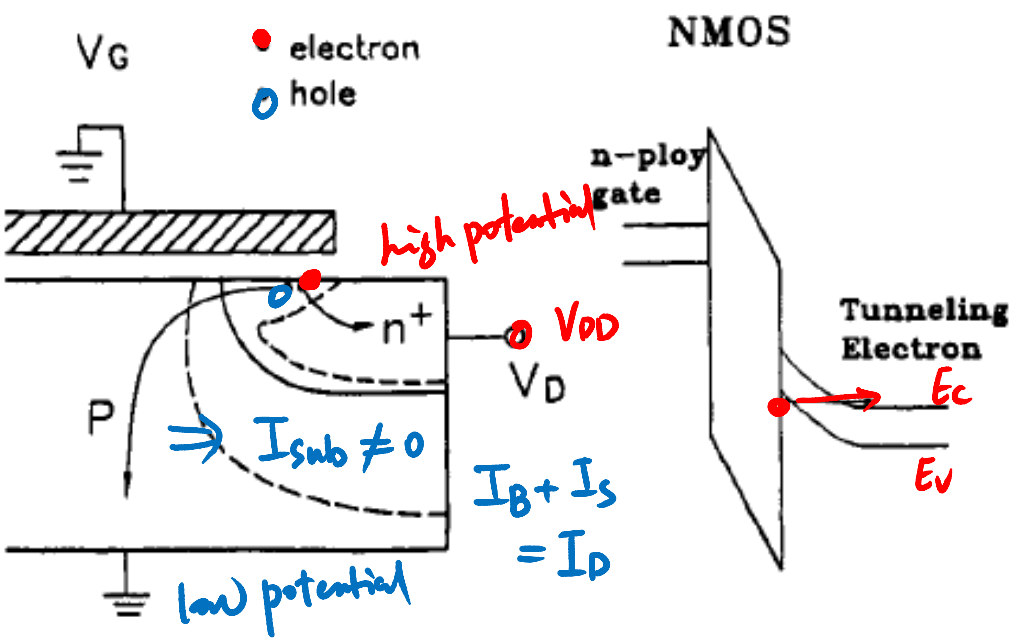
IBM's 20nm Bulk CMOS I_{OFF} *vs.* I_{ON} Plots



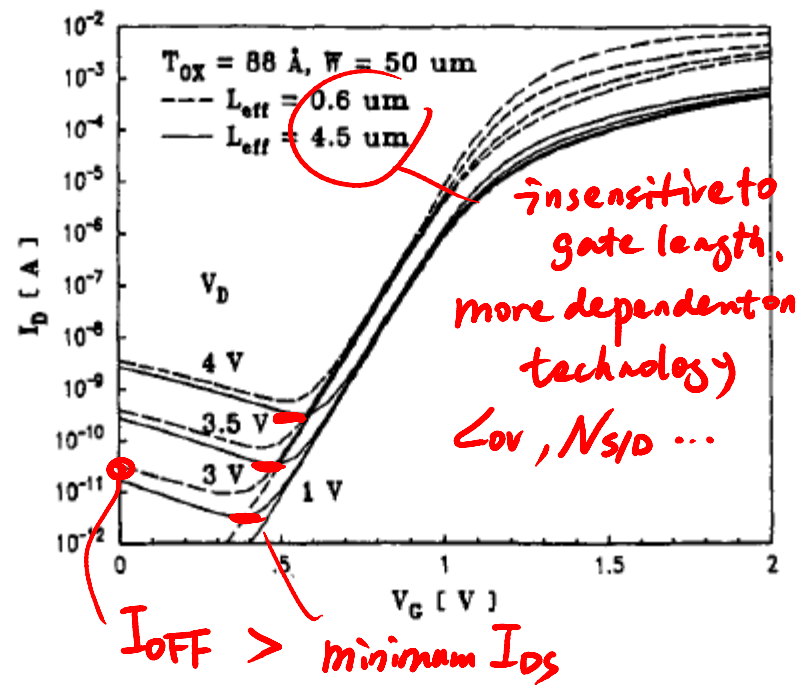
H. Shang, VLSI-T (2012)

Gate Induced Drain Leakage (GIDL)

Illustration and Band Profiles



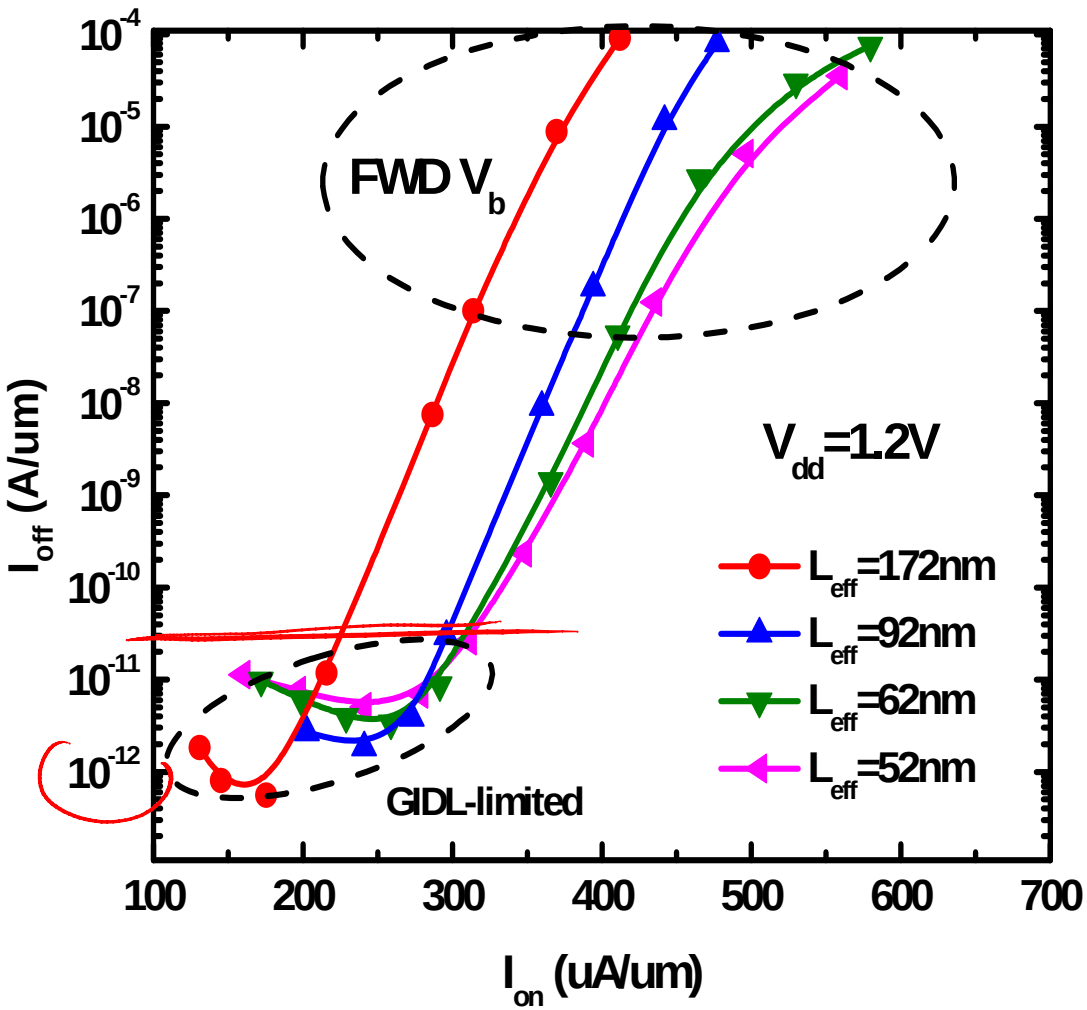
I_d vs. V_{gs} Characteristics

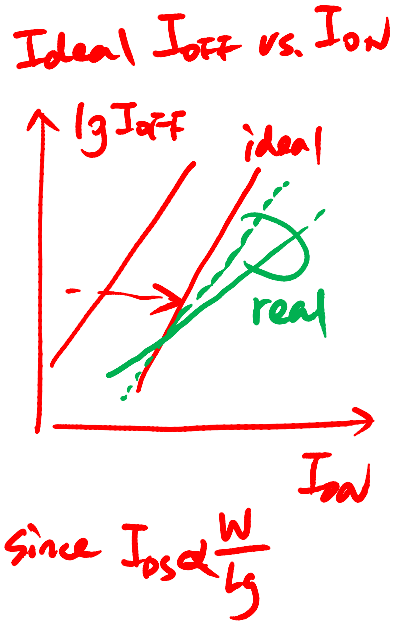


1. Overlapped (Gate w/ S/D) region
2. High V_{DS} (large band bending)

T.-Y. Chan, IEDM (1987)

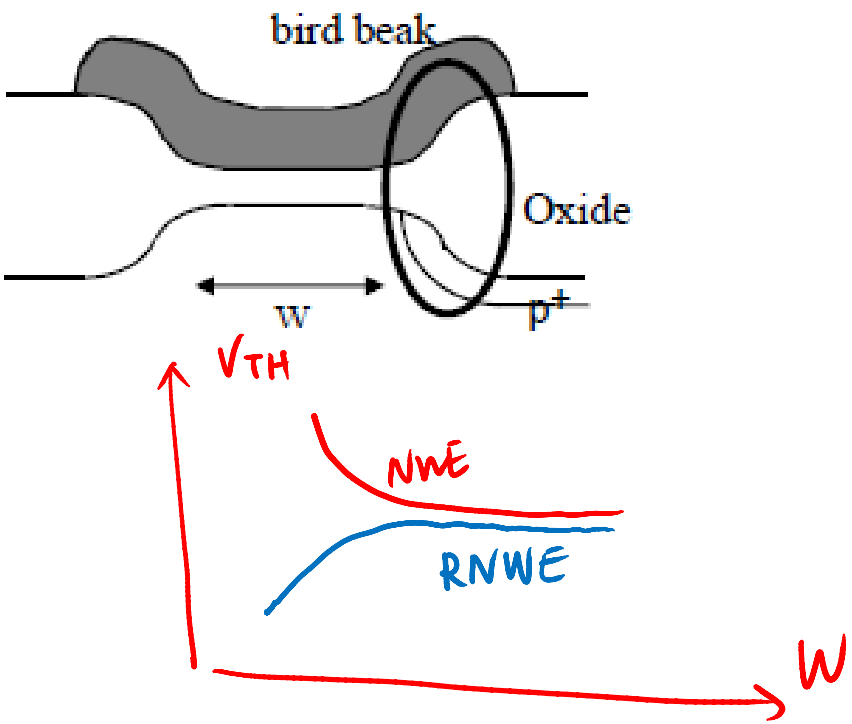
GIDL-Limited I_{OFF} *vs.* I_{ON} Plots





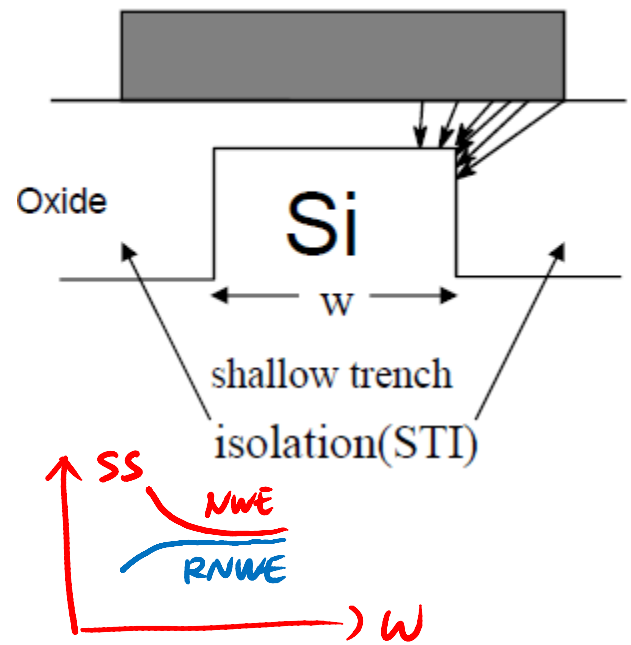
Narrow Width Effects

Narrow Width Effect



Reverse Narrow Width Effect

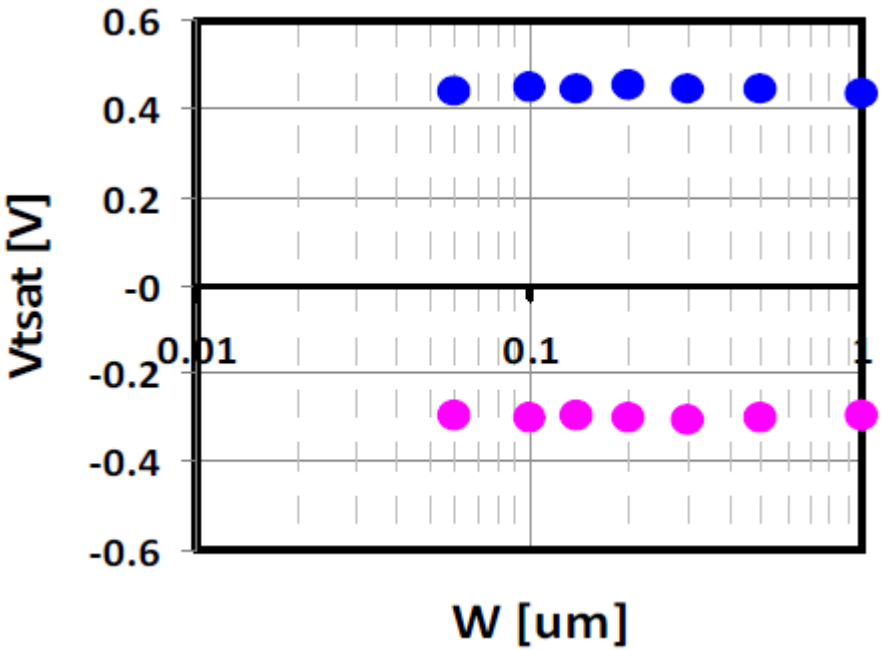
- A "Quasi-planar" MOSFET !



- **Narrow Width Effect is caused by LOCOS process.**
- **Reverse Narrow Width Effect is caused by STI process.**
- **Introduce problems as transistor *systematic variations*.**

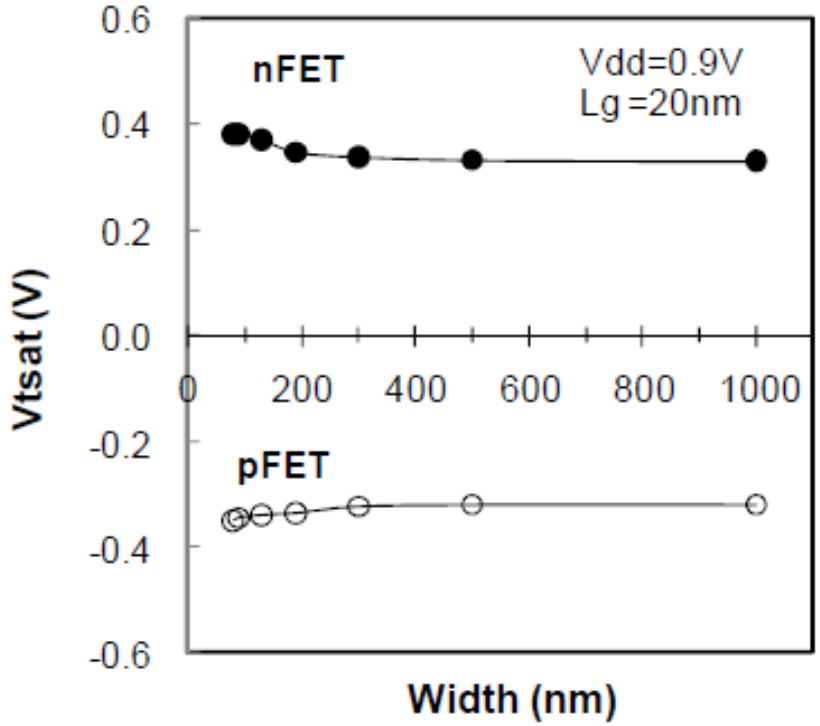
State-of-the-Art MOSFET's Narrow Width Effects

IBM's 20nm CMOS



H. Shang, VLSI-T (2012)

Samsung's 20nm CMOS

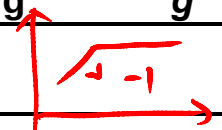
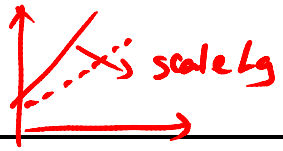
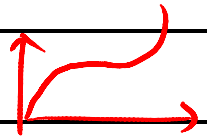
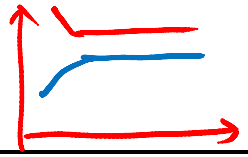
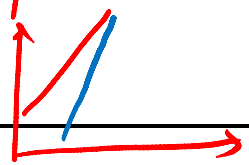


H.-J. Cho, IEDM (2011)

- **Thanks to advanced isolation techniques, narrow width effects are no longer problematic.**

Summary

- **How bad a planar bulk MOSFET is, <u>regarding electrostatics</u>?**

	I_d *vs.* V_g	I_d *vs.* V_d	V_g *vs.* L_g	I_{OFF} *vs.* I_{ON}
SCE				
DIBL				
SS Degradation				
Punchthrough				
GIDL				
Narrow Width Effects				

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