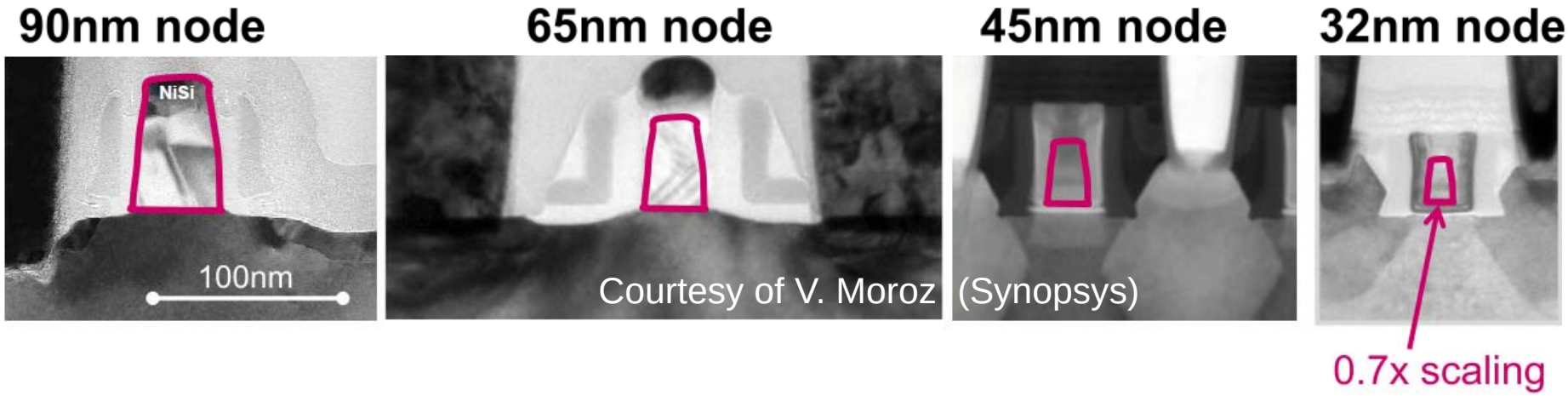


Lecture 2

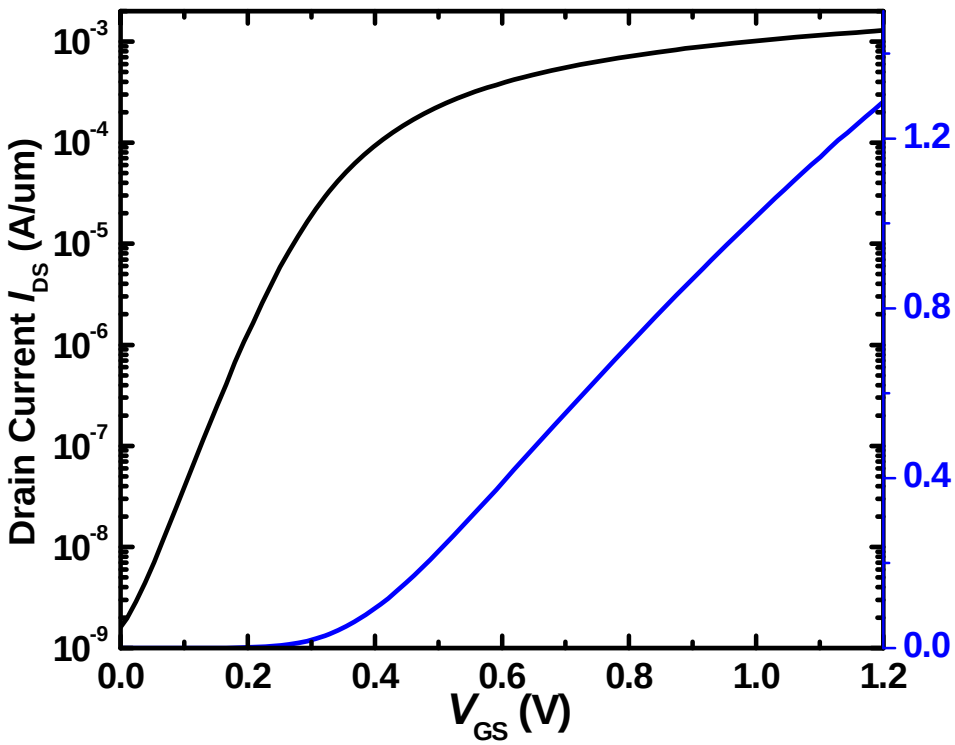
- Short-Channel MOSFET Electrostatics
  - MOSFET Performance Metrics
  - Short-Channel Effects

Reading:

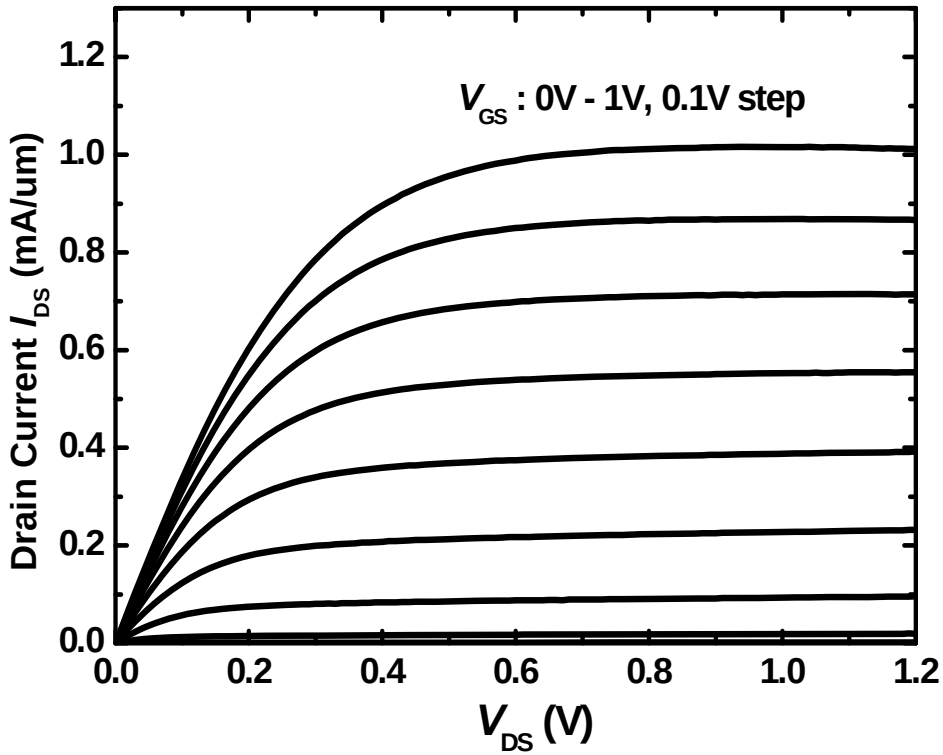
- Taur & Ning, "Fundamentals of Modern VLSI Devices," Cambridge Univ. Press, 1998.
- multiple research articles (reference list at the end of this lecture)

Simple MOSFET Performance Metrics

Transfer Characteristics

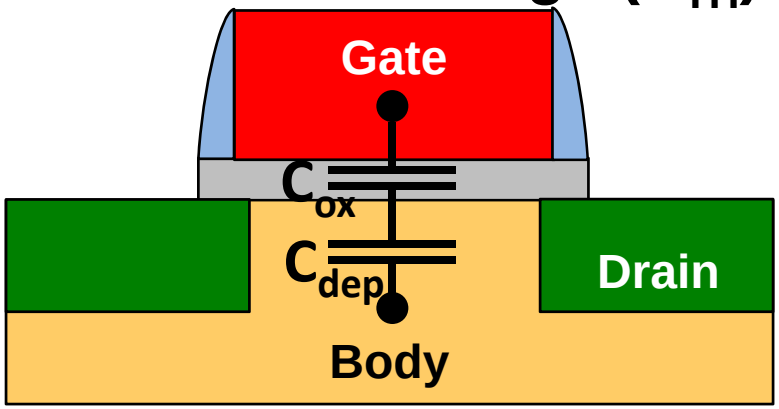


Output Characteristics

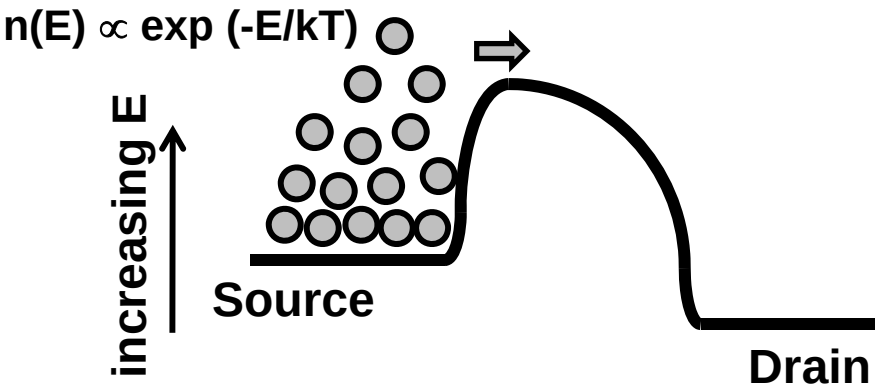


Review of Long Channel MOSFET

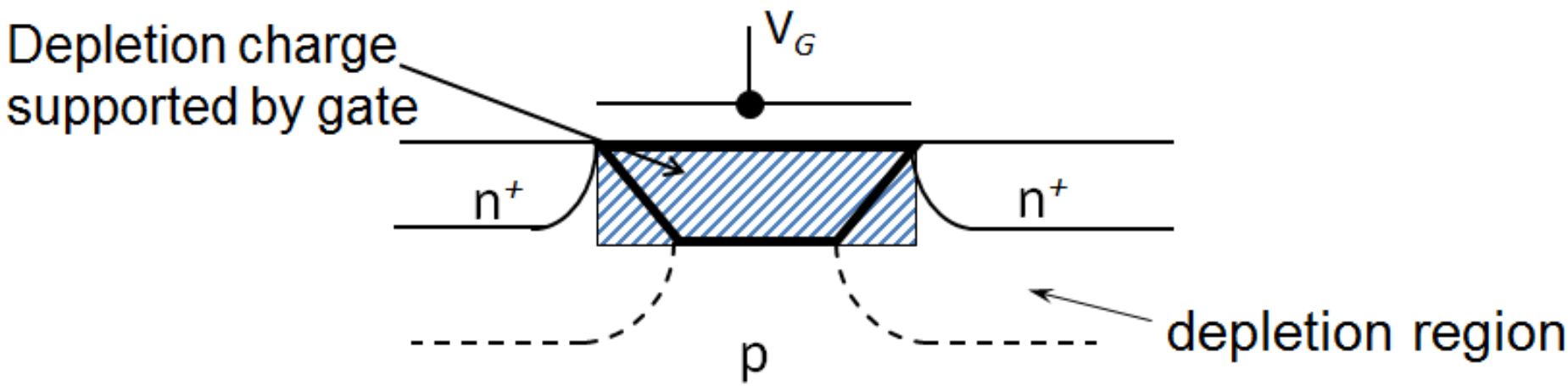
- **Threshold Voltage (V_{TH})**



- **Sub-threshold Swing (SS)**

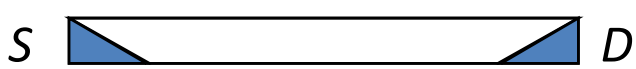


Short Channel Effect (SCE)



- **The smaller L_g is, the greater percentage of depletion charge balanced by the S/D PN junctions**

  <u>Long Channel</u>:



  <u>Short Channel</u>:

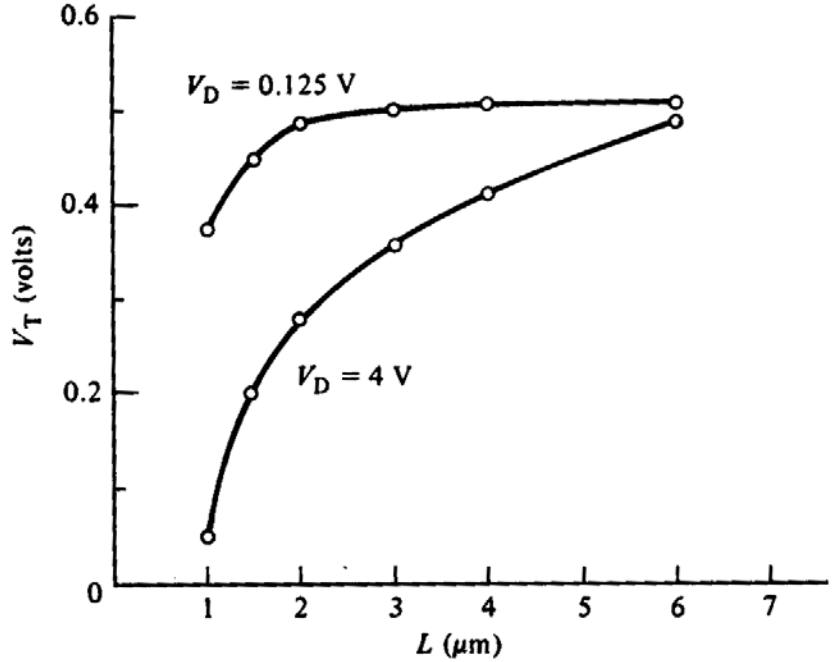
- **1st Order Analysis**

Quantitative Derivation of SCE: Yau's Model

L.-D. Yau, SSE (1974)

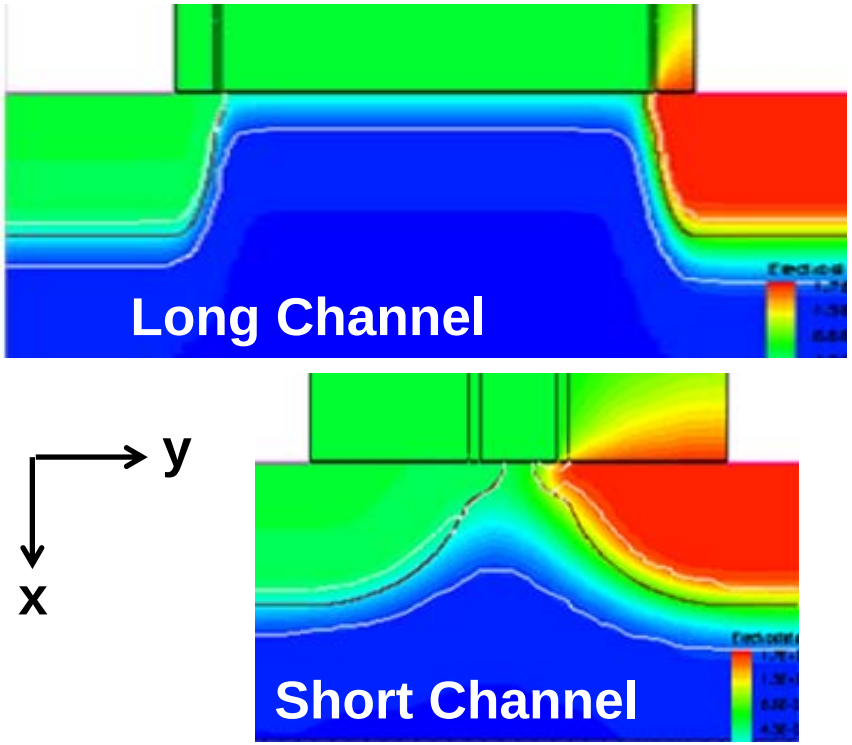
- **Depletion charge (Q_{dep}) reduction:**

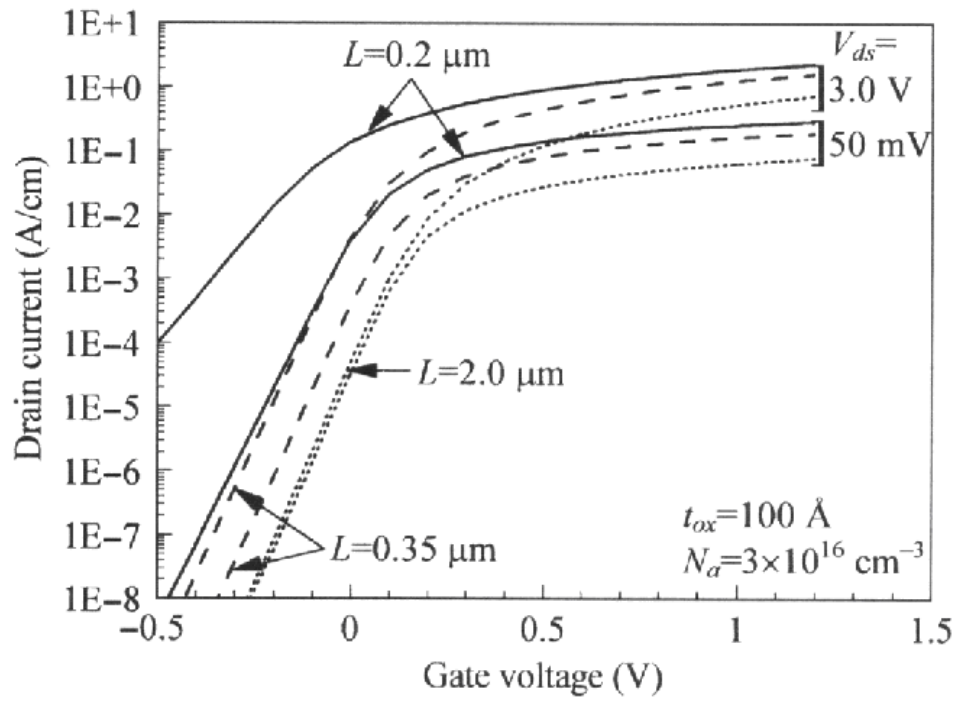
- **Threshold Voltage Lowering:**



- **Yau's model's assumptions:**
  - **Uses geometry relations instead of solving Poisson's equation**
  - **Assumes channel potential is linear along lateral (*i.e.* channel) direction**

Drain Induced Barrier Lowering (DIBL) - Qualitative





C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Figure 7-5

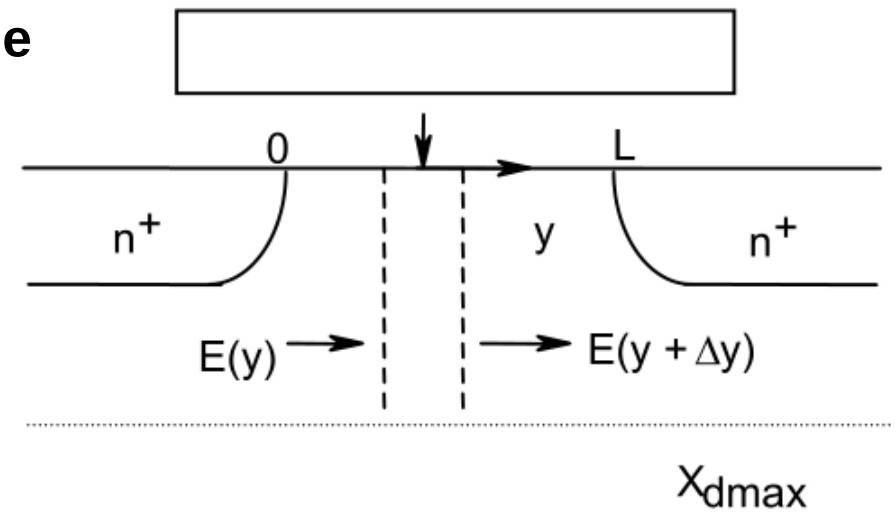
In short-L_g MOSFET:

- **x- and y- components of the electric field are coupled**
  → Drain bias will affect the barrier at source/channel
  → More band bending at given gate bias → V_T decreases

Derivation for DIBL
- A Quasi-2D Model

Steps:

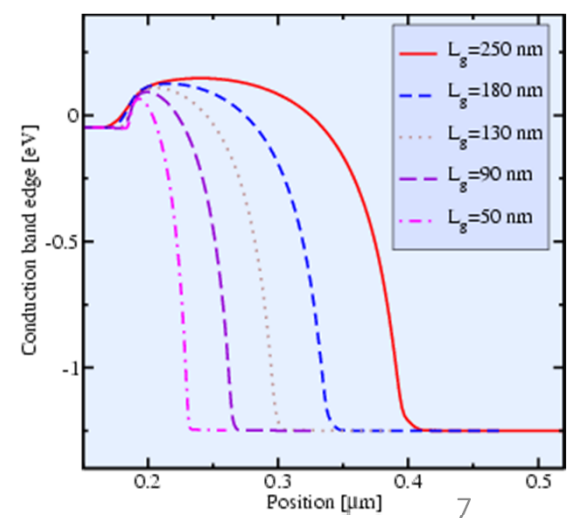
1. Develop Poisson's equation in the channel region, including x- and y-components.



2. Solve φ_S as a function of position (y)

$$\varphi_s(y) = V_{sL} + (V_{bi} + V_{DS} - V_{sL})\frac{\sinh(y/l)}{\sinh(L/l)} + (V_{bi} - V_{sL})\frac{\sinh((L-y)/l)}{\sinh(L/l)}$$

3. Calculate the peak of φ_S, which corresponds to V_{TH}. $V_{sL} = V_{GS} - V_T$



Scale Length – A Simplified Knob

1. **Tells how closely a MOSFET approaches a "short-channel" device.**

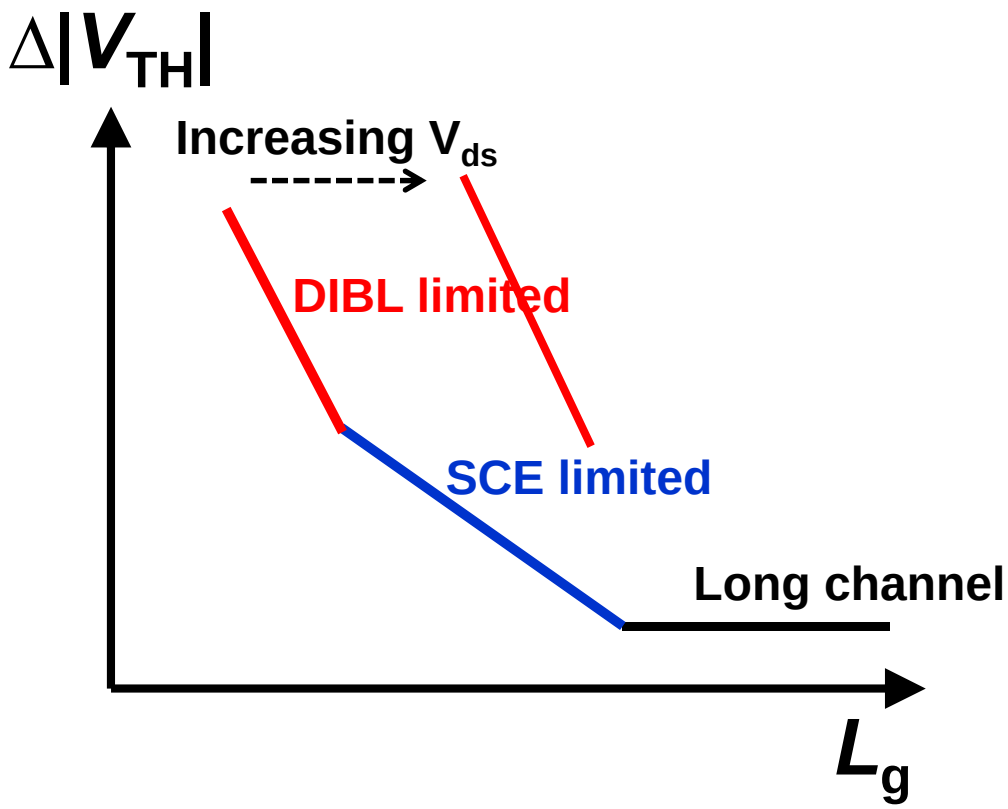
$$l \equiv \sqrt{\frac{\varepsilon_S T_{Ox} X_{d\max}}{\varepsilon_{Ox}}} = \sqrt{3 T_{Ox} X_{d\max}}$$

2. **Provides the guideline to scale a MOSFET while maintaining its electrostatic integrity.**

e.g. **for Planar Technology:**

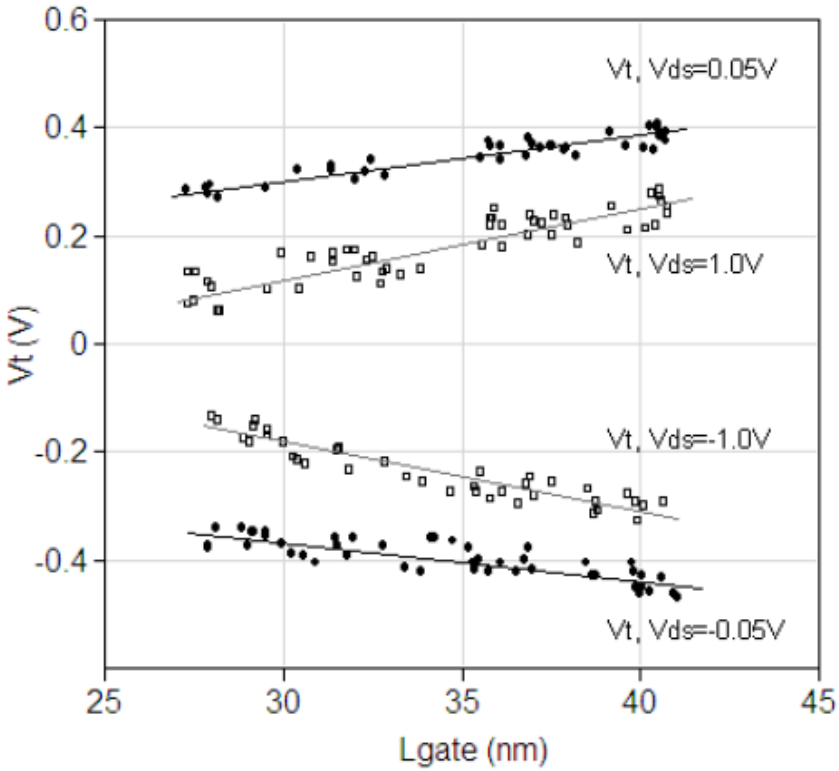
<u>Bulk</u> **<u>Ultra-Thin-Body</u>** **<u>Double-Gated FinFET</u>**

V_{TH} *vs.* L_g Plots: SCE + DIBL



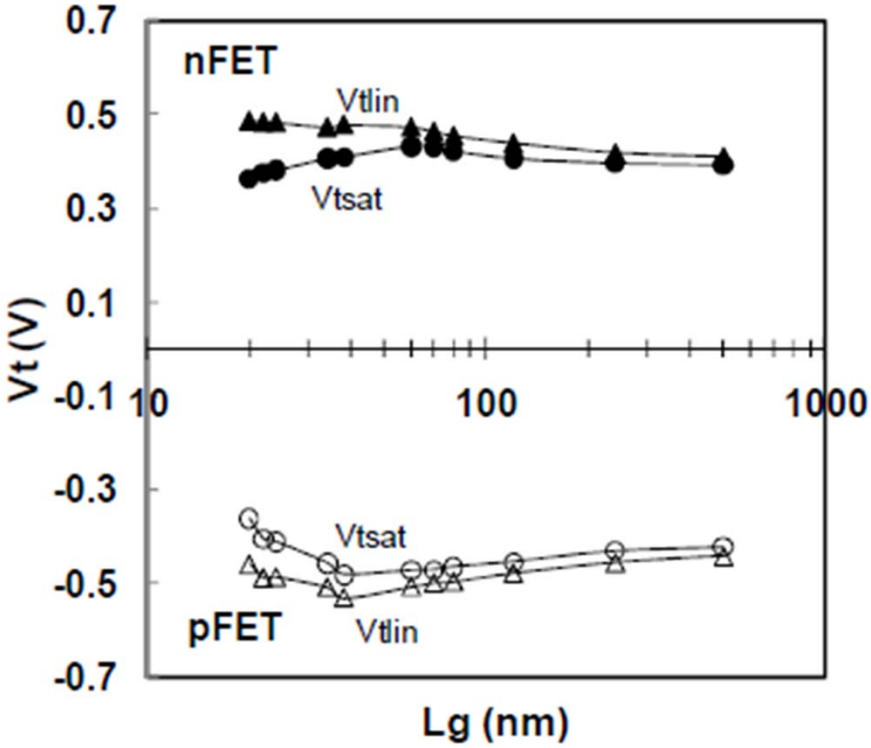
State-of-the-Art MOSFET's V_{TH} *vs.* L_g Plots

Intel's 32nm Bulk



P. Packan, IEDM (2009)

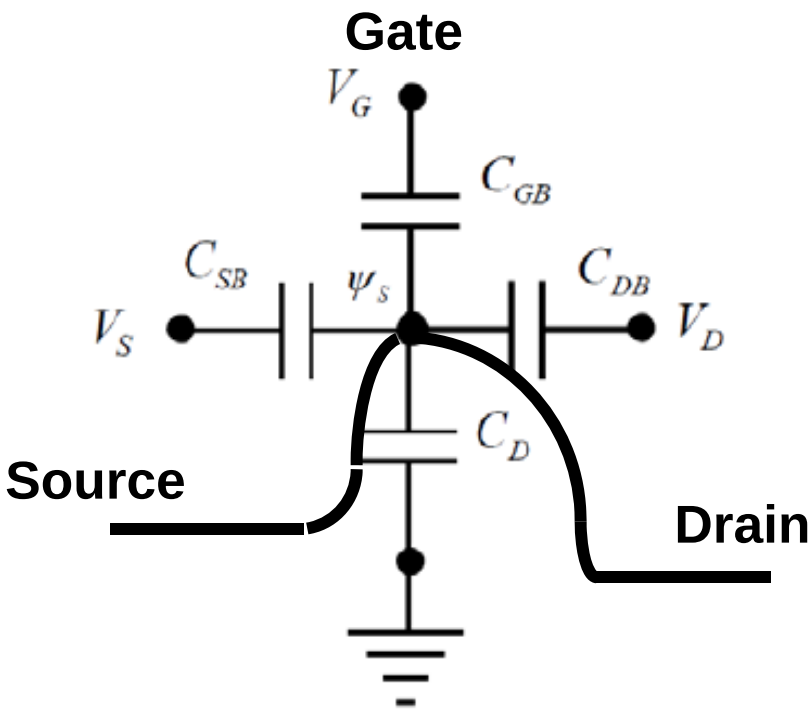
Samsung's 20nm Bulk



H.-J. Cho, IEDM (2011)

Sub-threshold Swing Degradation

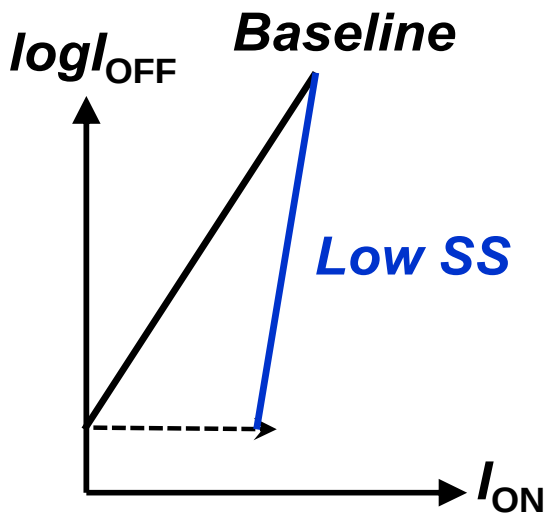
- **A 2-D Capacitor Network Model (after Prof. M. Lundstrom)**

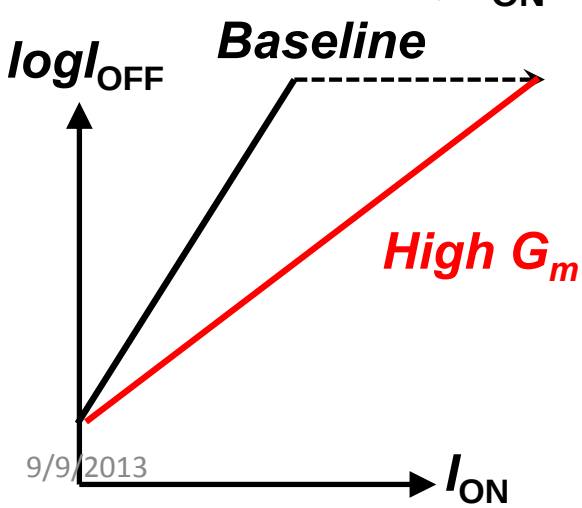


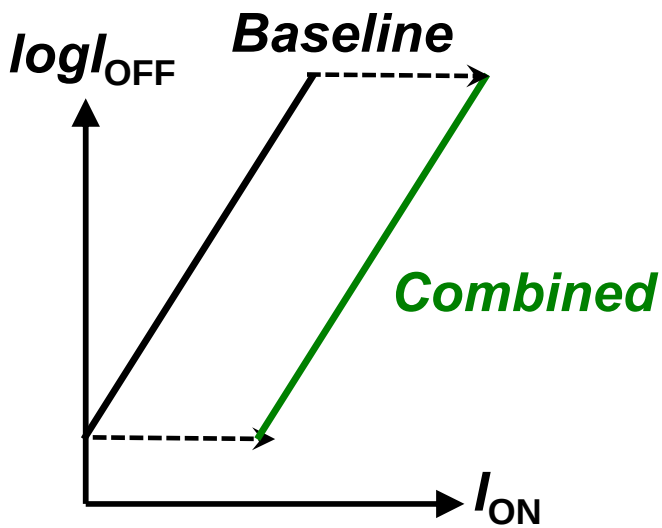
- **Impact of L_g Scaling on SS**

I_{OFF} *vs.* I_{ON} Plots

- Generated by "shifting" a device's V_{TH} under a fixed V_{DD}
- To benchmark the effectiveness of technology advancement.

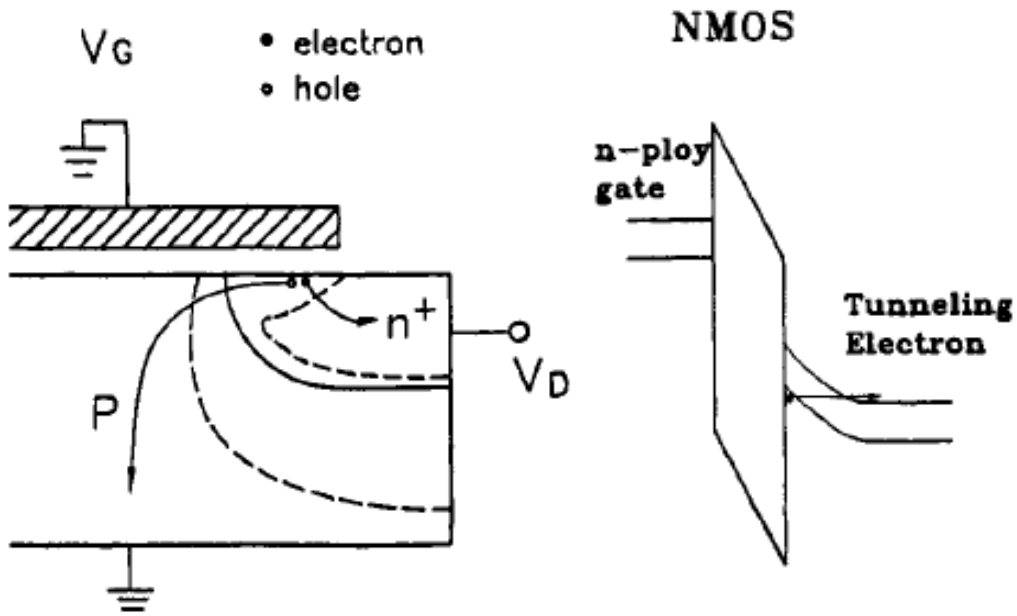




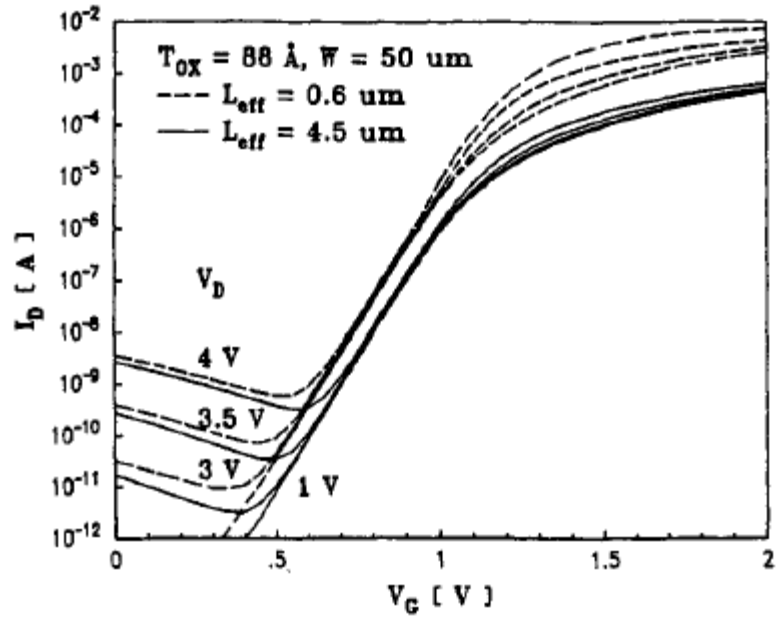


Gate Induced Drain Leakage (GIDL)

Illustration and Band Profiles

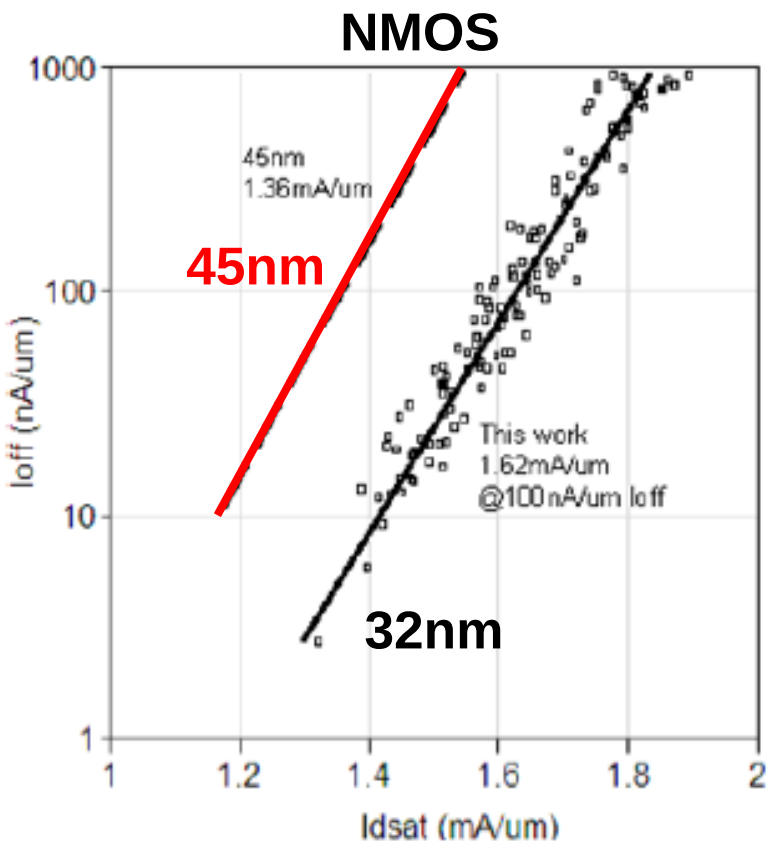


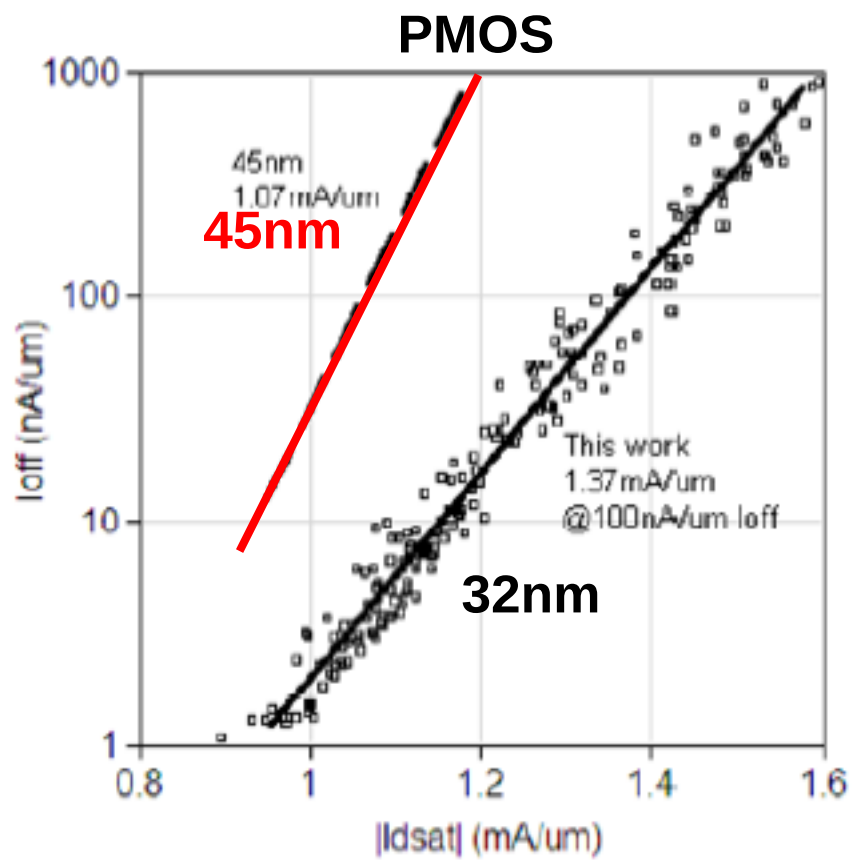
***I_d vs. V_{gs}* Characteristics**



T.-Y. Chan, IEDM (1987)

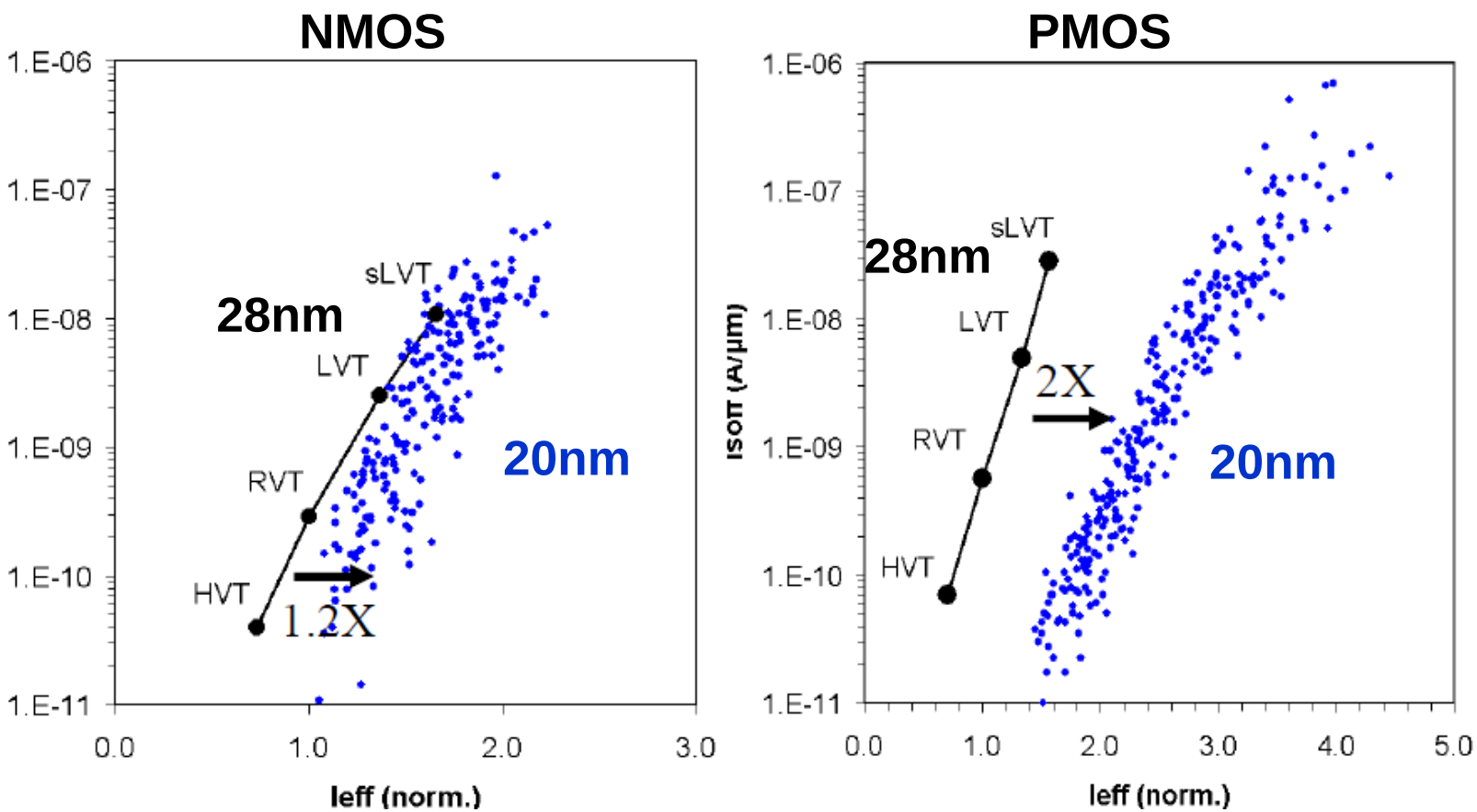
Intel's 32nm Bulk CMOS I_{OFF} *vs.* I_{ON} Plots





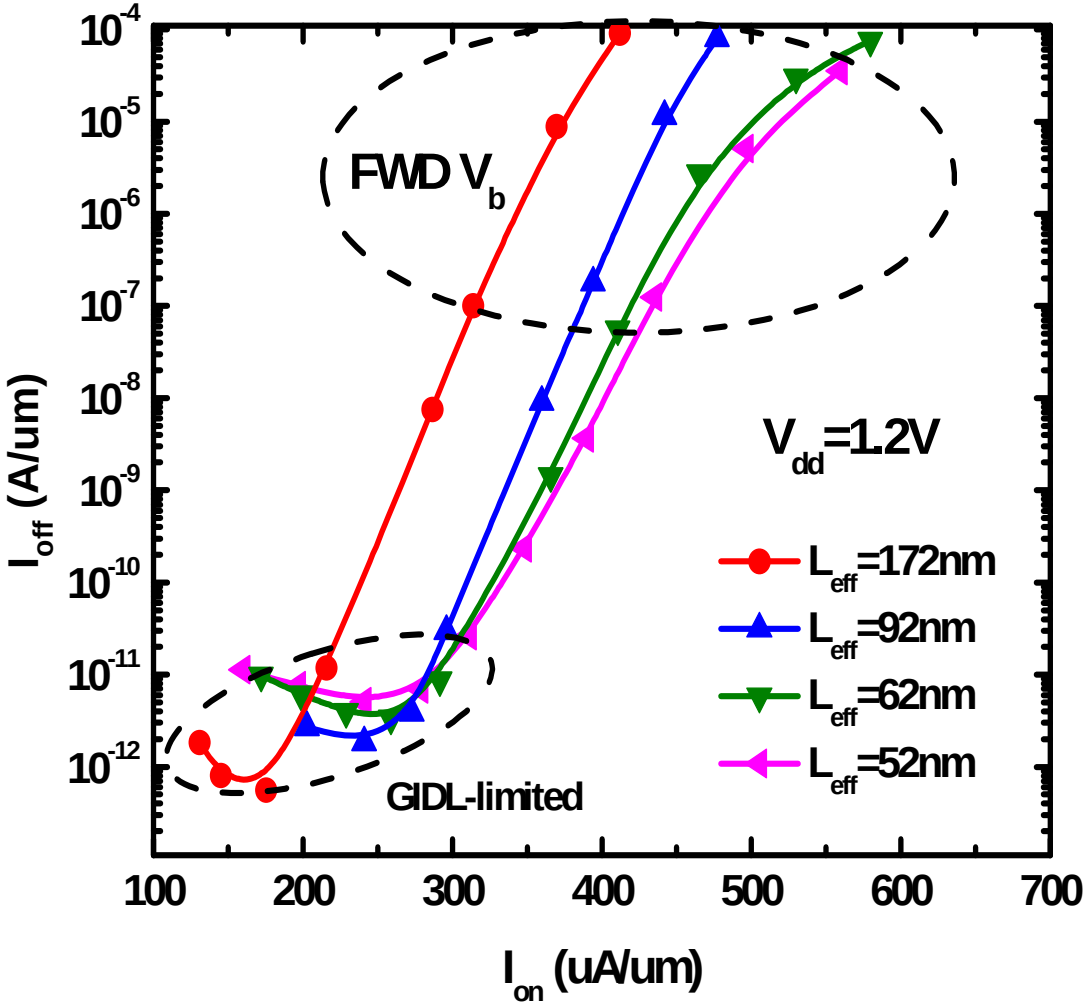
P. Packan, IEDM (2009)

IBM's 20nm Bulk CMOS I_{OFF} *vs.* I_{ON} Plots



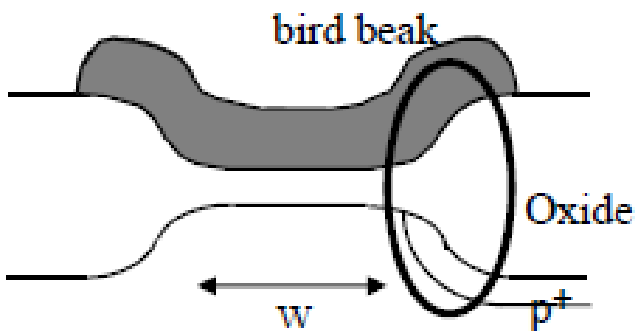
H. Shang, VLSI-T (2012)

GIDL-Limited I_{OFF} *vs.* I_{ON} Plots



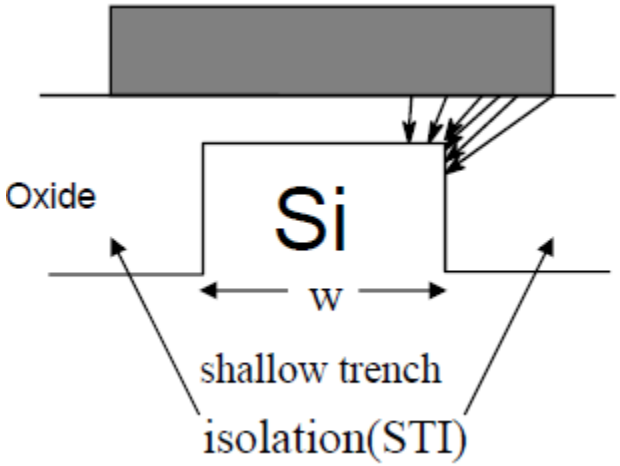
Narrow Width Effects

Narrow Width Effect



Reverse Narrow Width Effect

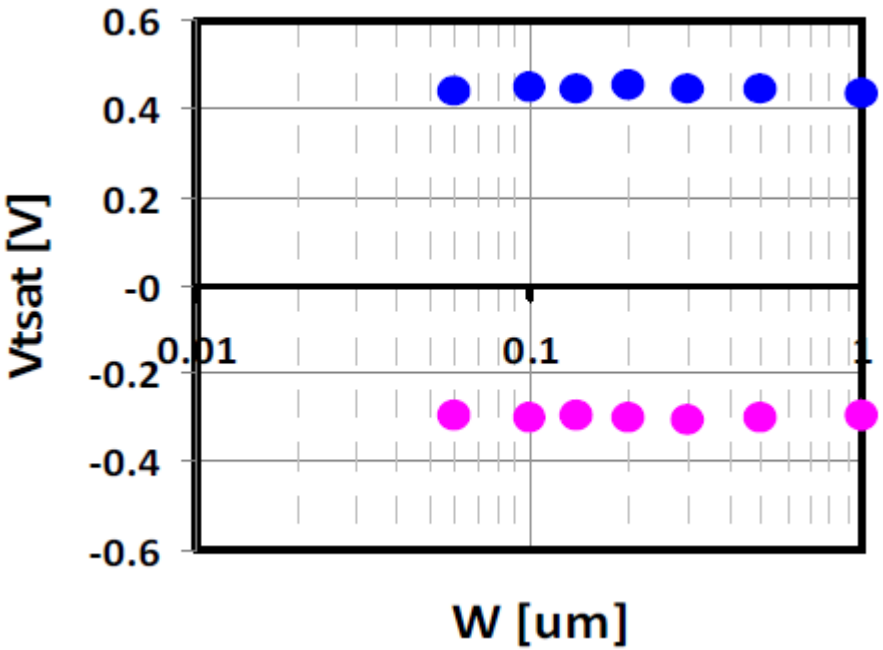
- A "Quasi-planar" MOSFET !



- **Narrow Width Effect is caused by LOCOS process.**
- **Reverse Narrow Width Effect is caused by STI process.**
- **Introduce problems as transistor *systematic variations*.**

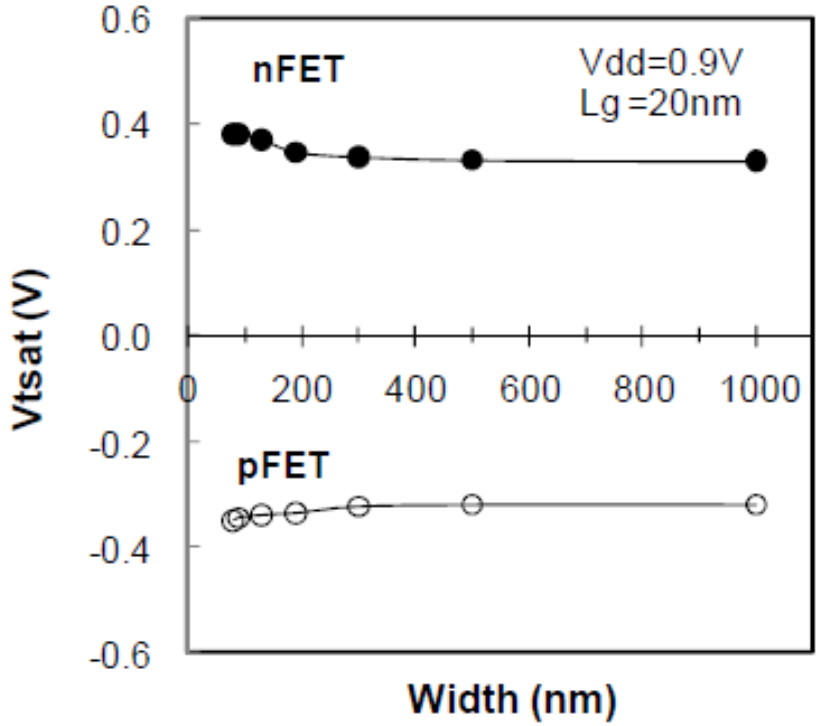
State-of-the-Art MOSFET's Narrow Width Effects

IBM's 20nm CMOS



H. Shang, VLSI-T (2012)

Samsung's 20nm CMOS



H.-J. Cho, IEDM (2011)

- **Thanks to advanced isolation techniques, narrow width effects are no longer problematic.**

Summary

- **How bad a planar bulk MOSFET is, <u>regarding electrostatics</u>?**

	I_d *vs.* V_g	I_d *vs.* V_d	V_g *vs.* L_g	I_{OFF} *vs.* I_{ON}
SCE				
DIBL				
SS Degradation				
Punchthrough				
GIDL				
Narrow Width Effects				

References

Short Channel Effects

1. (SCE) L.-D. Yau, "A Simple Theory to Predict the Threshold Voltage of Short-Channel IGFET's," Solid State Electronics, Vol.17, pp. 1059-1063, 1974.

2. (Scale Length) R.-H. Yan, A. Ourmazd, K.F. Lee, "Scaling the Si MOSFET: from Bulk to SOI to Bulk," *IEEE Transactions on Electron Devices,* Vol. 39, Issue 7, pp. 1704-1710, 1992.

3. (2D Capacitor) M. Lundstrom, "2D MOS Electrostatics," *NanoHub Online Resources at http://nanohub.org/resources/15617/download/nanoHUB-U-Lundstrom-L2.5.pdf*, 2012.

4. (GIDL) T.-Y. Chan, J. Chen, P. K. Ko, C. Hu, "The Impact of Gate-Induced Drain Leakage Current on MOSFET Scaling," *IEEE International Electron Devices Meeting Technical Digest*, pp. 87-90, 1987.

Industry Bulk CMOS Platforms

5. (Intel 32nm HP) P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier *et al*., "High Performance 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors," *IEEE International Electron Devices Meeting Technical Digest*, pp. 659-662, 2009.

6. (Samsung 20nm) H.-J. Cho, K.-I. Seo, W.C. Jeong, Y.-H. Kim, Y. D. Lim *et al.,* "Bulk Planar 20nm High-K/Metal Gate CMOS Technology Platform for Low Power and High Performance Applications," *IEEE International Electron Devices Meeting Technical Digest*, pp. 350-353, 2011.

7. (IBM 20nm) H. Shang, S. Jain, E. Josse, E. Alptekin, M. H. Nam et al., "High Performance Bulk Planar 20nm CMOS Technology for Low Power Mobile Applications," *Symposium on VLSI Technology Digest*, pp. 129-130, 2012.