EE 290D: Advanced Topics in Semiconductors
- *3-D Transistor Technologies*

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Administrative

1. **Course Focus**
2. **Course Webpage**

   http://www-inst.eecs.berkeley.edu/~ee290d/fa13/
3. **Office Hours (TBD)**
4. **Course Prerequisites**

   EE 130, EE 105
5. **References**

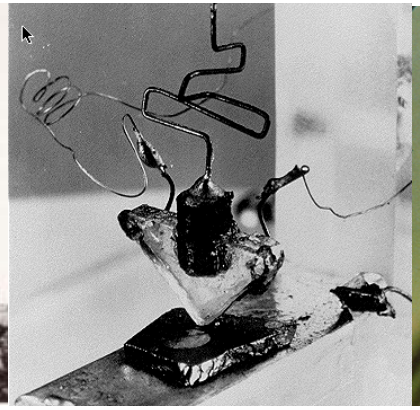
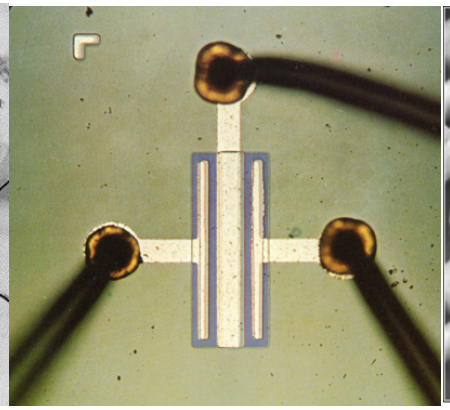
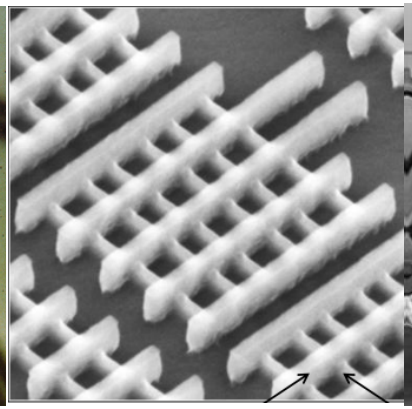
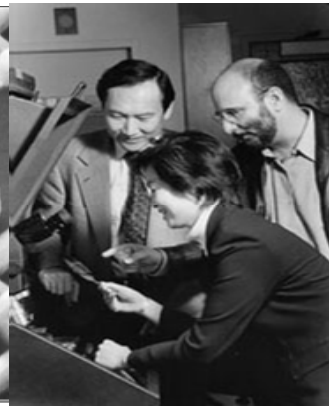
   Primarily based on lecture notes

   No required texts
6. **Grading**

   HW (30%): 3 assignments

   Midterm Exam (40%): Take-home, 48 hrs

   Project/Presentation (30%)

Lecture 1

- Course Overview
  - Concepts of Thin-Body MOSFETs
  - History of FinFET Development

<u>Reading</u>: multiple research articles (reference list at the end of this lecture)

A Journey Back through Time…

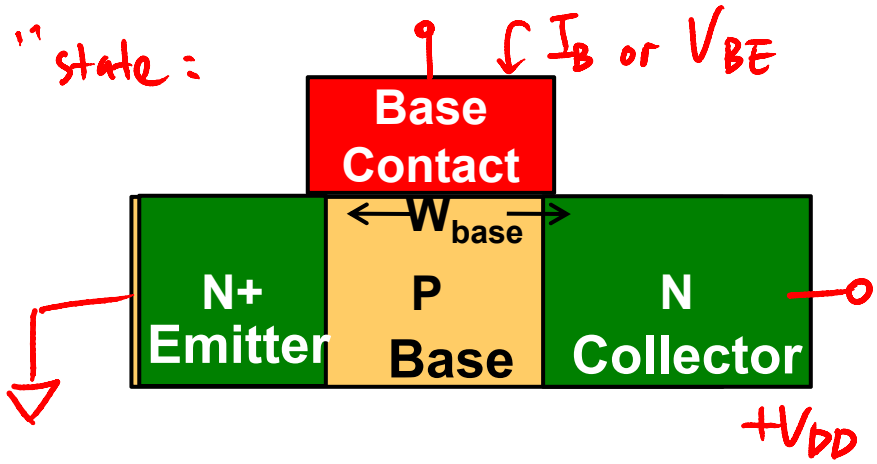
Notice of Courtesy:
Lots of materials here are from Prof. Tsu-Jae King Liu's various talks on advanced CMOS devices

1950s: Diffusive Transistors

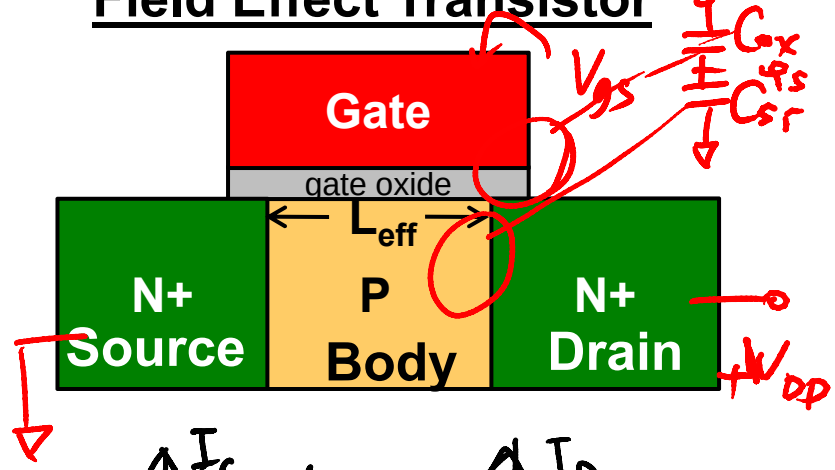
E (S) — C (D) — I — ⊥ Control Voltage

1947: Bipolar Junction Transistor

"ON" state:



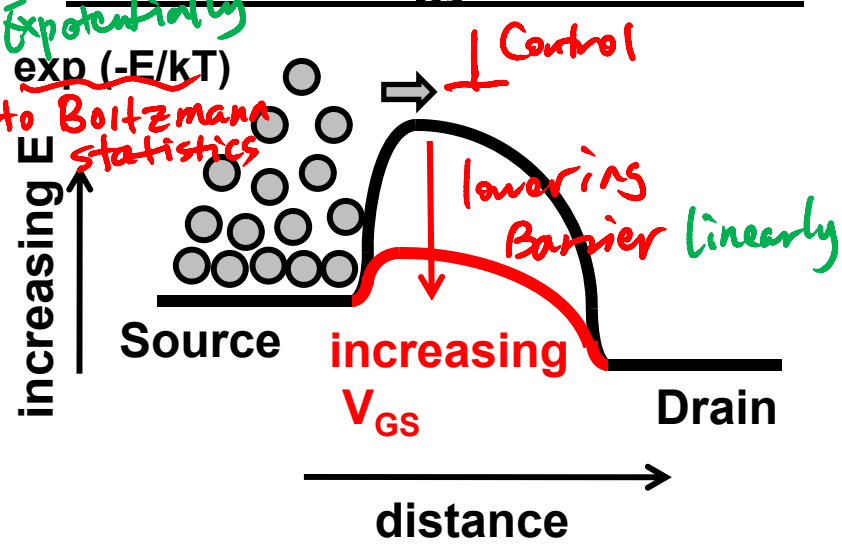
1959: Metal-Oxide-Semiconductor Field Effect Transistor

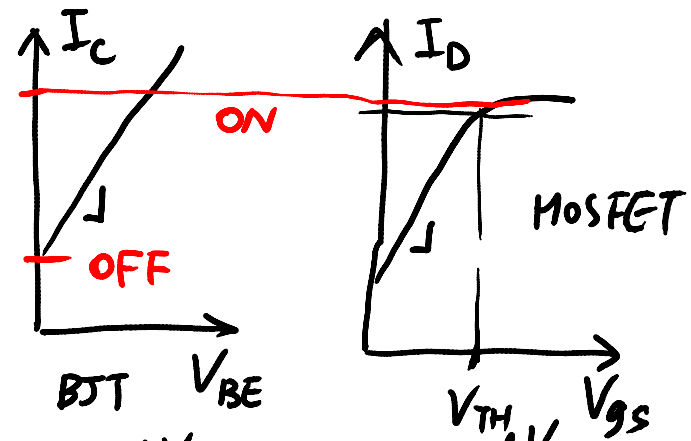


Electron Energy Band Profile

$n(E) \propto \exp(-E/kT)$

Exponentially due to Boltzmann statistics





$$\text{slope} \equiv \frac{dV_{BE}}{d\log_{10} I_C} = \frac{k_B T}{q} \ln 10 = 60\,\text{mV/dec}$$

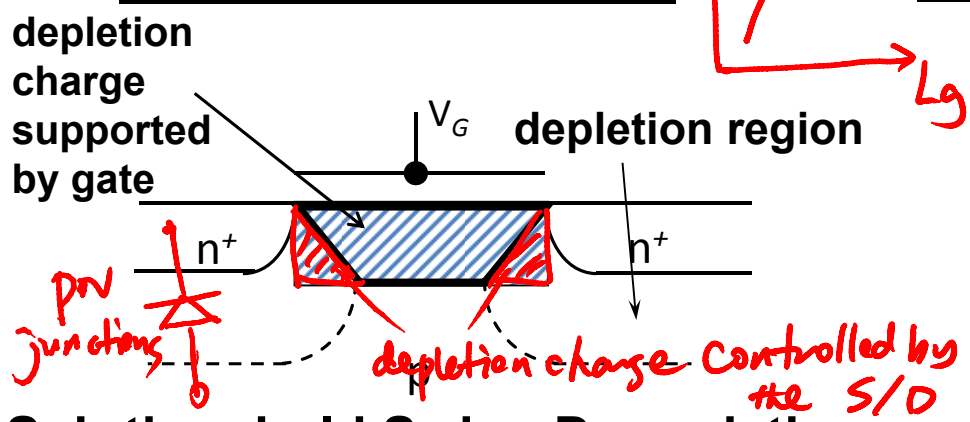
$$\text{slope} \equiv \frac{dV_{gs}}{d\log_{10} I_D} = 60\,\text{mV/dec} \cdot \left(1 + \frac{C_{sr}}{C_{ox}}\right)$$

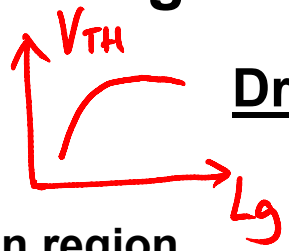
why this term appear?

1990s: Short L_g MOSFET Effects

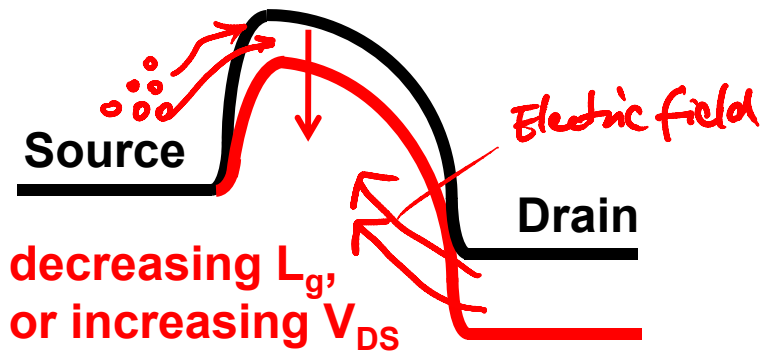
(Below 1 μm Lg)

Short Channel Effects

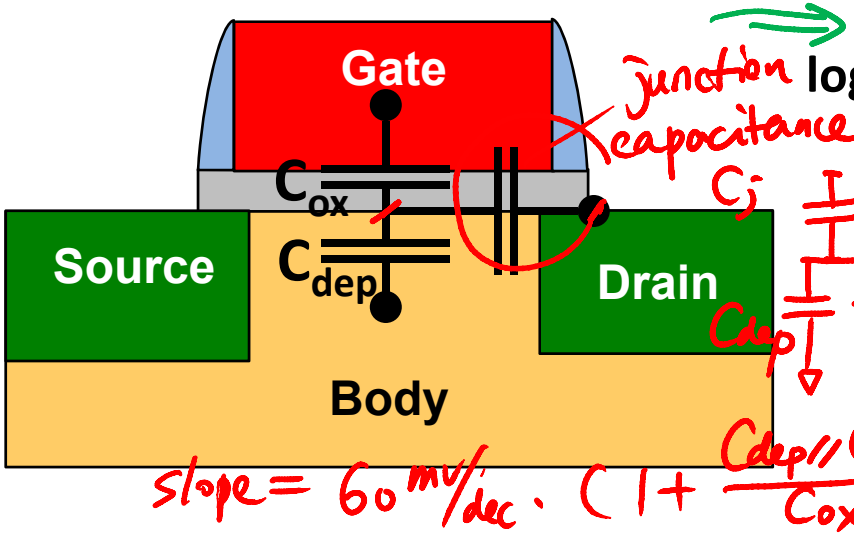


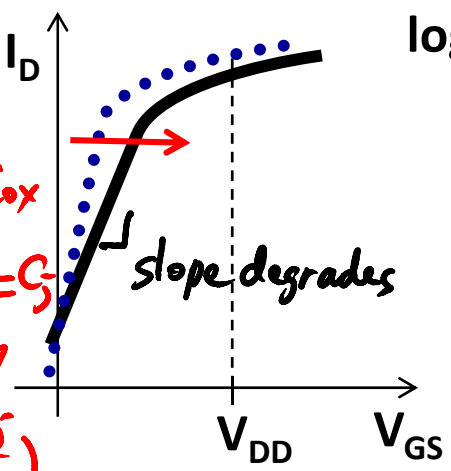


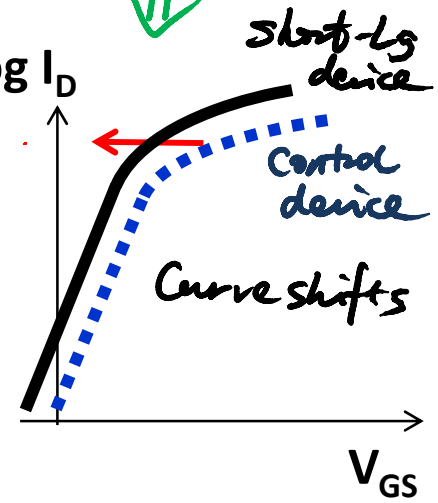
Drain Induced Barrier Lowering



Sub-threshold Swing Degradation

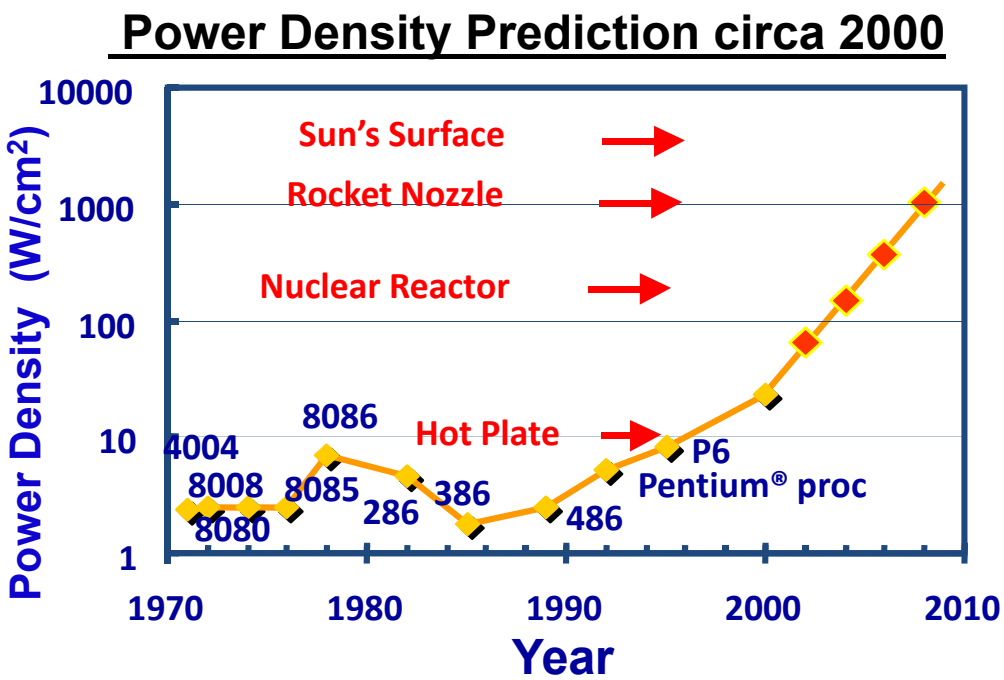




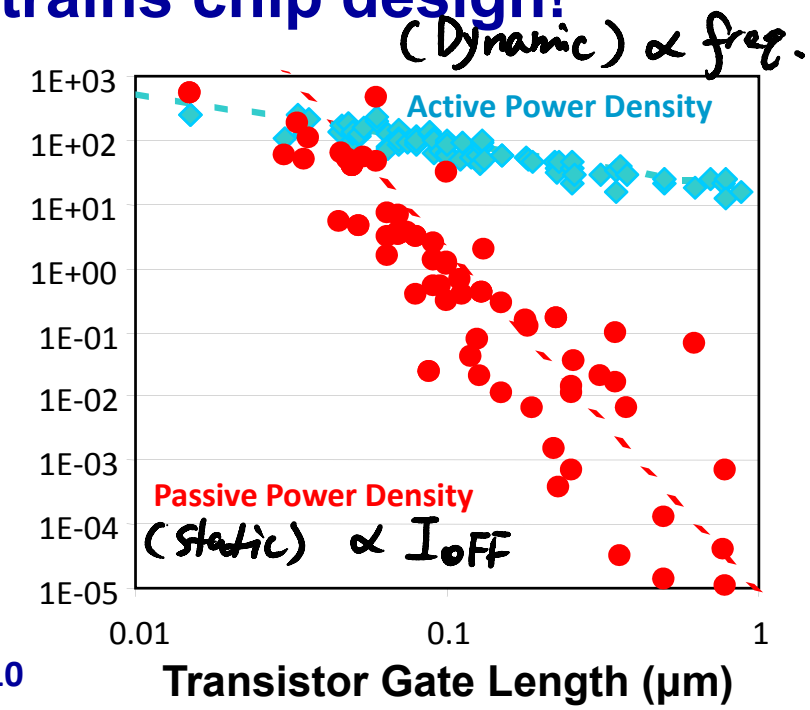


2000s: The IC Power Crisis

- **As transistor density has increased, the transistor operating voltage has not decreased proportionately.**
  → Power density now constrains chip design!



Source: S. Borkar (Intel)



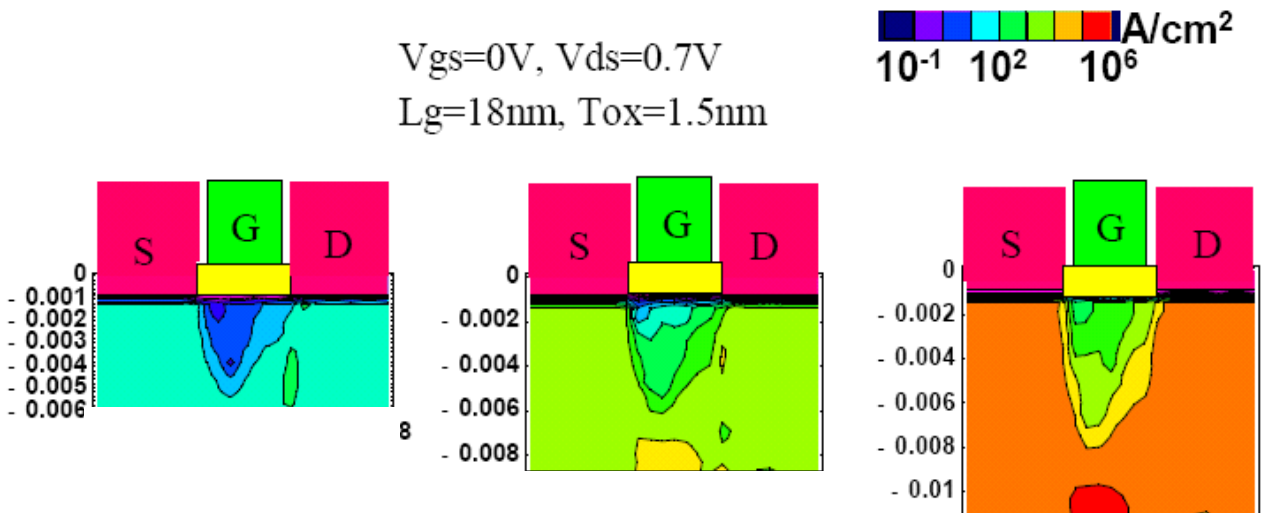
Source: B. Meyerson (IBM)
Semico Conf., January 2004

- **Transistor innovations are needed to alleviate this crisis.**

Impact of Body Thickness

- TCAD Simulation results

Courtesy of Prof. C. Hu



Tsi=5nm Tsi=7.5nm Tsi=10nm

Thin body – 1000x lower leakage current !!!

By reducing T_{si}

1. $C_j \downarrow \Rightarrow$ better SS
2. reduced electrical field coupling $\Rightarrow$ improved DIBL
3. less charge controlled by source/Drain $\Rightarrow$ improved short channel effect.

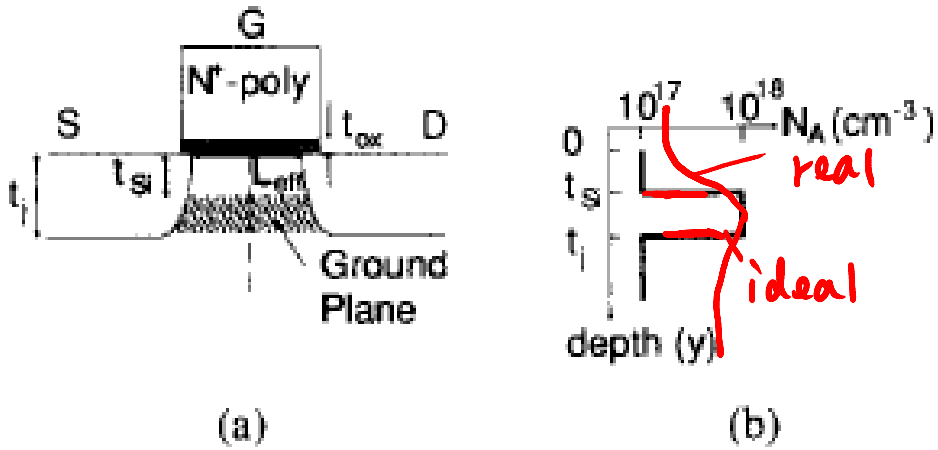
Planar MOSFET Scaling Technique: Retrograde Well Doping

(channel) epi-Si

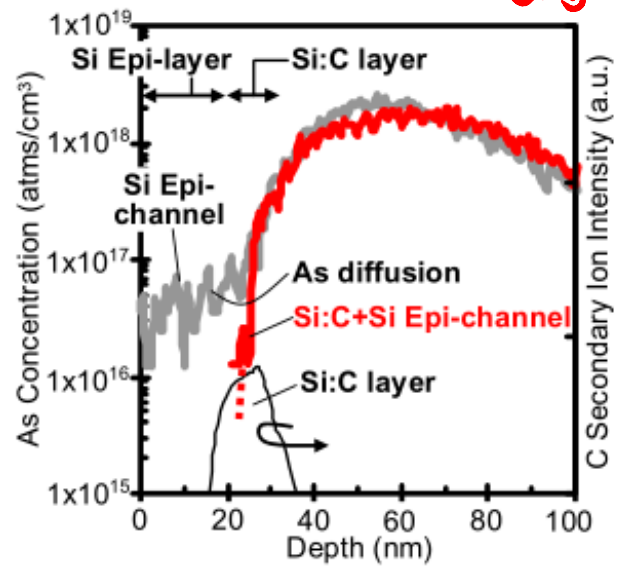
screen layer

sub

"δ-doping"



R.-H. Yan, T-ED(1992)



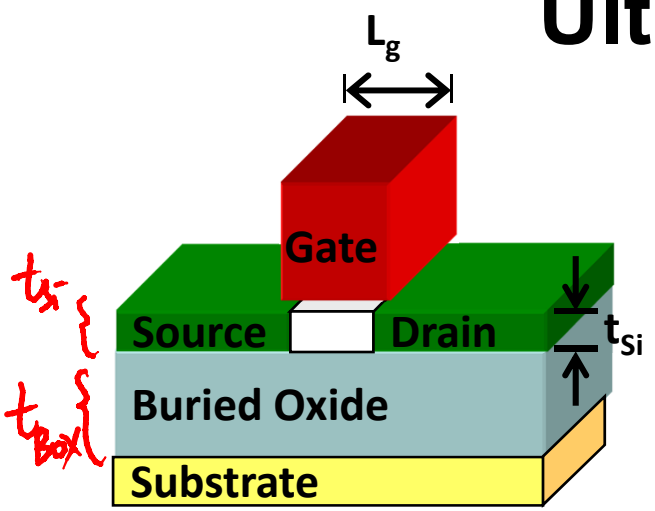
A. Hokazono, VLSI-T(2008) & IEDM(2009)

Epi-enhanced Cost; Not scalable

- Use high doping to "turn off" the sub-channel leakage path.
- Channel is kept undoped, ideally. Gaussian doping profile → effective Slop ≐ 15 nm/dec
- Steep retrograde doping gradient is a limiting factor.
  - ➢ Exotic materials have to be used (Si:C, Si:N, *etc*.) as a screen layer

can achieve as steep as 2 nm/dec

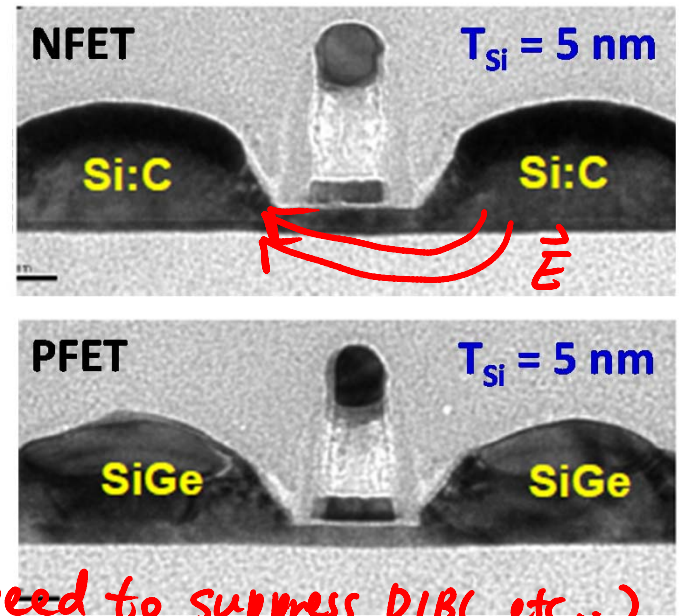
Planar MOSFET Scaling Technique: Ultra-Thin-Body SOI



- "Remove" the MOSFET substrate by fabricating it on the SOI wafer.
- No channel doping. (No need to suppress DIBL, etc..)
- Channel and BOX thicknesses are knobs to tune the device electrostatics.

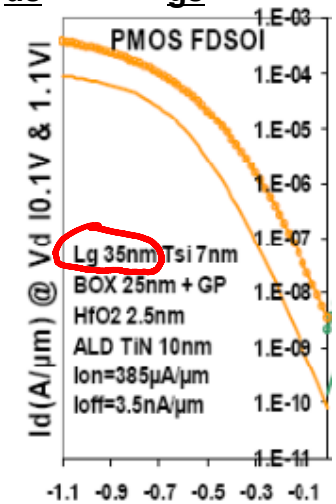
Cons:
1. High substrate cost
2. $\vec{E}$-field coupling through BOX

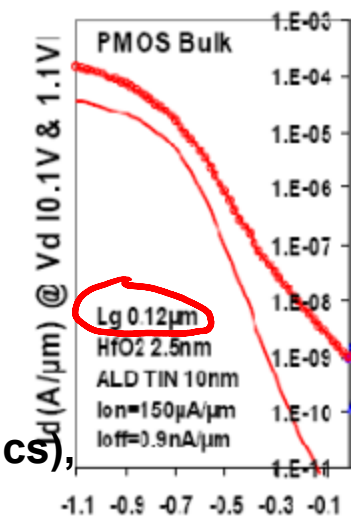
IBM's 20 nm UTB-SOI MOSFETs



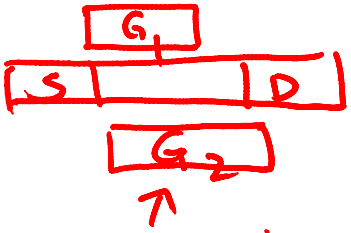
K. Cheng (IBM), IEDM(2009)

I_{ds} *vs.* V_{gs} Curves





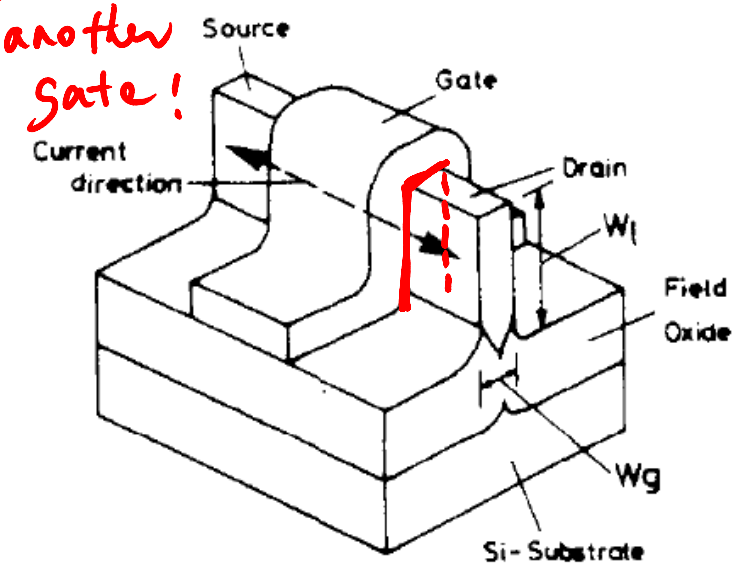
C. Fenouillet (STMicroelectronics), IEDM(2009)



1990: Delta MOSFET

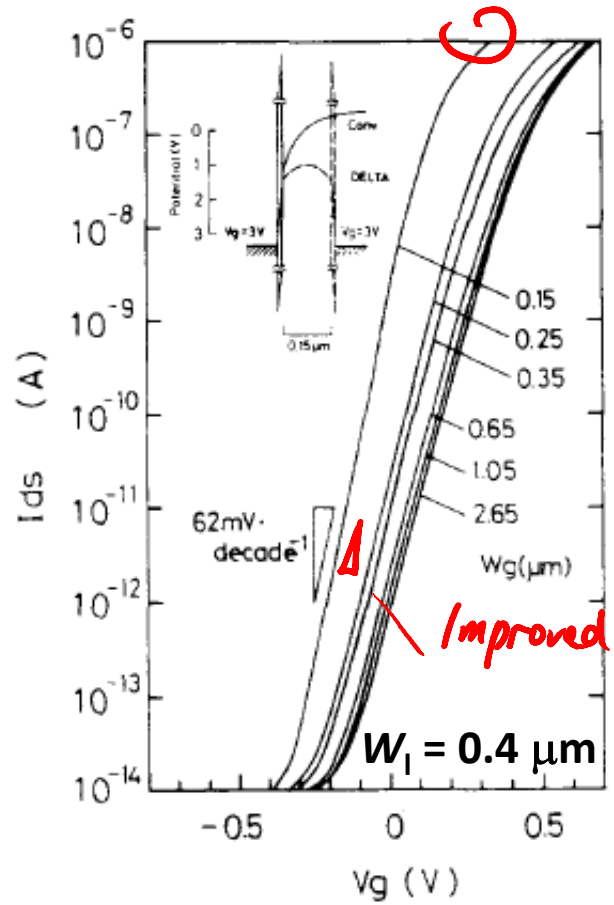
(Hitachi Central Research Laboratory)

Add another gate!



D. Hisamoto, EDL(1990)

Improved Ion

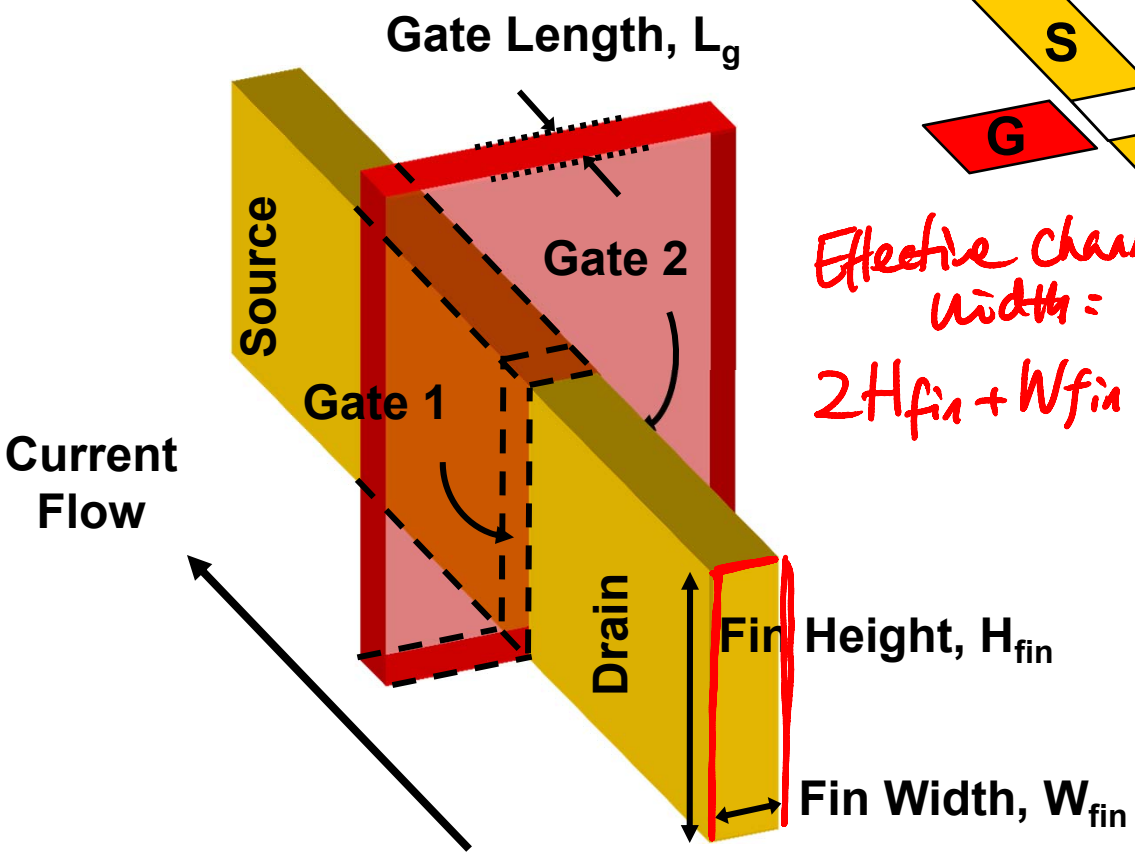


Improved Swing

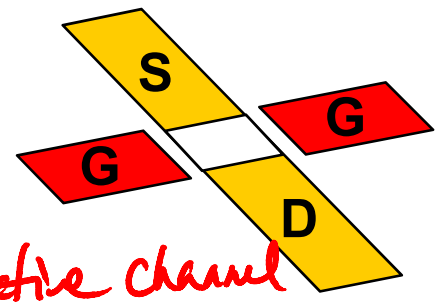
- Improved gate control observed for W_g < 0.3 um
  - L_{eff}= 0.57 um

FinFET Concepts

- **Self-aligned gates straddle narrow silicon fin**
- **Current flows parallel to wafer surface**



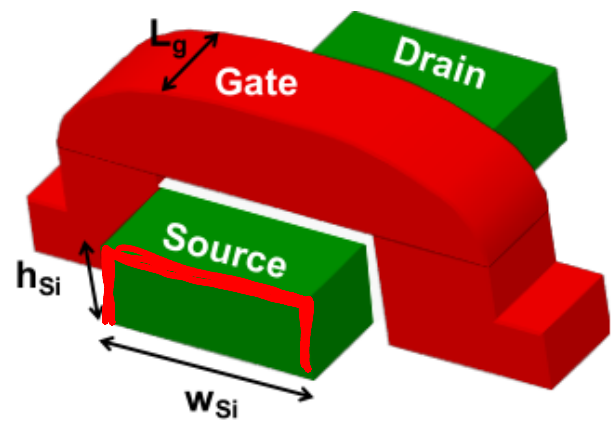
Tall & Narrow



Effective channel width:

$2H_{fin} + W_{fin}$

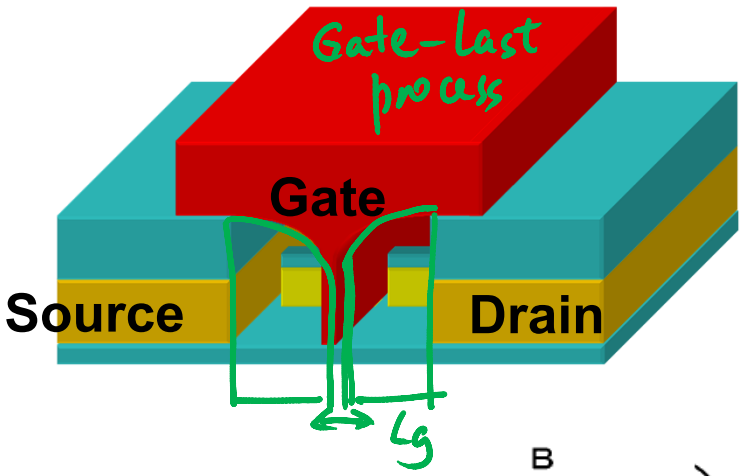
Design Variations



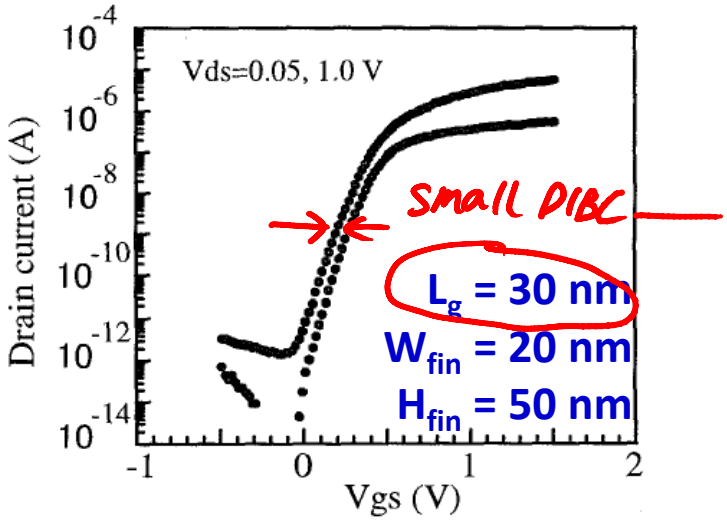
Short & Fat

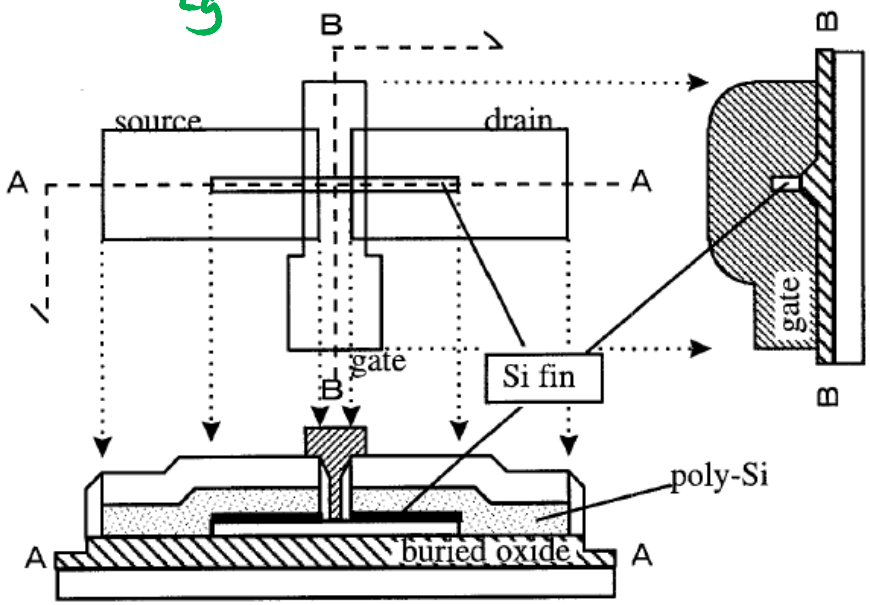
1998: 1st N-Channel FinFET

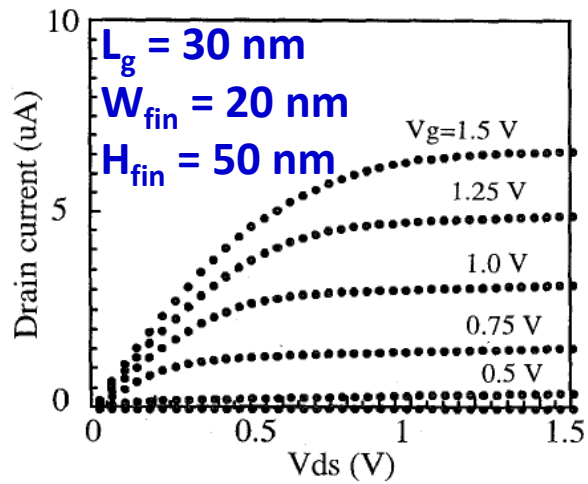
(UC Berkeley)



- Gate-last flow was used originally.







D. Hisamoto, IEDM(1998)

1999: 1st P-Channel FinFET
(UC Berkeley)

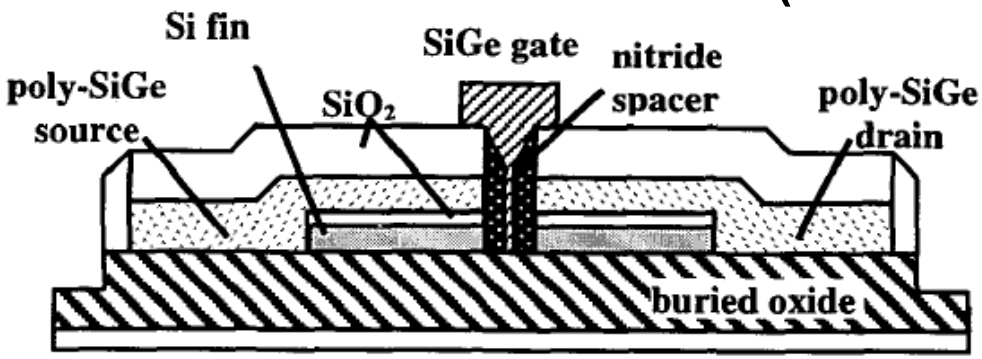
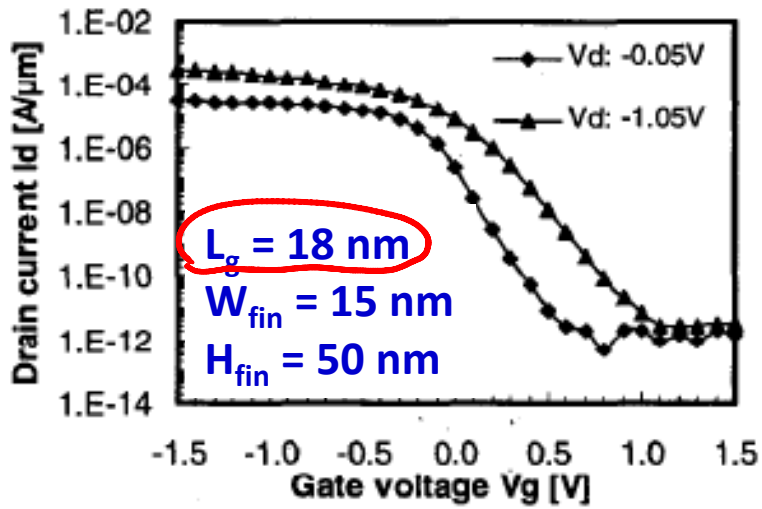
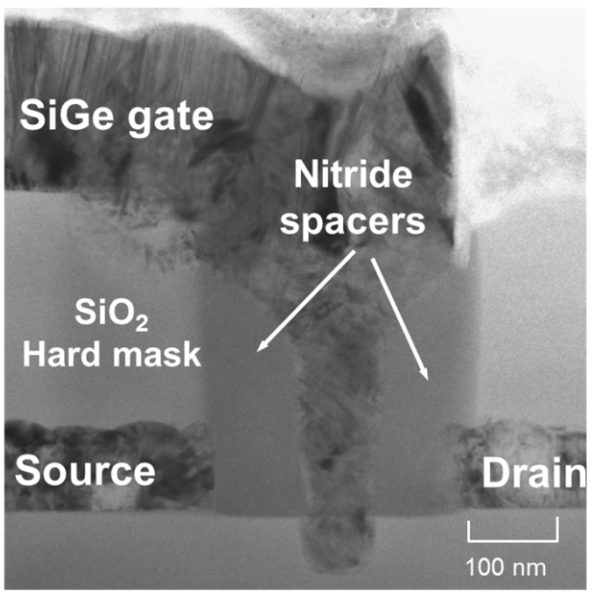
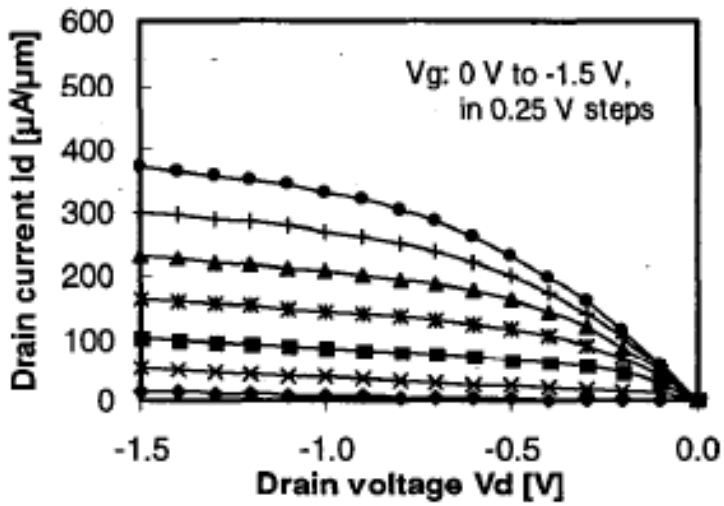


Figure 1: Schematic drawing of FinFET





Transmission Electron Micrograph

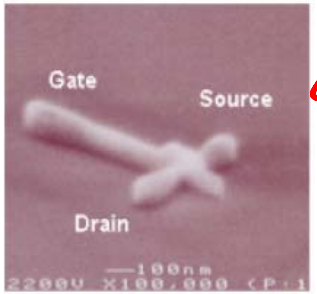


X. Huang, IEDM(1999)

2002: 10 nm L_g FinFETs

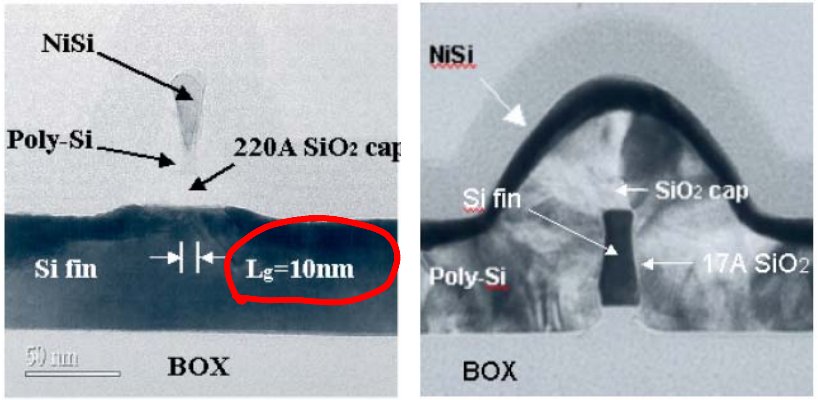
(AMD & UC Berkeley)

SEM image:

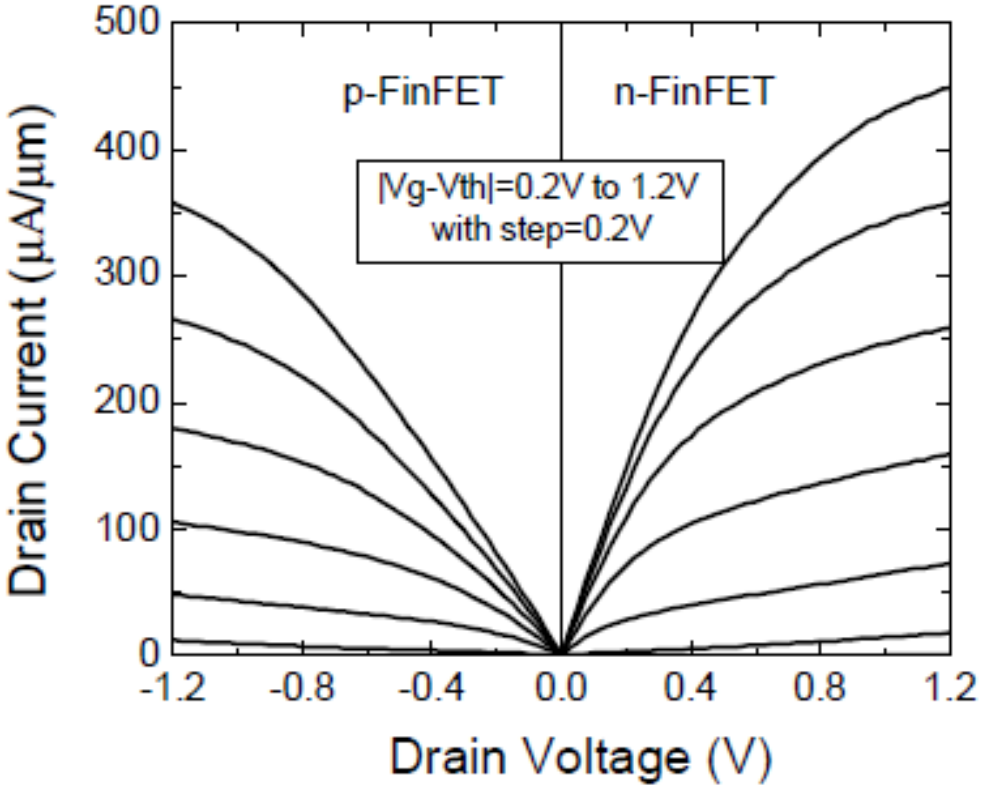


By lithography

TEM images



Output Characteristics

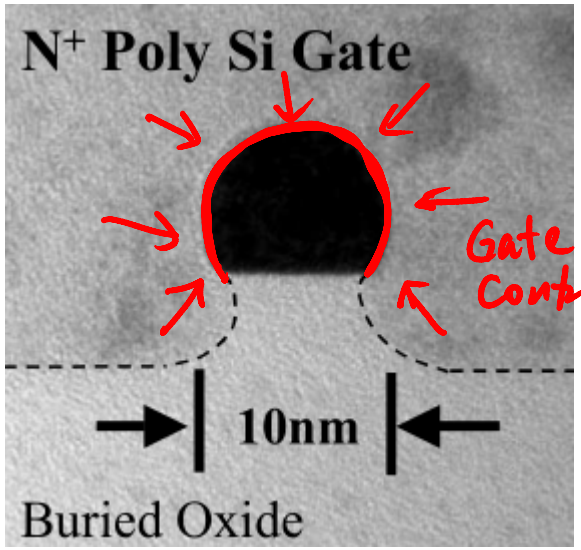


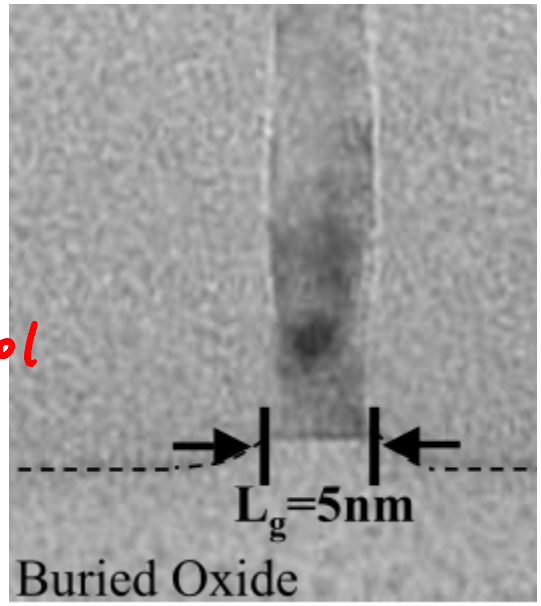
B. Yu, IEDM(2002)

2004: 5 nm L_g FinFETs

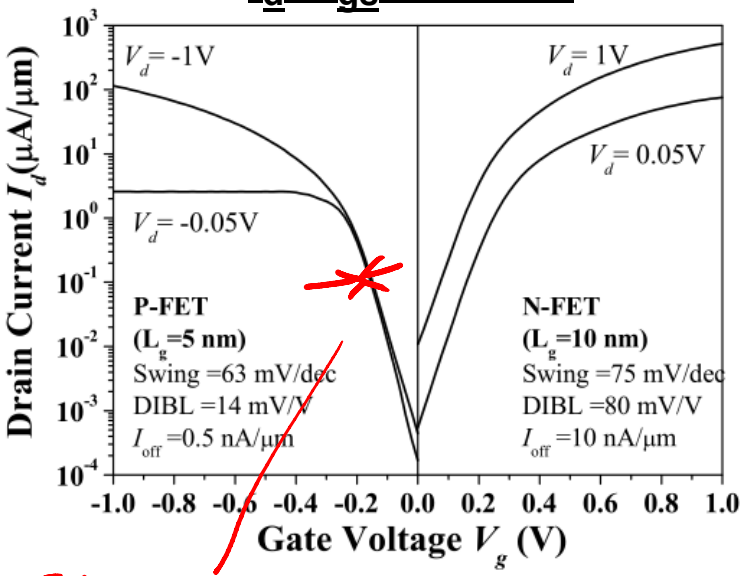
(TSMC)

TEM images





I_d-V_{gs} Curves

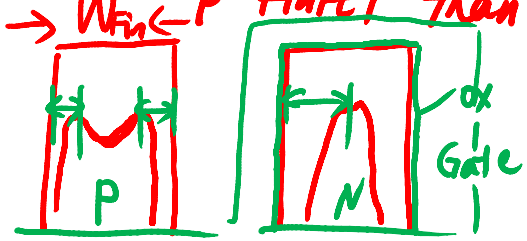


a "Gate-All-Around" device

N/p mismatch is smaller in FinFETs than in planar MOSFETs

Extremely small DIBL, due to smaller inversion thickness in P-FinFET than n-FinFET

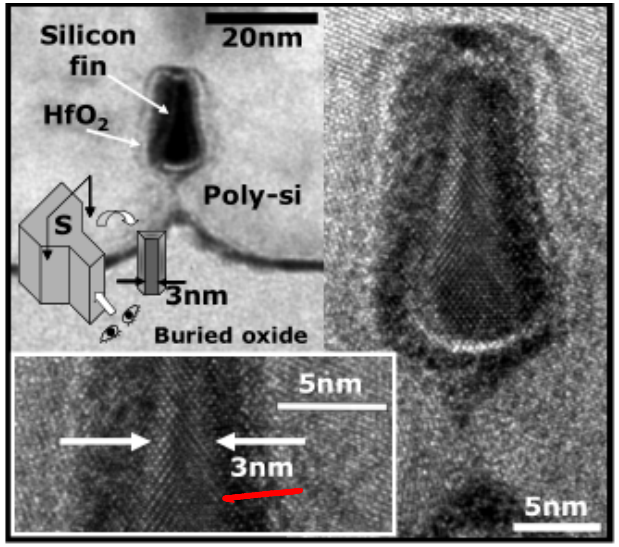
→ W_{Fin} ←

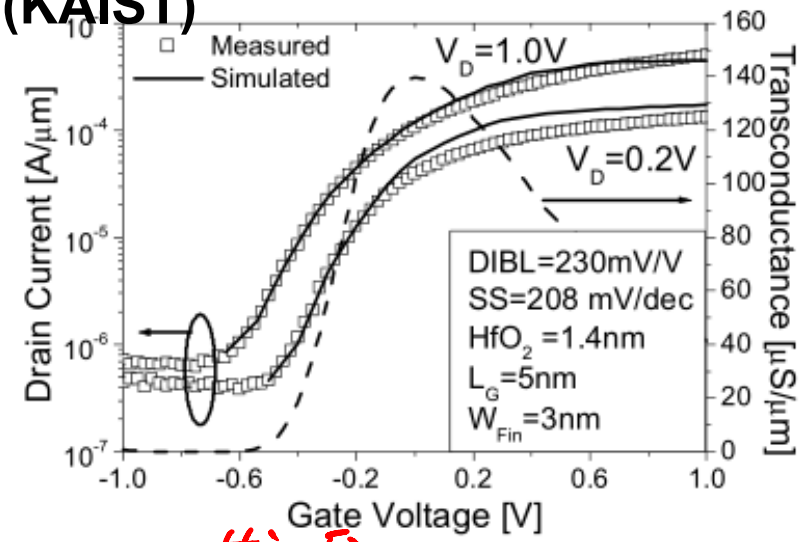


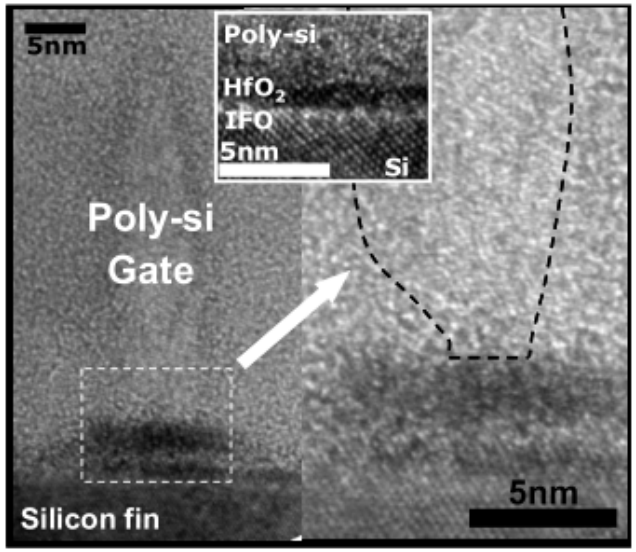
F.-L. Yang, VLSI-T(2004)

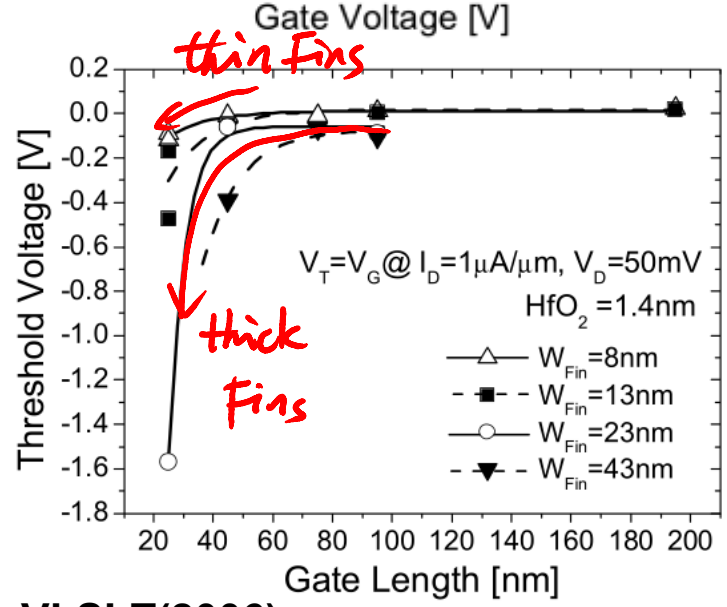
2006: 5 nm L_g, 3 nm W_{Fin} FinFETs

(KAIST)









H. Lee, VLSI-T(2006)

2004: 1st Bulk FinFET

(Samsung)

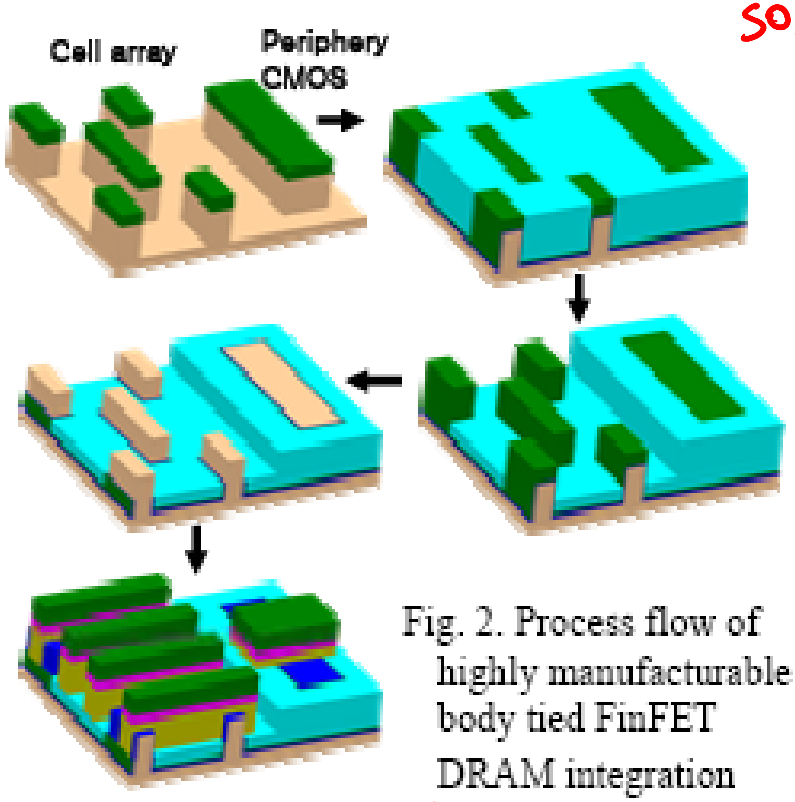
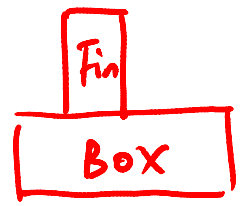


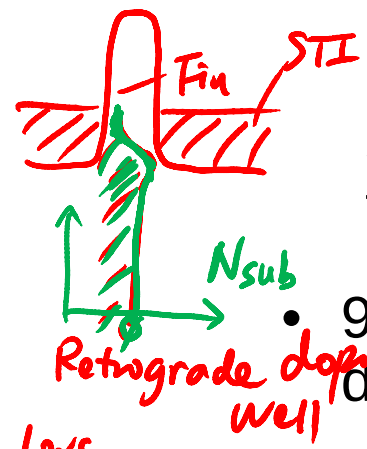
Fig. 2. Process flow of highly manufacturable body tied FinFET DRAM integration

for DRAM access transistors, require extremely low I_{OFF}

SOI FinFETs:



Bulk FinFETs:



- **FinFETs can be made on bulk-Si wafers**
  - ✓lower cost
  - ✓improved thermal conduction

  with super-steep retrograde well (SSRW) or "punch-through stopper" at the base of the fins

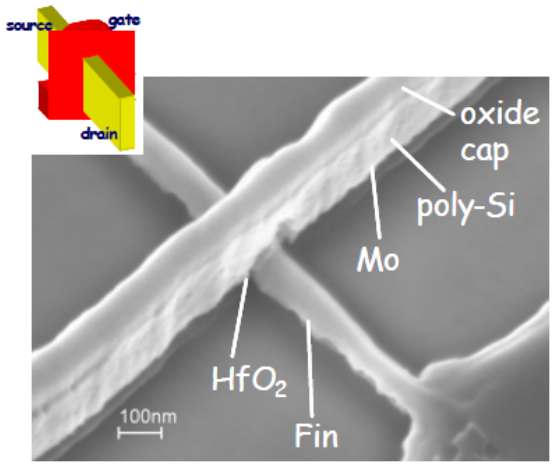
- 90 nm L_g FinFETs demonstrated
  - W_{fin} = 80 nm
  - H_{fin} = 100 nm

  DIBL = 25 mV

C.-H. Lee, VLSI-T(2004)

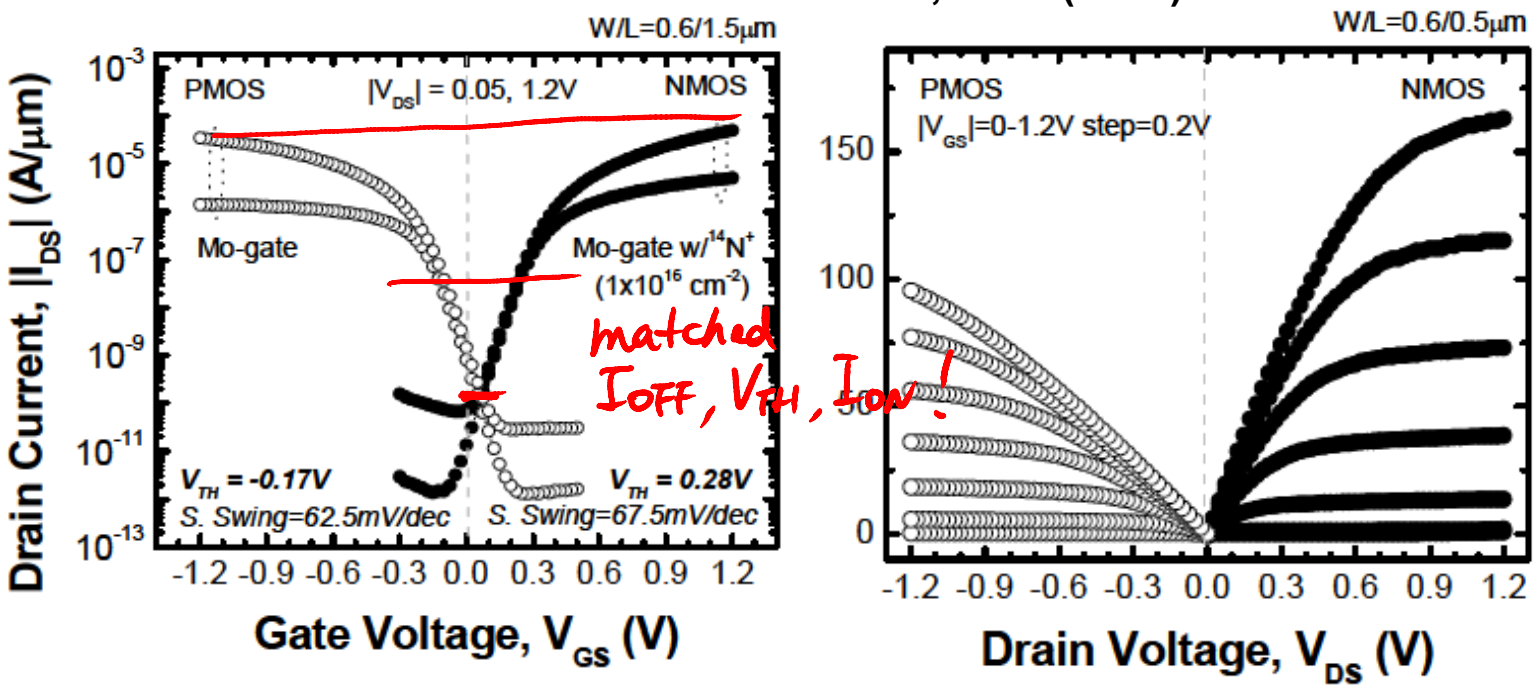
2004: High-κ FinFETs

(UC Berkeley)



- FinFET Threshold Voltage tuning is flexible by implementing N into Mo metal gate ← doped with N_2, to tune WF
- Highly matched N/P-FinFETs

D. Ha, IEDM(2004)



matched I_{OFF}, V_{TH}, I_{ON}!

On May 4, 2011, Intel Corporation announced what it called the most radical shift in semiconductor technology in 50 years.

A new 3-dimensional transistor design will enable the production of integrated-circuit chips that operate faster with less power…

for 22nm Node CMOS platform

THE WALL STREET JOURNAL. * * * * Thursday, May 5, 2011

CORPORATE NEWS

Intel Rethinks Chip's Building Blocks

By Don Clark

Intel Corp. showed off what it called the most radical shift in semiconductor technology in more than fifty years, a design that could produce more powerful chips for gadgets without taxing their batteries.

The company plans to change a key part of each chip into a vertical, fin-like structure, a similar principle to the way high-rise buildings pack more office space in a city. The parts being changed—transistors—are the building block of nearly all electronic products; today's microchips can contain billions of the tiny switching elements.

Intel said its latest technology could bring more computing power to smartphones and tablet computers as well as speed up corporate data centers—all while sharply reducing power consumption.

Though rivals also have been exploring similar technologies, Intel is the first to commit to using the so-called 3-D approach in high-volume production, a gamble that analysts said could help Intel match the performance advantages of rivals that have largely kept Intel's chips out of the smartphone market.

"We've been talking about these 3-D circuits for more than 10 years, but no one has had the confidence to move them into manufacturing," said Dan Hutcheson, a chip-manufacturing specialist with the firm VLSI Research.

Intel executives demonstrated working chips based on the new approach at a gathering Wednesday in San Francisco. They indicated the first microprocessors would likely be targeted for high-end desktop computers and server systems and arrive in early 2012.

For decades, chip manufacturers have raced to shrink the size of components, which increases the performance of chips while decreasing the cost of each computing function. Competition has spurred companies to introduce ever-smaller processes every couple of years.

Intel executives say the shift to 3-D transistors brings more benefits than simply moving to a new generation of manufacturing technology. For example, if designers keep performance consumption constant, the new technology consumes half the power as Intel's existing production method.

"That is an unprecedented gain," said Mark Bohr, who holds the title of Intel fellow and leads its development of new manufacturing processes. "We've never achieved that kind of performance gain at low voltage."

Chip designers have long worked in more than two dimensions, with transistors topped by layers of interconnecting wiring. Intel's shift relates to a part of each transistor that determines how fast electricity flows and how much current may leak out, affecting power consumption.

Intel engineers replaced a flat channel for conducting electrons with a fin-shaped structure surrounded on three sides by a device called a gate that turns the flow on and off. The three-dimensional shape, Mr. Bohr said, lets more current flow during the "on" state and less current to leak when the transistor is switched "off."

Intel disclosed the underlying approach in research papers in 2002, and has spent the intervening years perfecting it. It has opted to shift completely to the new transistors for its next manufacturing process—slated to create chips with circuit dimensions measured at 22 nanometers, or billionths of a meter. Intel's current chips use 32-nanometer technology.

Departures from conventional manufacturing technologies tend to increase costs, and chip companies try to avoid them. Mr. Bohr said Intel concluded it could move to the new technology with a 2% to 3% increase in the cost of a finished silicon wafer, each of which contains hundreds of chips.

Others are expected to use the approach at some point, too, but not until they have shrunk their circuitry beyond 22 nanometers.

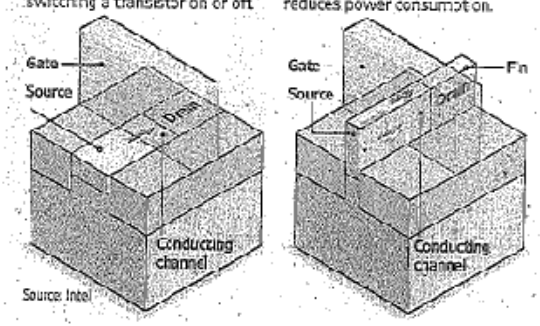
Globalfoundries, a production service spun off from Advanced Micro Devices Inc., said Wednesday it will use conventional transistors for its forthcoming 20-nanometer process. "We don't see the need" for technologies like 3-D transistors until subsequent production processes, a spokesman said.

Intel's Move Into 3-D

The chip maker breaks from conventional approaches to make transistors.

Conventional transistor: Electrons flow between components called a source and a drain, forming a two-dimensional conducting channel. A component called a gate starts and stops the flow, switching a transistor on or off.

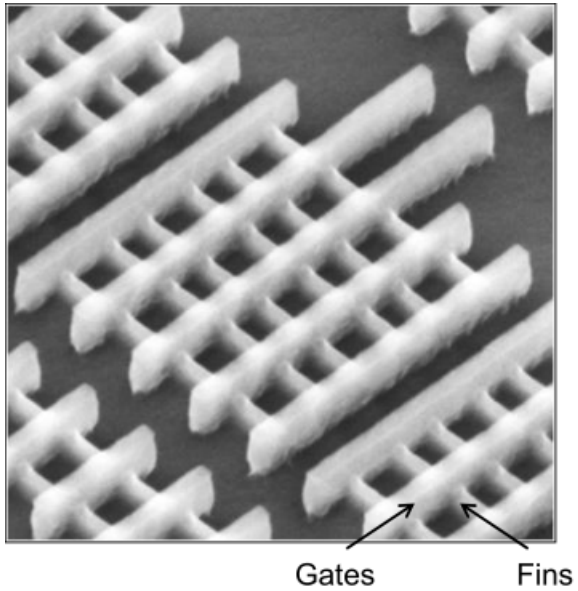
Intel's new transistor: A fin-like structure rises above the surface of the transistor with the gate wrapped around it, forming conducting channels on three sides. The design takes less space on a chip, and improves speed and reduces power consumption.

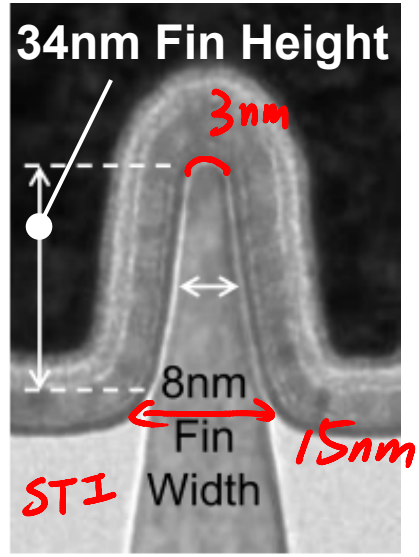


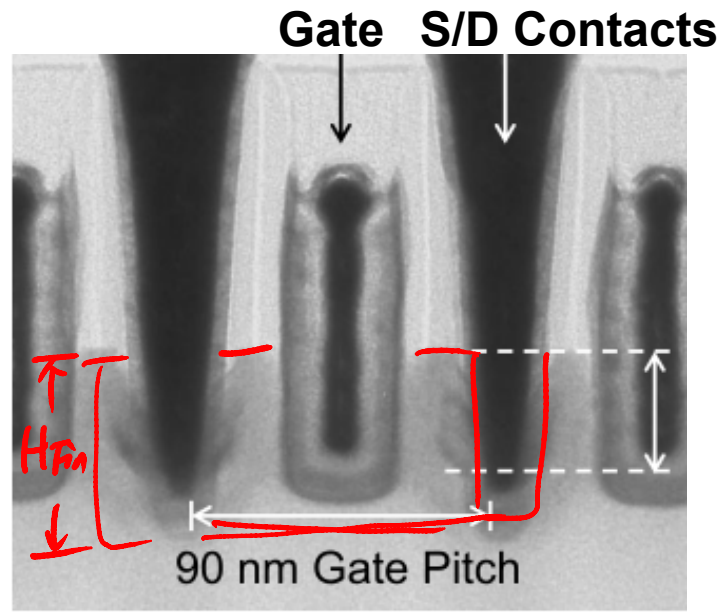
Source: Intel

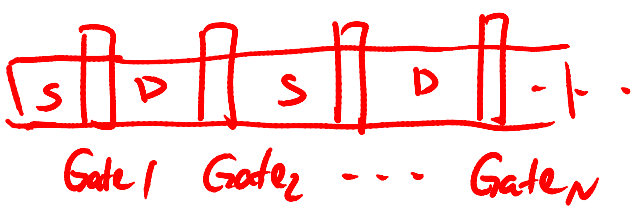
2012: 1st Tri-Gate FETs in Production

(Intel)









"Nested" FinFETs

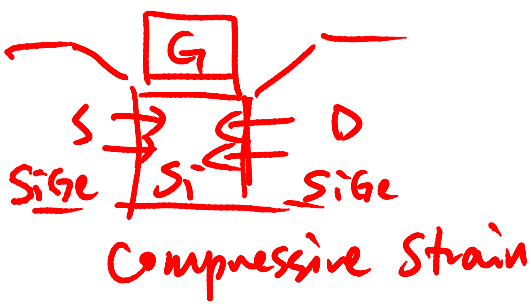
tapered fin (due to bulk process)

High-k/Metal-gate last flow

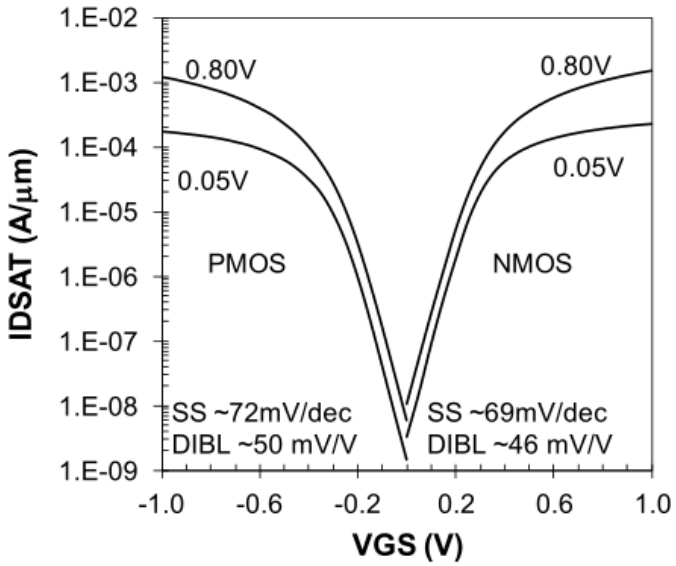
C. Auth, VLSI-T (2012)
M. Bohr, Intel Design Forum (2012)

Intel's Tri-Gate FETs Performance

TEM of PMOS epi-SiGe Source/Drain

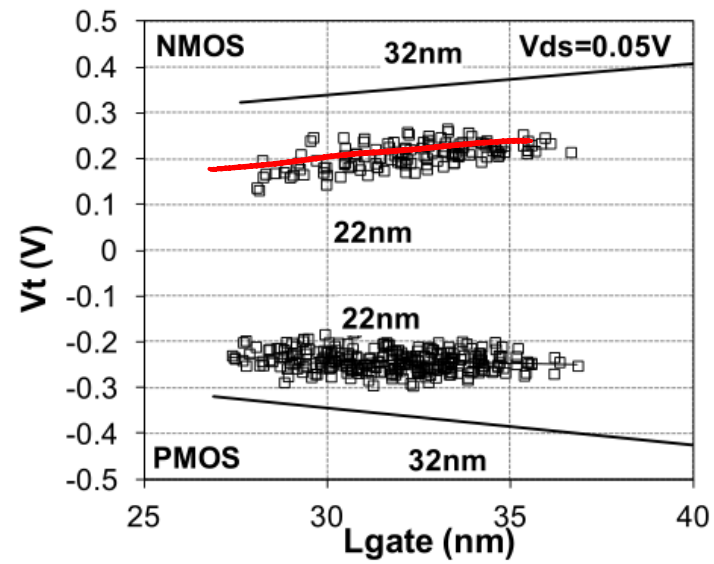


I_{ds} *vs.* V_{gs}



Strained p-MOS
matched I_{ON} between
N and P

V_T *vs.* L_{gate}



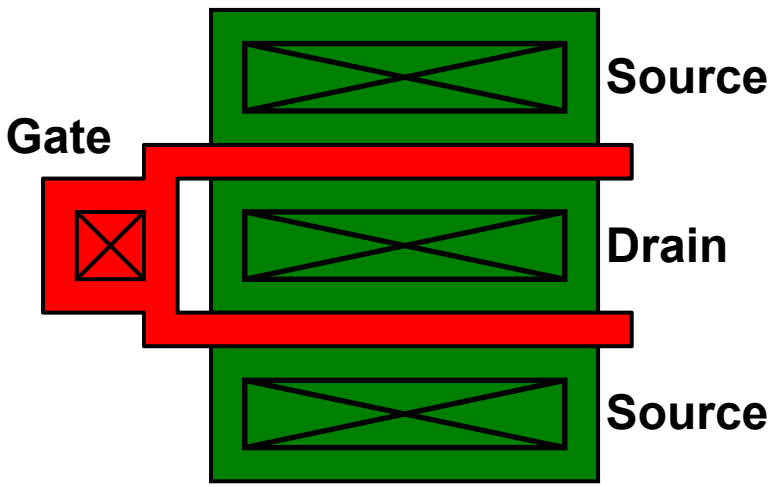
Small V_{TH} roll-off

C. Auth, VLSI-T (2012)
M. Bohr, Intel Design Forum (2012)

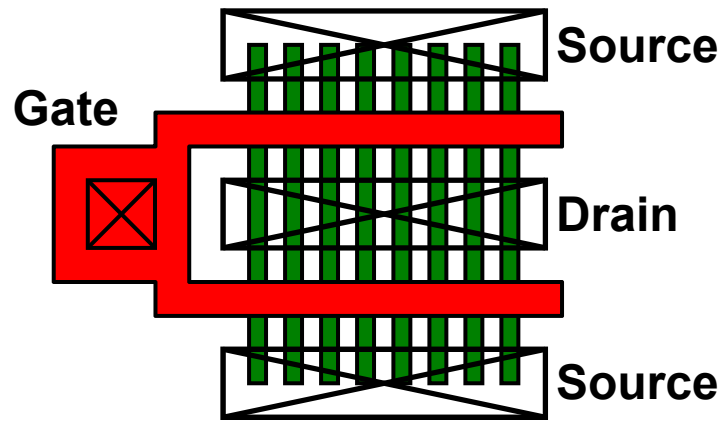
FinFET Layout

- **Layout is similar to that of conventional planar MOSFET,** except that the channel width is quantized:

$$W_{eff} = (2 * H_{fin}) * N_{Fins} * N_{Gate\text{-}fingers}$$

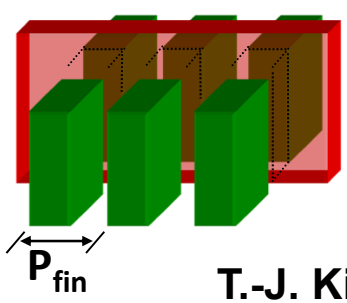


Bulk-Si MOSFET



FinFET

- **Fin pitch (P_{fin}) is a new key parameter to be optimized for performance and layout efficiency.**



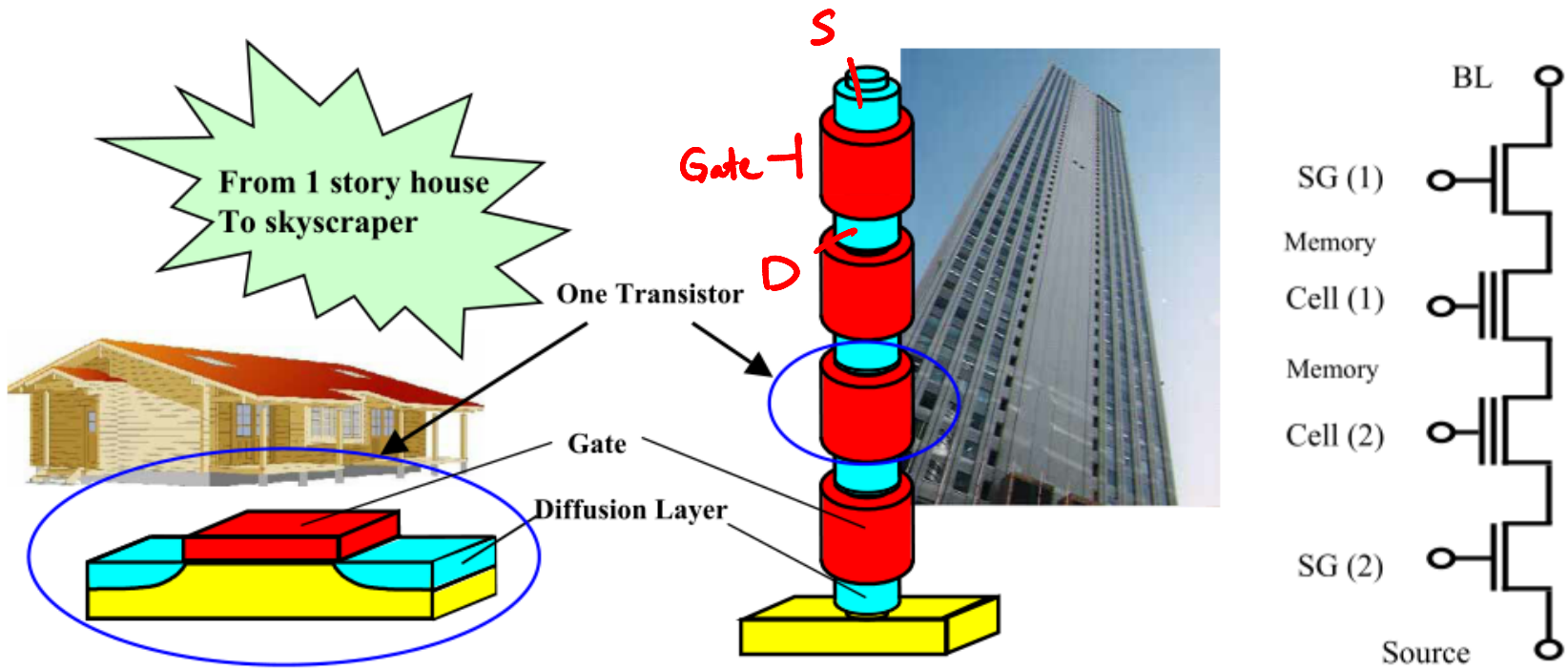
Effective width: $2H_{Fin} + W_{Fin}$

to achieve better layout efficiency:

$2H_{Fin} \geq P_{Fin}$

T.-J. King Liu, ISSCC Forum on Mixed-Signal/RF (2013)

Vertical Stacked MOSFETs – Implication for High Density Memory



Currently used Planar type Transistor

Proposed novel Stacked Vertical Transistor

→ Vertical Gate-all-around MOSFET

→ promising for High Density Memories
(Low cost, low performance compared to Logic)

T. Endoh (Tohoku Univ.), (2007)

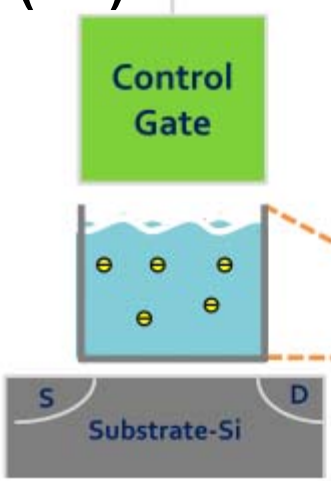
2013: 1st 3-Dimensional NAND

(Samsung)

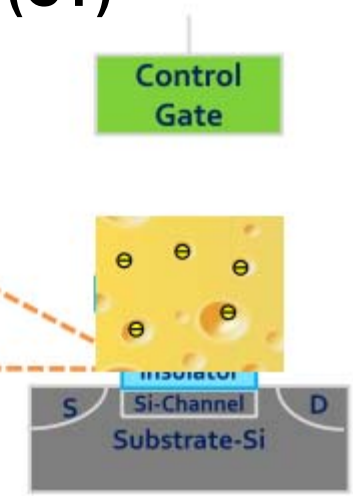
Structure Innovation

Material Innovation (2004)

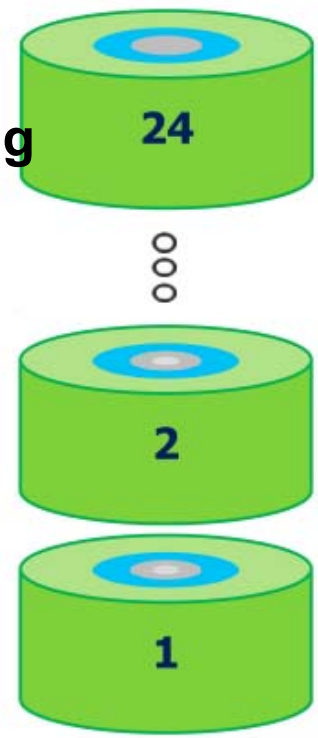
Floating Gate (FG)



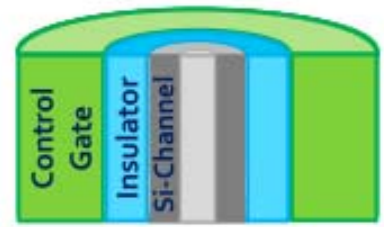
Charge Trapping (CT)



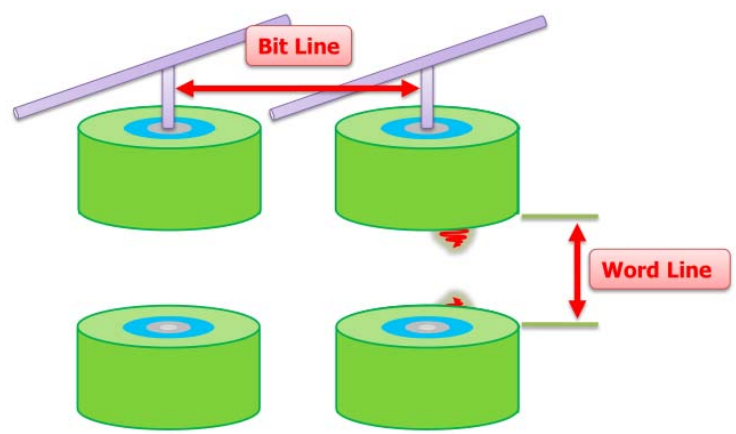
3D CT



Device Structure



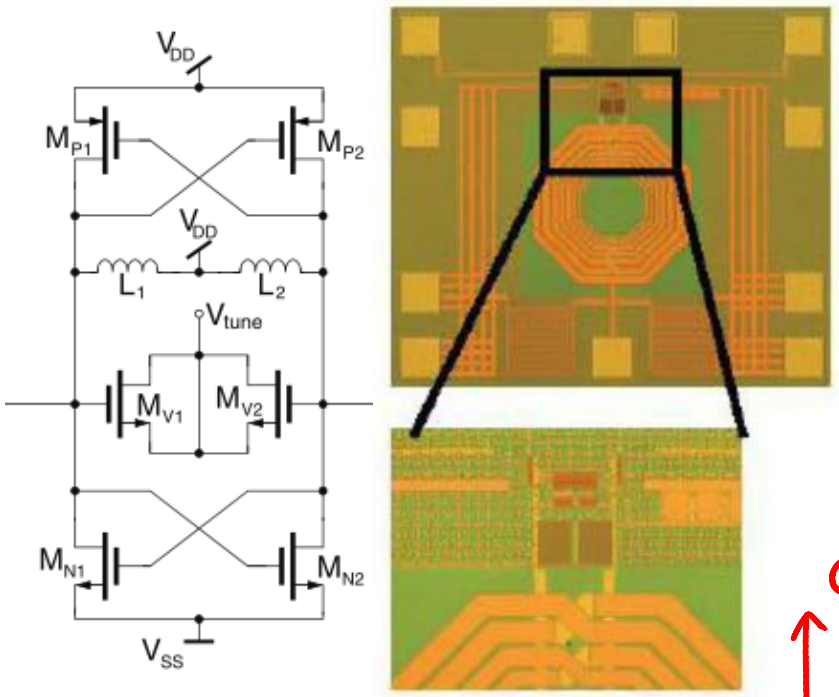
Memory Architecture



J. Elliott & E.S. Jung, Flash Memory Summit (2013)

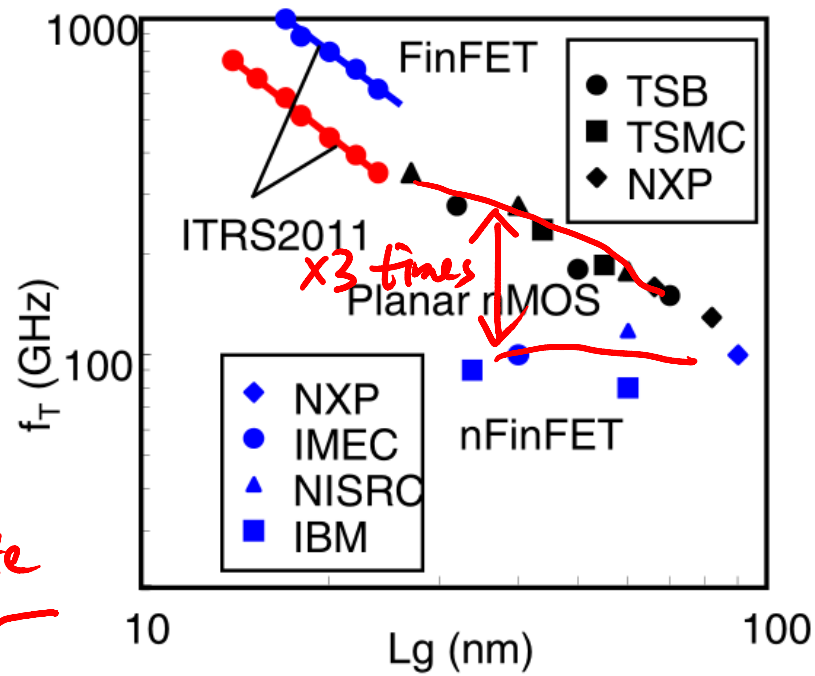
FinFETs in Analog/RF World

FinFET-based VCO

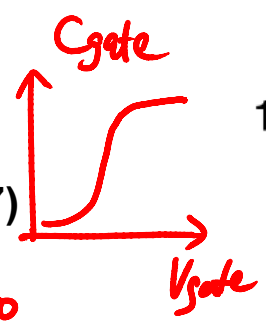


G. Knoblinger, *Int. SOI Conf.* (2007)

Cutoff Frequency (f_T): Bulk *vs.* FinFET



T. Ohguro, VLSI-T(2012)



Uses MOSFET as a varactor to tune $\omega = \frac{1}{\sqrt{LC}}$

$f_T \doteq \frac{G_m}{2\pi(C_{gs}+C_{gd})}$

parasite $R_{s/d}$, C could hurt

Summary

- **The FinFET was originally developed for manufacture of self-aligned double-gate MOSFETs**, to address the need for improved gate control to suppress I_{OFF}, DIBL and process-induced variability for L_g < 25nm.
  - Different variations of the FinFET have been developed to improve performance, manufacturability and cost.
  - **It has taken ~10 years to bring "3-D" transistors into volume** production.

- **Multi-gate** MOSFETs provide a pathway to achieving **lower power and/or improved performance.**
  - Further evolution of the MOSFET to a 3-D stacked-channel structure may occur by the end of the roadmap.
  - Issues needed to address for implementing FinFET into a System-on-Chip (SoC).

Course Modules

1. Device Physics (~5 lectures)

- History and course overview
- Short-channel MOSFET Issues, performance metrics,
- Thin-body transistors design, scale length,
- MOSFET Compact Modeling, Technology CAD

2. Device-Process Interactions (~9 Lectures)

- Advanced MOSFET process flow overview,
- FinFET substrate impacts,
- Advanced gate stack process,
- Source/Drain doping, Threshold Voltage tuning for FinFETs
- Quantum Mechanical effects,
- Carrier mobilities, Strained-Si technology, high mobility channel materials (guest lecture)

Course Modules (Cont'd)

3. Device-Circuit Interactions (~9 lectures)

- Performance variability: systematic and random
- Industry's state-of-the-art FinFET platforms
- FinFET-based SRAM design
- FinFET-based analog and RF device/circuit
- 3-D integrations for advanced CMOS technologies
- FinFET reliability issues: Bias-Temperature Instability, noise, ESD and self-heating,…

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Retrograde Well Doping

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