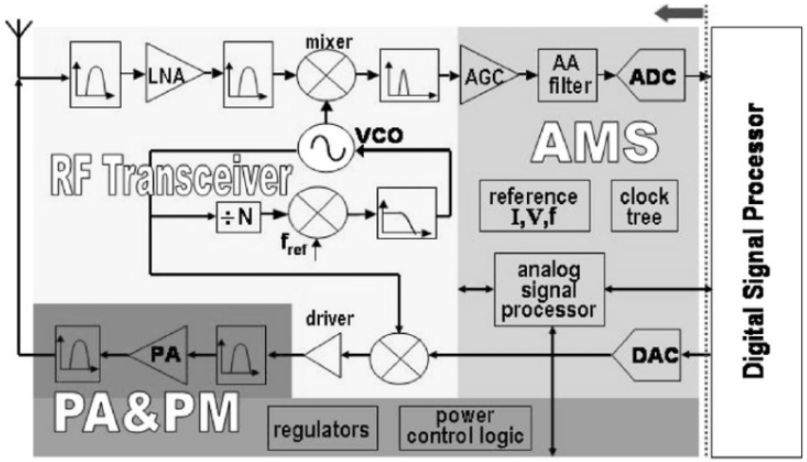
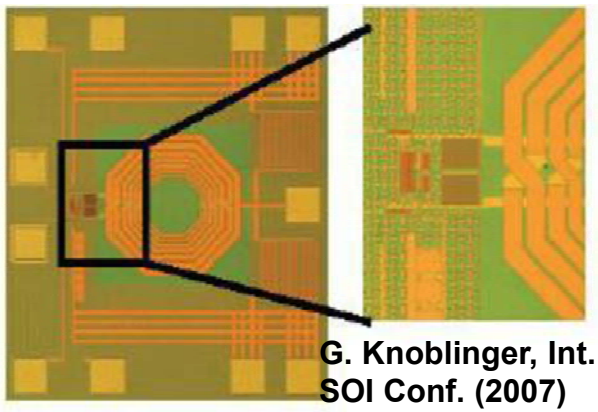
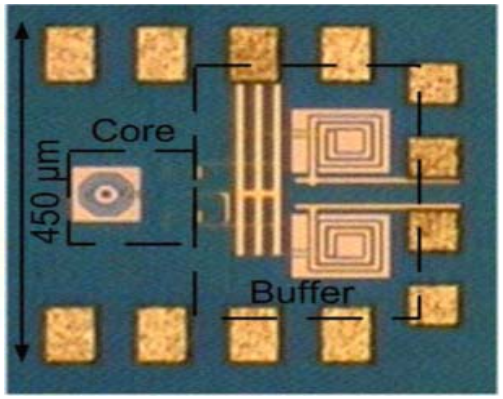


FinFET-based VCOs



G. Knoblinger, Int. SOI Conf. (2007)



D. Siprak, ESSCIRC (2009)

Lecture 16

- **Advanced Technologies on Analog/RF Circuits**
  - Analog/RF MOSFET Metrics and Challenges
  - Thin-Body MOSFETs for Analog/RF Applications

Reading:

- M. Fulde, "Variation Aware Analog and Mixed-Signal Circuit Design in Emerging Multi-Gate CMOS Technologies," *Springer,* 2010.
- multiple research articles (reference list at the end of this lecture)

RF Technology: Not Dictated by Si CMOS!

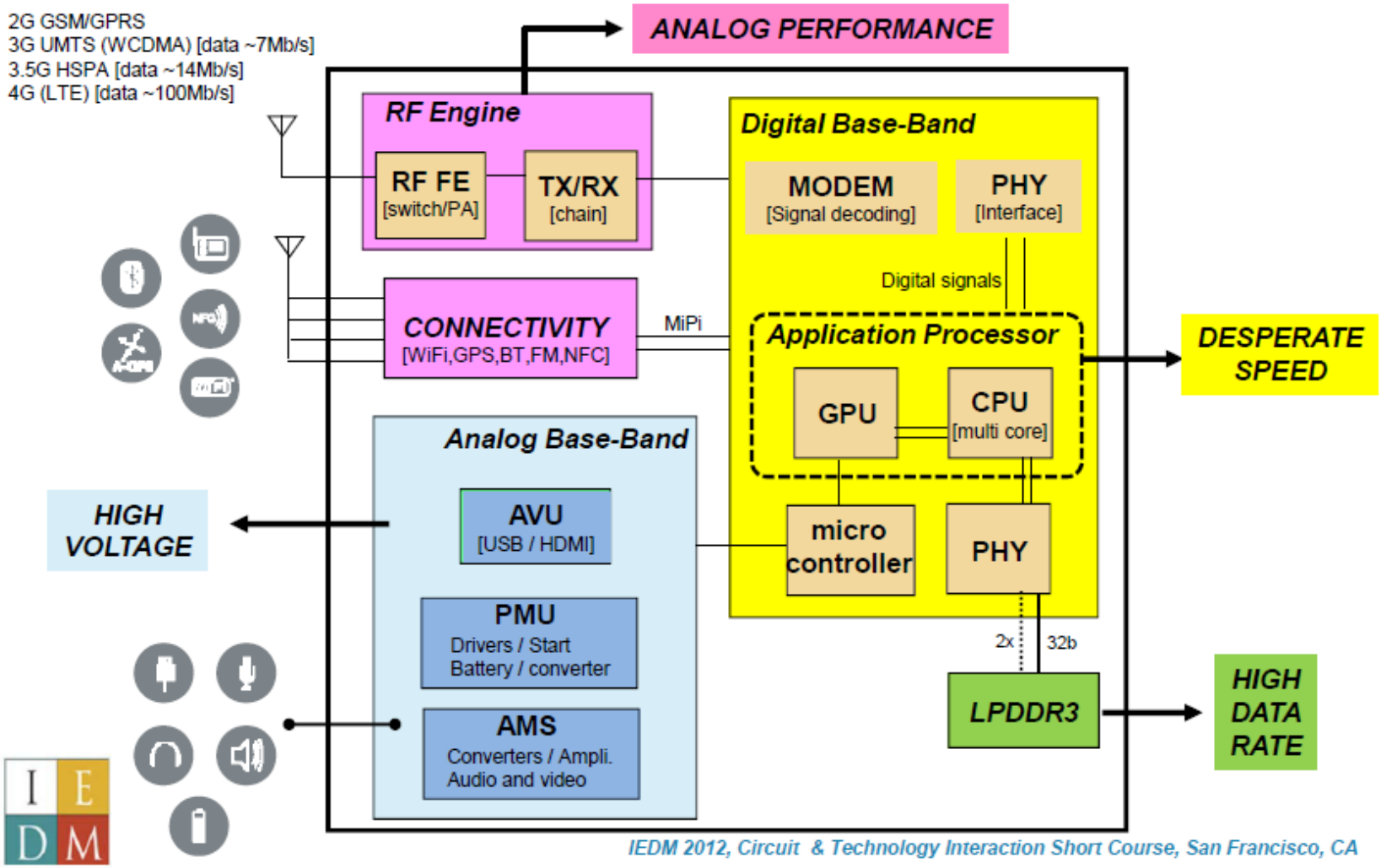
Source: ITRS (2011)

Frequency Range:	Applications:	Technology:
LF Analog (-0.4 GHz)	Automotive controls, power management	RF CMOS
RF (-30 GHz)	Cellular (2G-GSM, 3G-CDMA, 4G-LTE) WLAN(Bluetooth, GPS), Serdes, high performance ADC/DAC	RF CMOS / SiGe Bipolar
Millimeter Wave (-300 GHz)	60 GHZ point-to-point, radar, wireless backhaul	SiGe Bipolar
THz	No product yet	

- For extremely high-frequency and high-power (*e.g.* PA) applications, SiGe BJT has performance advantage over RF MOSFETs, due to its
  - Larger transconductance (G_m) as well as G_m/I_d
  - Higher power density

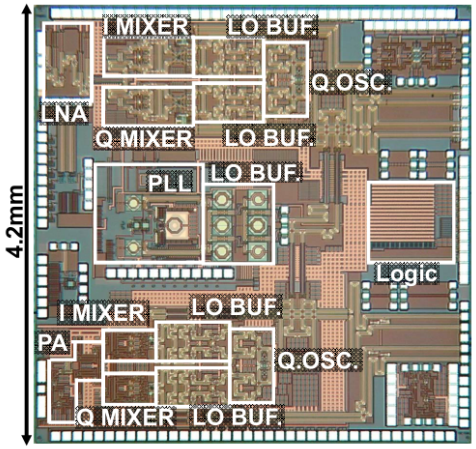
Mobile System Structure

F. Arnaud, IEDM SC (2012)

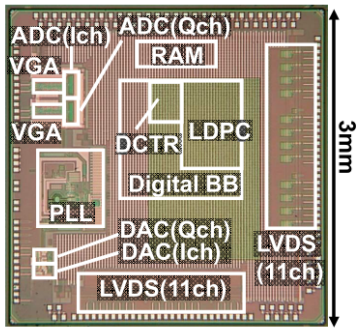


System on Chip (SoC)

65nm CMOS (RF)

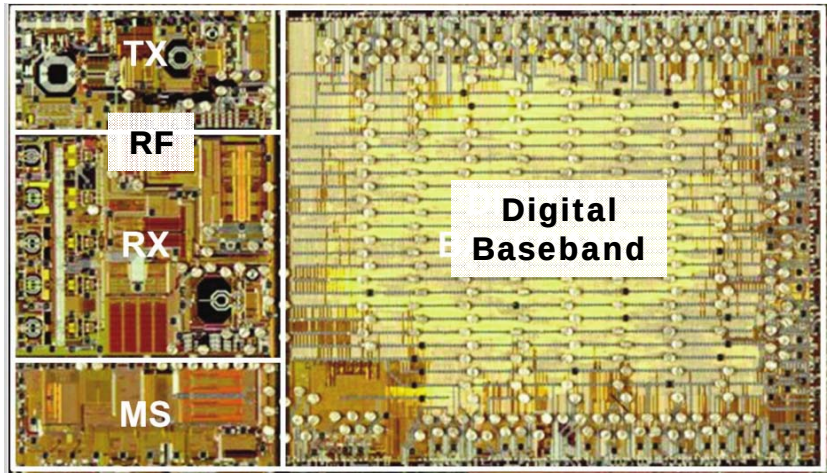


40nm CMOS (BB)



A. Matsuzawa, IEDM (2012)

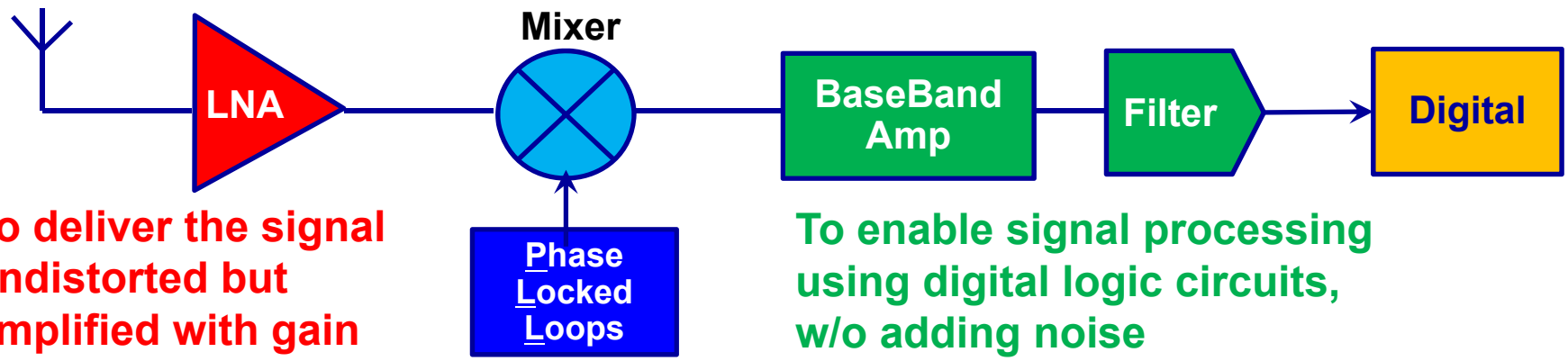
65nm SoC (Qualcomm)



A. Cicalini, ISSCC (2011)

- SoC: system integration onto a single IC die
  → higher performance, lower cost
- Preferred to be implemented by LSTP technology, due to:
  - ✓ Low power (good for battery-supported mobile devices)
  - ✓ Low noise
  - ✓ High V_{DD} (easier design for RF/Analog circuits)
  - × Limited performance (digital clk frequency, f_T & f_{MAX})

RF RX Front-End Requirement



To deliver the signal undistorted but amplified with gain

$$FOM_{LNA} = \frac{A_{V0} \cdot I_{IP3}}{(NF-1) \cdot P} \propto \frac{f_{MAX} G_m R_{out}}{NF_{min} V_{DD}}$$

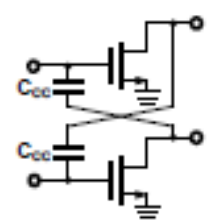
To synchronize communications

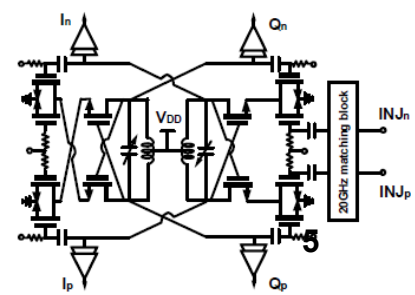
$$FOM_{PLL} = \frac{f^2}{\Delta f^2} \frac{1}{S(f) \cdot P} \propto \frac{Q_{LCR}}{V_{DD}}$$

To enable signal processing using digital logic circuits, w/o adding noise

→ ***preferred low noise, high gain and linearity***

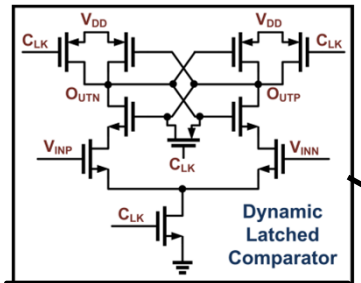
- **Continued CMOS technology scaling worsens SCE, variability, parasitic components, and noise**
  - → **Negatively impacts critical RF performance parameters**
- **Circuit techniques are used to mitigate these effects**
  e.g. negative capacitance, injection locking…

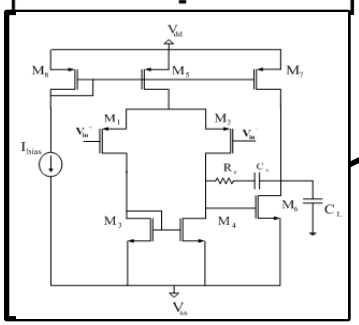




Analog-to-Digital Converter (ADC) Requirement

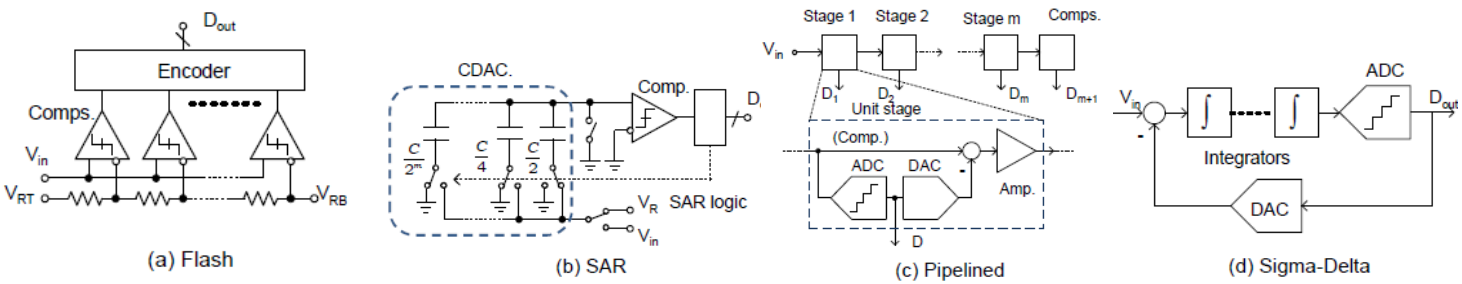
Comparator-based:
small mismatch





ADC Type	Resolution	Speed	Power Consumption
Flash	low	ultra-high	high
SAR	low	moderate	ultra-low
Pipeline	moderate	high	low
Σ-Δ	high	low	high

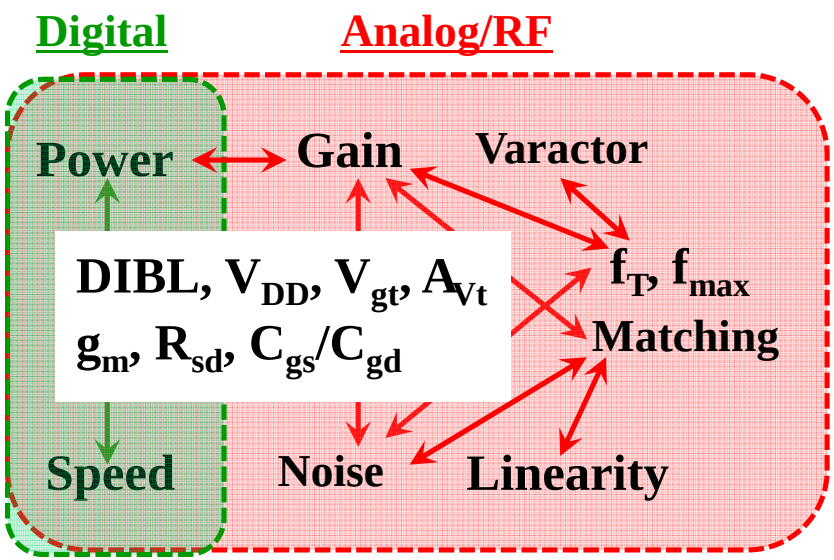
OPA-based:
small mismatch
high gain (>40dB)



- CMOS scaling → larger DIBL → lower gain
- V_{DD} reduction → smaller V_{GT} → larger mismatch

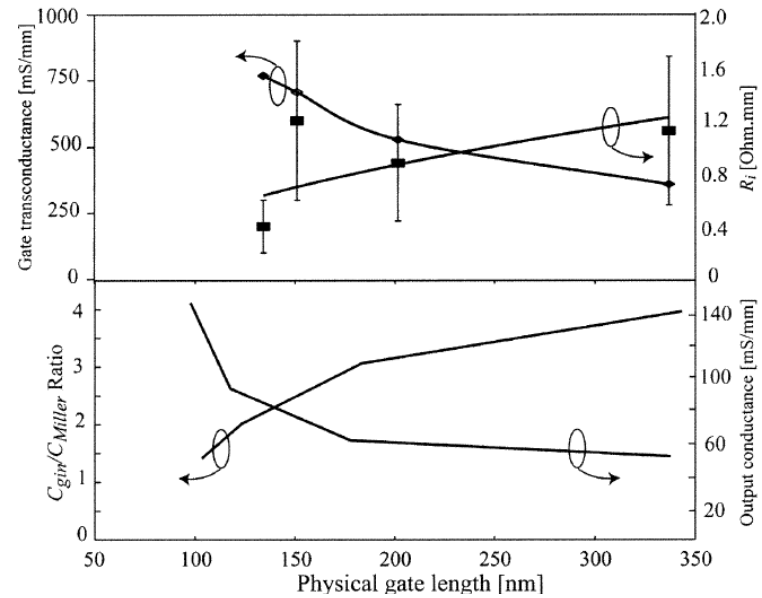
→ **High-resolution ADCs are extremely challenging!**

Analog/RF Technology Metrics and Challenges



A. Matsuzawa, IEDM (2012)

Performance Degradation in Bulk MOSFETs



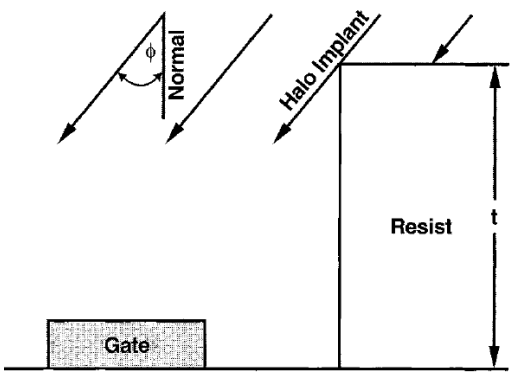
G. Dambrine, EDL (2003)

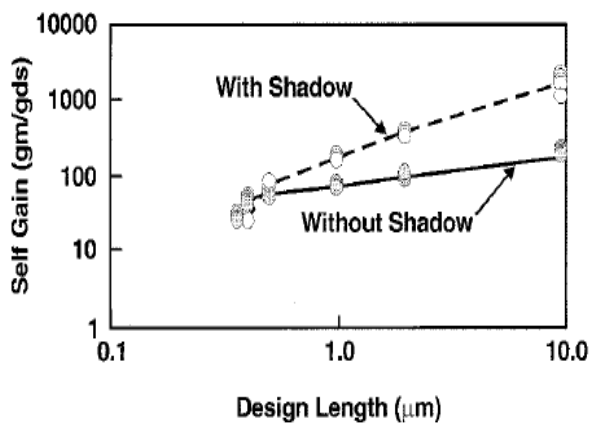
- More complicated, cross-related metrics than digital technology
- Traditionally, CMOS technology scaling is driven by digital logic
  - → not fully optimized for RF/analog
  - → More performance degradation is expected as scaling the gate length and V_{DD}

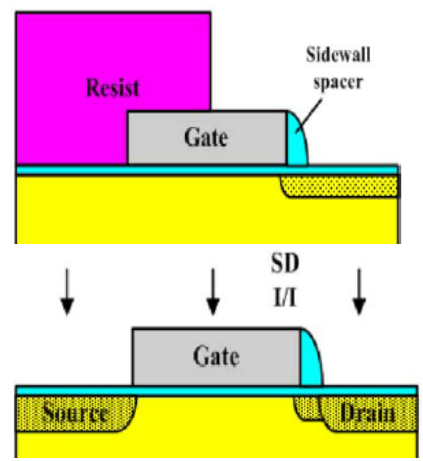
Analog/RF "Flavored" MOSFETs

- Only a trick to maintain some analog/RF performances

Asymmetric S/D MOSFETs







T. Hook, TED (2002)

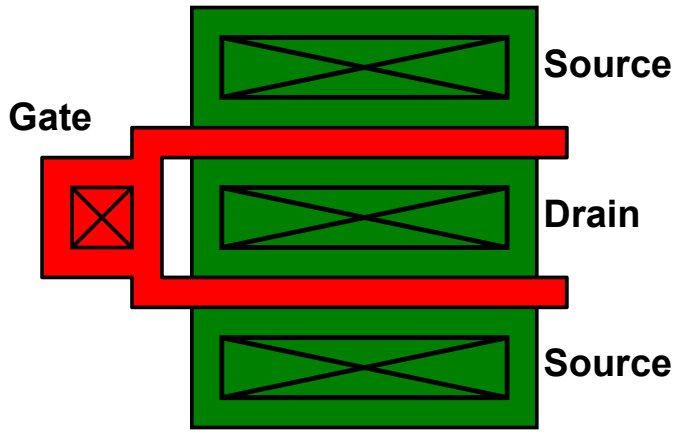
J.P. Kim, TED (2007)

- **Asymmetric S/D MOSFET can be co-fabricated with conventional digital MOSFET except for that its drain is more lightly doped than its source, for**
  - → **Improved electrostatics (↑ R_{out} & A_{v0})**
  - → **Improved mobility (↑ G_m)**
  - → **Reduced Miller capacitance C_{GD} (↑ f_T)**

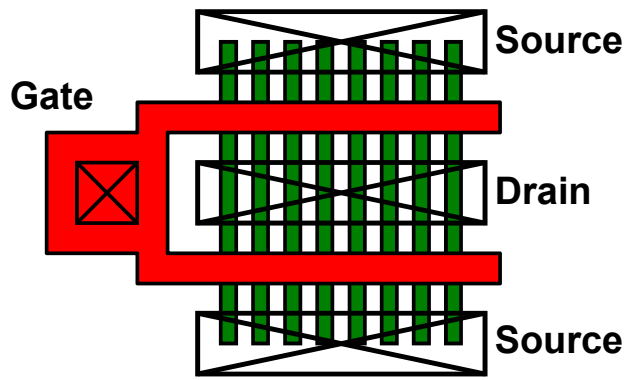
FinFET in Analog/RF Design

- **Layout is similar to that of conventional MOSFET,** except that the channel width is quantized:

$W_{eff} = (2 * H_{fin}) * N_{Fins} * N_{Gate\text{-}fingers}$

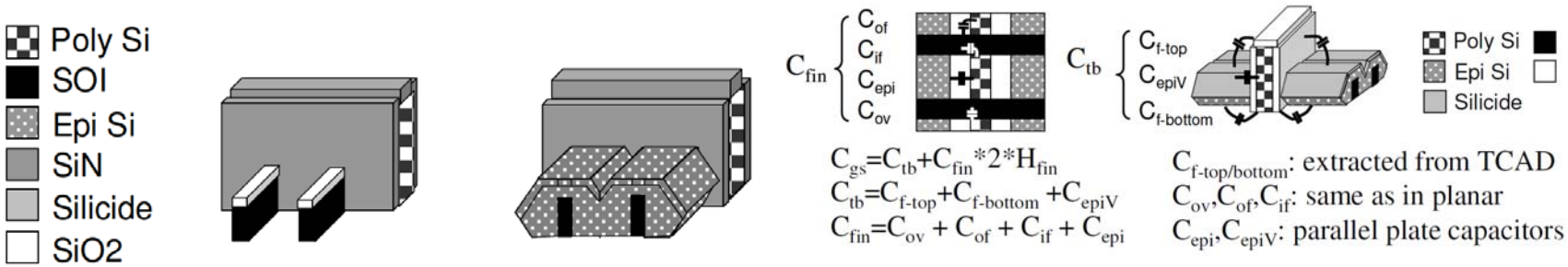


Bulk-Si MOSFET



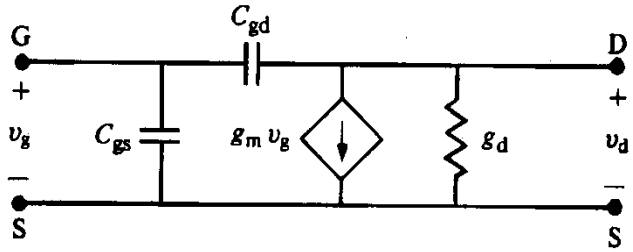
FinFET

- **FinFET Source/Drain can be merged with SEG.**

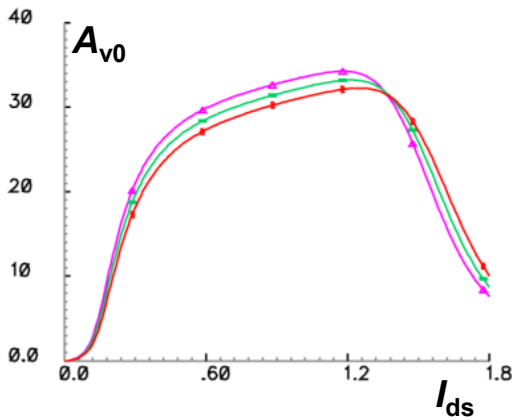


M. Guillorn, VLSI-T (2008)

Intrinsic Gain (A_{V0})



MOSFET's A_{V0} vs. I_D



$$A_{V0} = \frac{G_m}{G_{ds}}$$

define

$$\frac{G_m}{I_{ds}} = \frac{2}{V_{gs} - V_{TH}}$$

above threshold

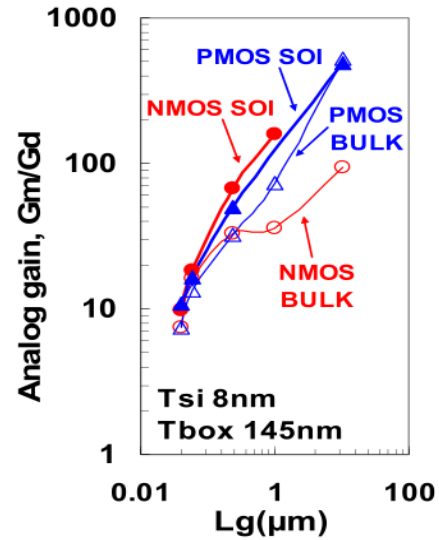
$$\frac{G_m}{I_{ds}} = \frac{1}{m\,kT/q}$$

below threshold

so that

$$A_{V0} = \frac{G_m}{I_{ds}} \cdot V_{EA}$$

FD-SOI *vs.* Bulk

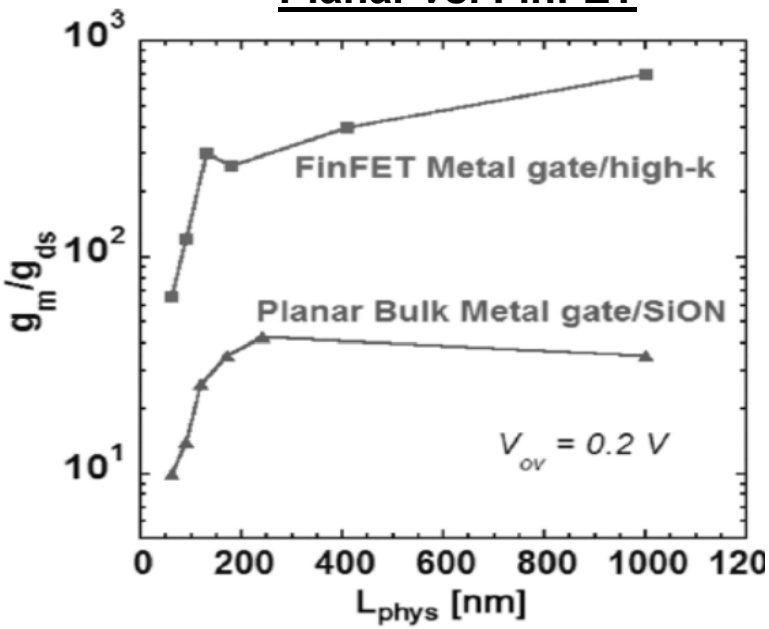


C. Fenouillet, IEDM (2009)

- **MOSFET intrinsic gain degrades as decreasing gate length, mainly resulted from the worsening electrostatics (DIBL, SCE).**
- **Thin-body MOSFETs can achieve significantly higher gain than planar-bulk MOSFETs, due to their superior electrostatic integrity and higher carrier mobilities.**

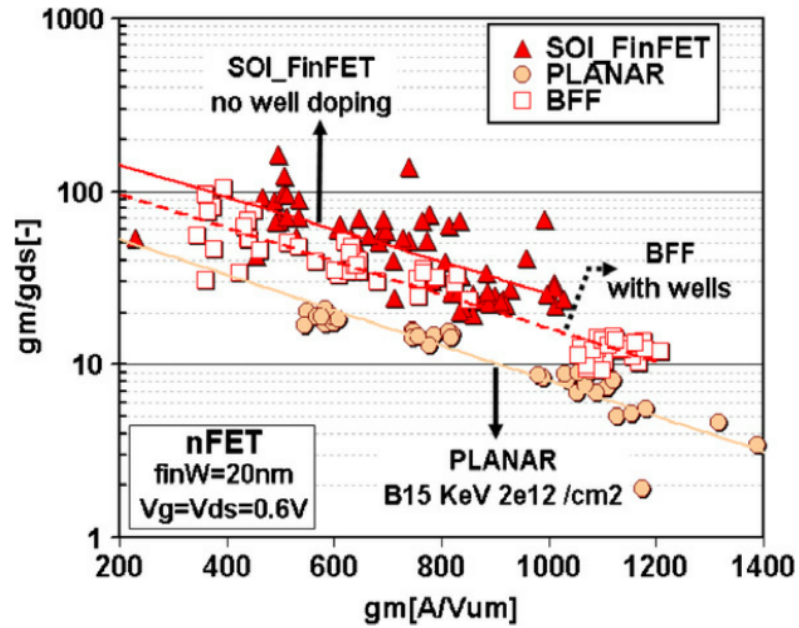
FinFET Intrinsic Gain

Planar *vs*. FinFET



P. Wambacq, TCS (2007)

SOI FinFET *vs*. Bulk FinFET



T. Chiarella, SSE (2010)

- FinFET shows over 20 dB gain increase over planar MOSFETs.
- SOI FinFET (with no well doping) outperforms bulk FinFET (with retrograde well doping).

f_T and f_{MAX}

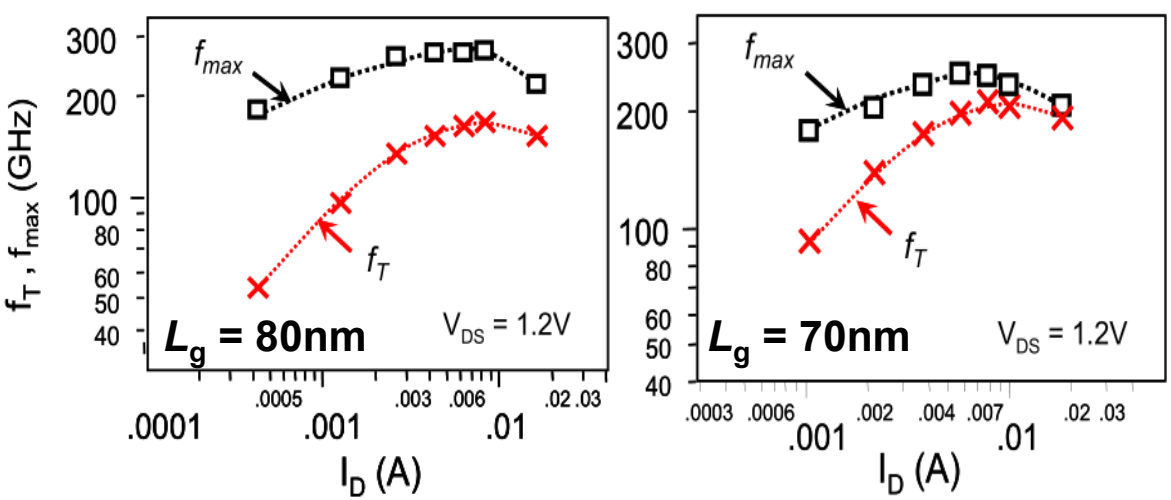
Cut-off Frequency:
(defined as the *f* when short-circuit current gain is unity)

$$f_t \approx \frac{g_m}{2\pi C_{gin}\sqrt{1+2\frac{C_{Miller}}{C_{gin}}}} = \frac{f_c}{\sqrt{1+2\frac{C_{Miller}}{C_{gin}}}}$$

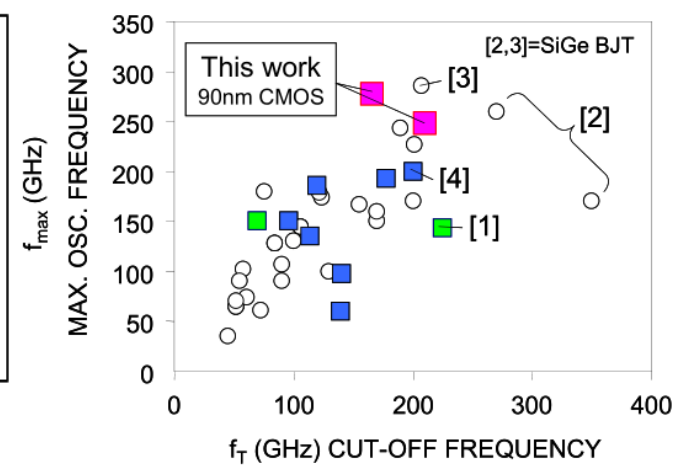
Maximum Oscillation Frequency:
(defined as the *f* when device power gain is unity)

$$f_{\max} \approx \frac{g_m}{2\pi C_{gin}} \frac{1}{2\sqrt{(R_g+R_s+R_i)\left(g_d+g_m\frac{C_{Miller}}{C_{gin}}\right)}}$$

90nm Si CMOS Technology



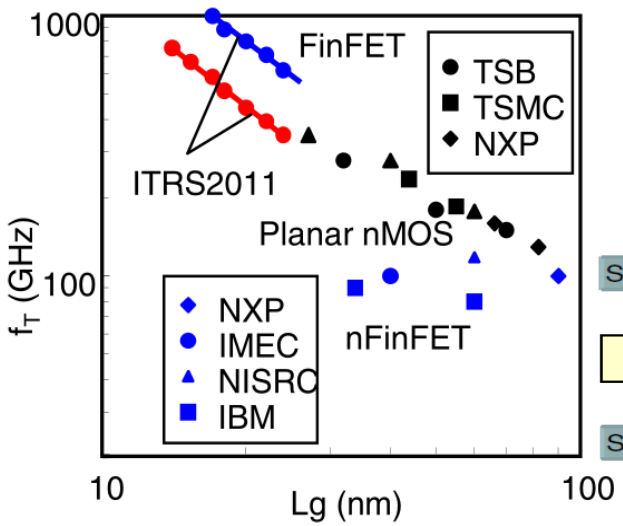
SiGe BJT *vs.* Si MOS



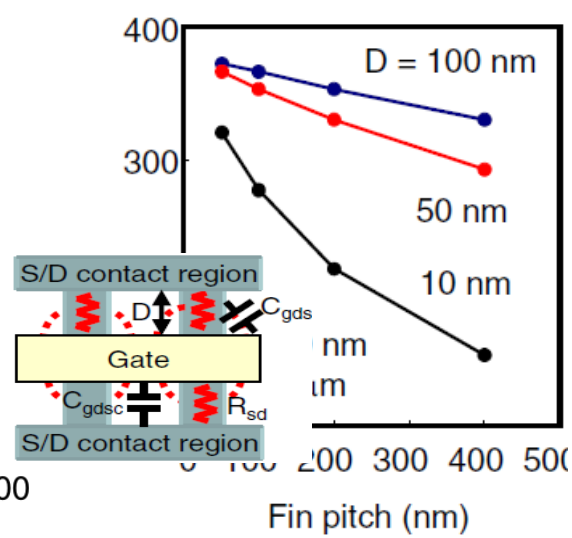
K. Kuhn, VLSI-T (2004)

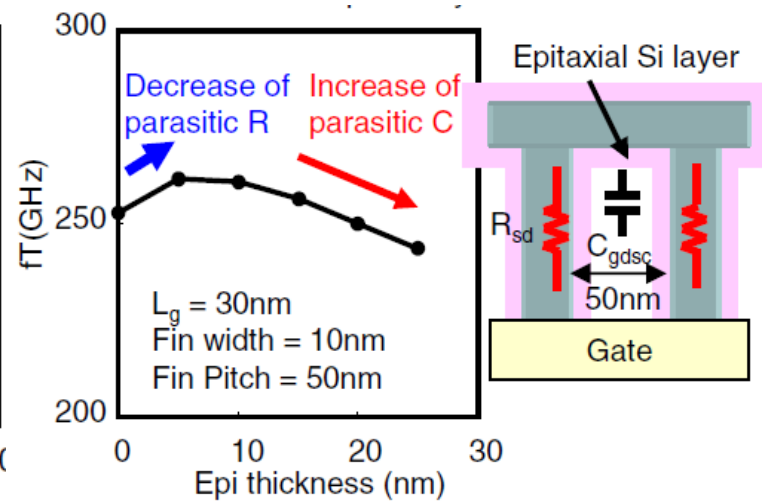
FinFET f_T and f_{MAX}

FinFET *vs.* Planar FET



Impact of Fin pitch & S/D Epi Thickness



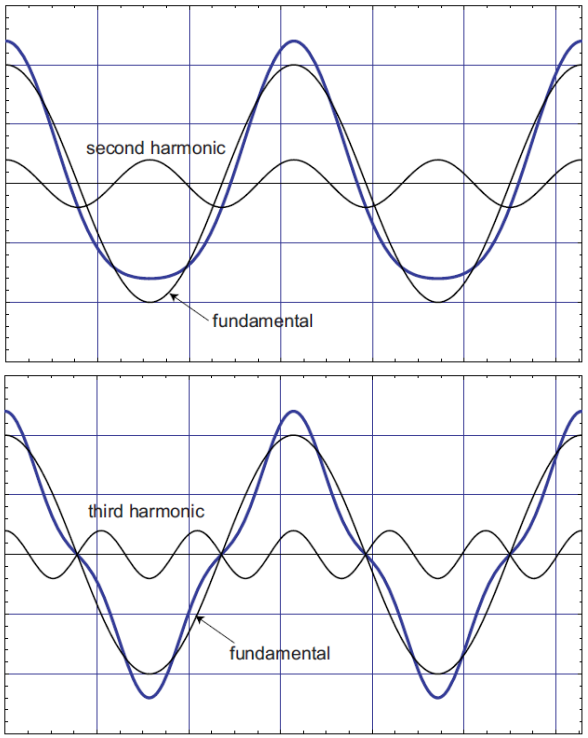


T. Ohguro, VLSI-T (2012)

- **FinFET has lower f_T than planar bulk MOSFET ☹**
- **Fin pitch, aspect-ratio and epi-S/D engineering can help to reduce the parasitic capacitance to be smaller.**

Linearity

Output Waveform Distortions



define

$$\mathrm{VIP}_2 = 4\frac{g_m}{g_{m2}}$$

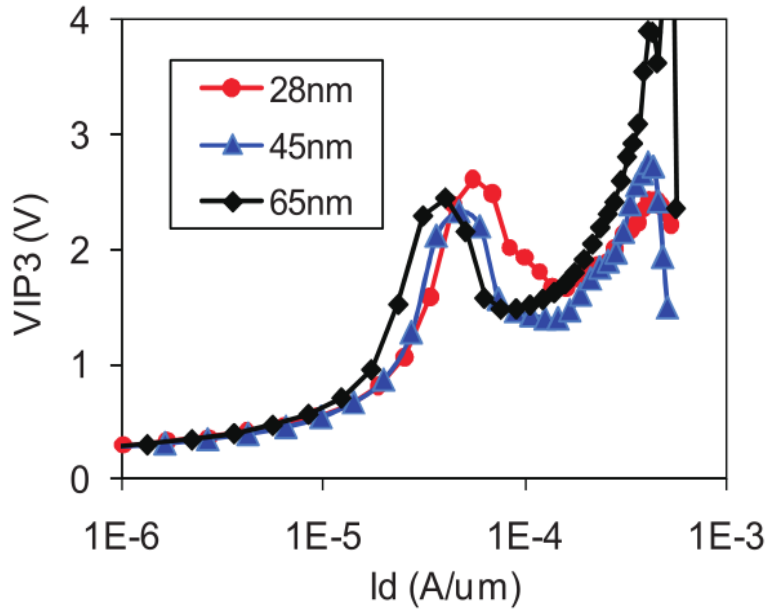
$$\mathrm{VIP}_3 = \sqrt{24\frac{g_m}{g_{m3}}}$$

where

$$g_{m2} = \frac{\partial^2 I_D}{\partial V_{gs}^2}$$

$$g_{m3} = \frac{\partial^3 I_D}{\partial V_{gs}^3}.$$

Planar LSTP Technology

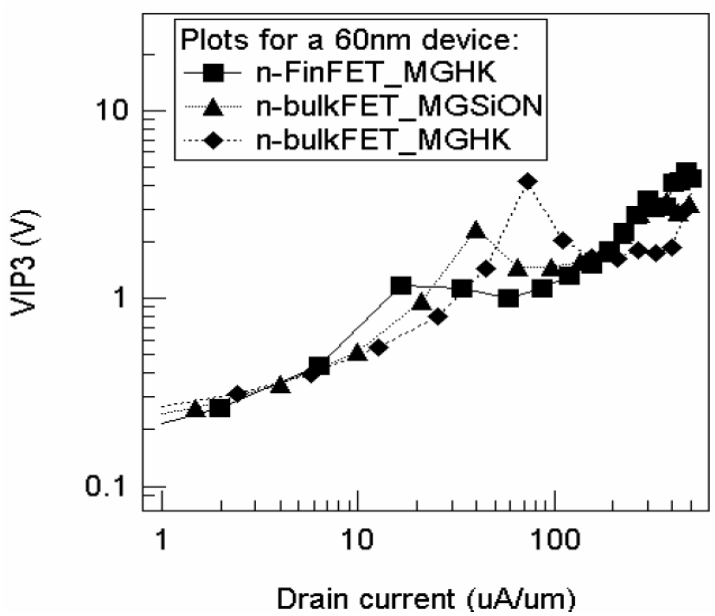


M.-T. Yang, VLSI-T (2011)

- The nonlinear products caused by n^{th} order distortion appearing at n times the frequency of the input (base) tone.
- Related to MOSFET G_m degradation slope.

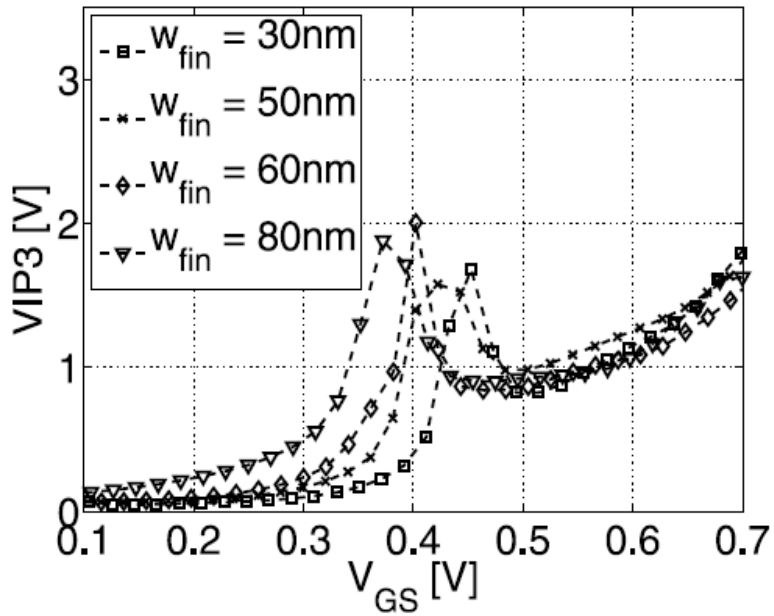
FinFET Linearity

Planar Bulk *vs*. FinFET



V. Subramanian, IEDM (2005)

V_{IP3} dependence on Fin Width

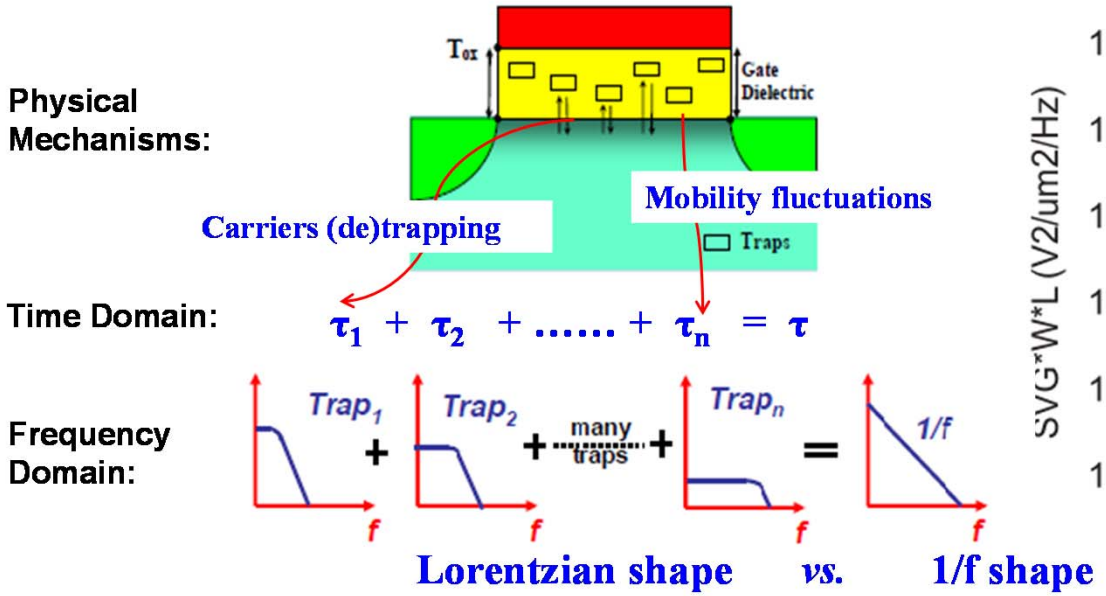


M. Fulde, *Springer Series in Adv. Microelec.* (2010)

- **FinFET has comparable V_{IP3} as planar bulk MOSFET.**
- **Sensitivity of V_{IP3} to device parameter variations can be reduced by using multiple fin widths (self-cascode) to achieve a broader maximum.**

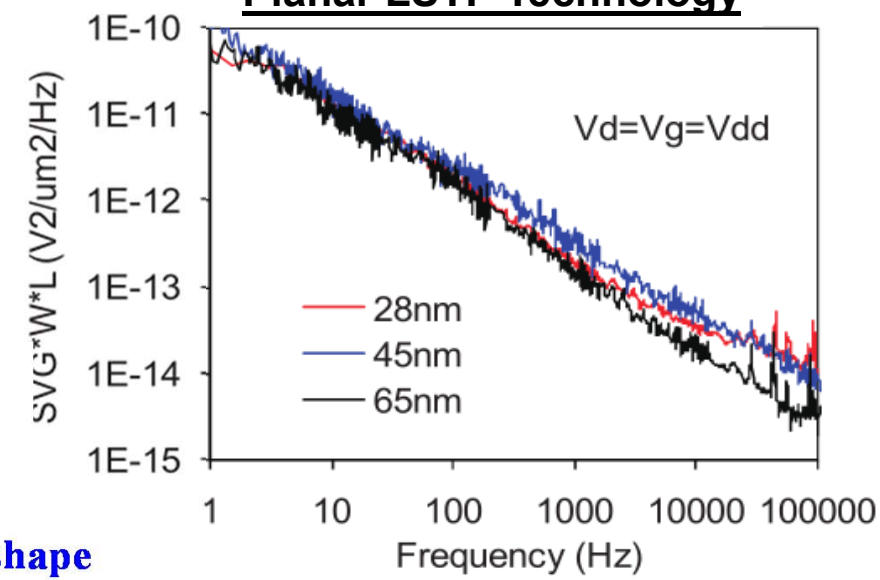
Low-Frequency Noise (LFN)

Physical Mechanisms



T. Morshed, IEDM (2009)

Planar LSTP Technology

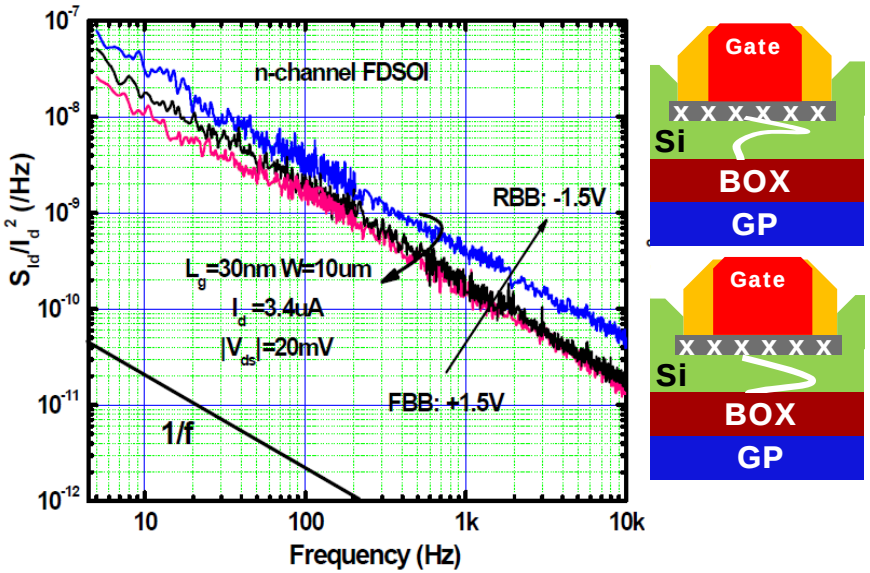


M.-T. Yang, VLSI-T (2011)

- **Origins: carrier concentration and mobility fluctuations induced by traps**
- **Impacts: causing instability issues in quasi-static circuits (*e.g.* SRAM) and correlating to high-frequency noise.**

Thin-Body MOSFET's LFN

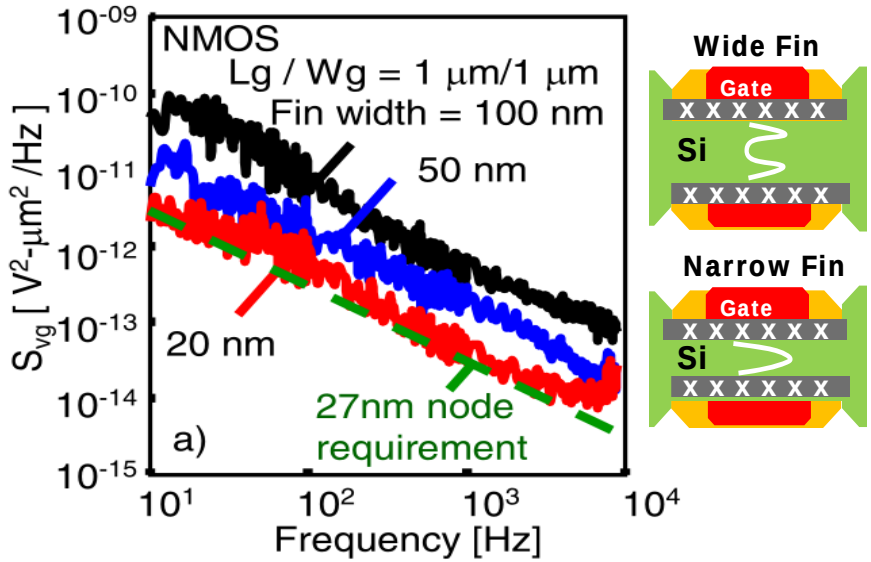
UTBB FDSOI LFN *vs.* BB



N. Xu, VLSI-T (2012)

- With FBB, the inversion layer channel moves away from the top high-κ interface and $E_\perp$ is reduced, resulting better LFN.

FinFET LFN *vs.* W_{Fin}

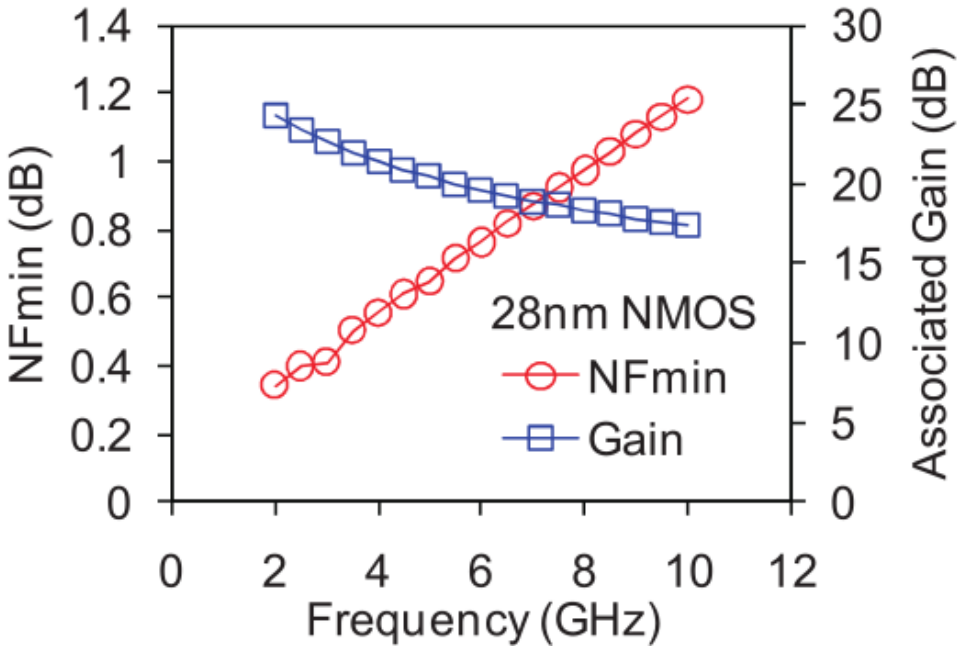


T. Ohguro, VLSI-T (2012)

- FinFET has lower LFN compared to the planar bulk MOSFET, due to the reduced $E_\perp$

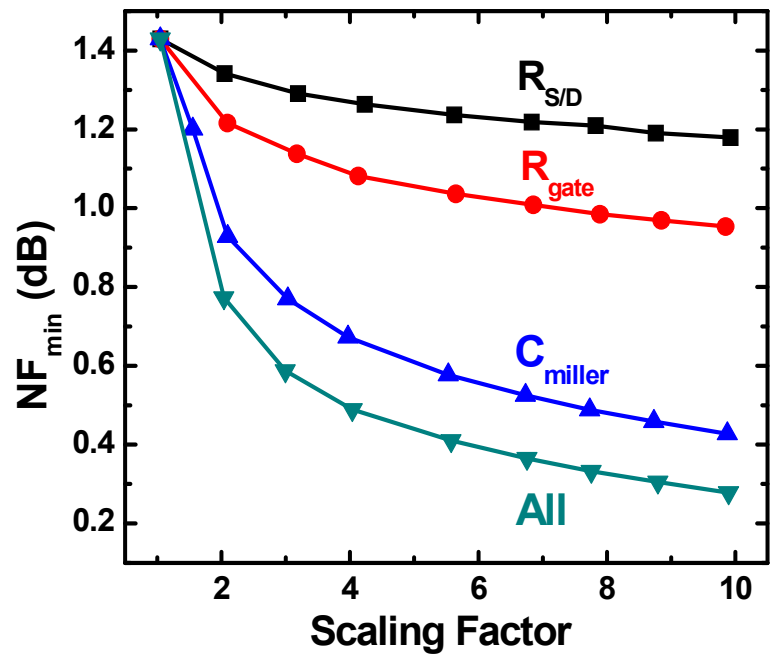
Minimum Noise Figure (NF_{min})

28nm LSTP Technology



M.-T. Yang, VLSI-T (2011)

FinFET

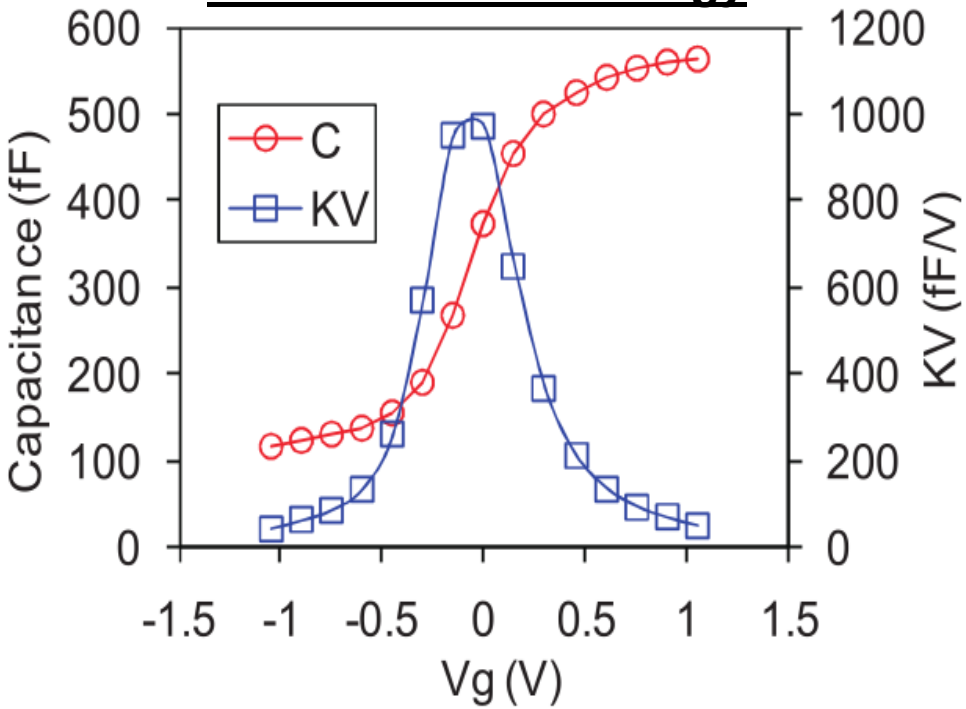


M. Badaroglu, IEDM Tutorial (2012)

- A measure of the degradation of SNR, defined as: $NF = log_{10}\left(\frac{SNR_{IN}}{SNR_{OUT}}\right)$
- Minimizing the Miller capacitance is the key to achieve low NF_{min} in FinFETs.

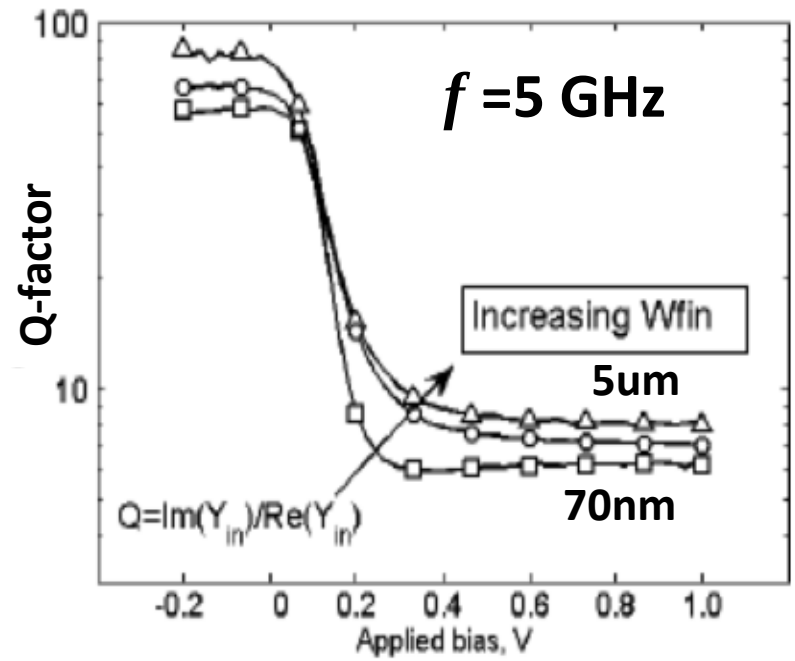
MOS Varactors

28nm LSTP Technology



M.-T. Yang, VLSI-T (2011)

FinFET

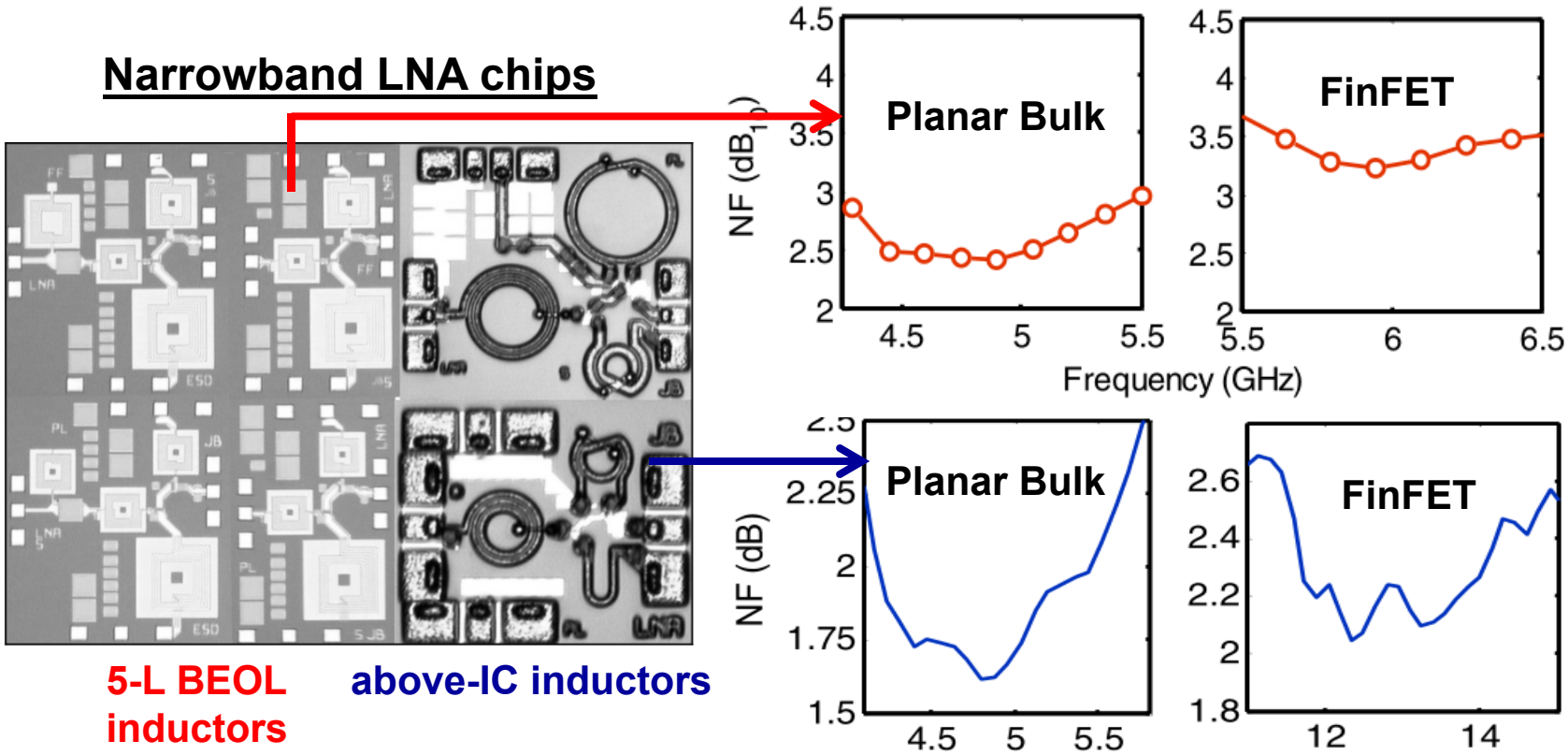


P. Wambacq, TED (2007)

- Mainly for VCO,PLL applications
- Capacitive tuning ratio and voltage swing are two major metrics

- Large $R_{S/D}$ limits the quality factor (Q).
  → Use wide (quasi-planar) fins for VCO

FinFET-based LNA Example

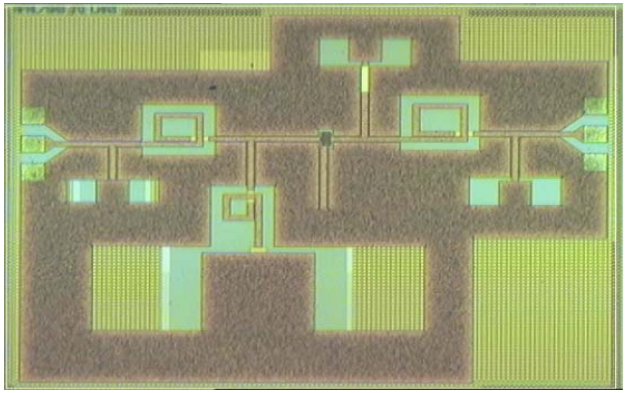


J. Borremans, RFIC (2008)

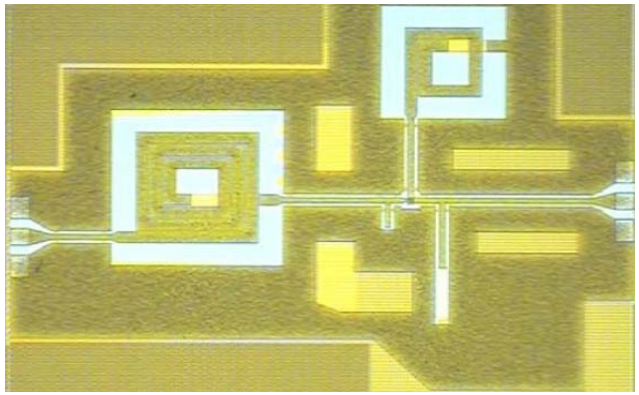
- FinFET-based LNA has degraded NF compared to planar bulk MOSFET based designs, irrespective of inductor integration scheme.

FDSOI-based LNA Example

Narrowband



Broadband



@ V_{gs}=0.75V; V_{ds}=1.0V

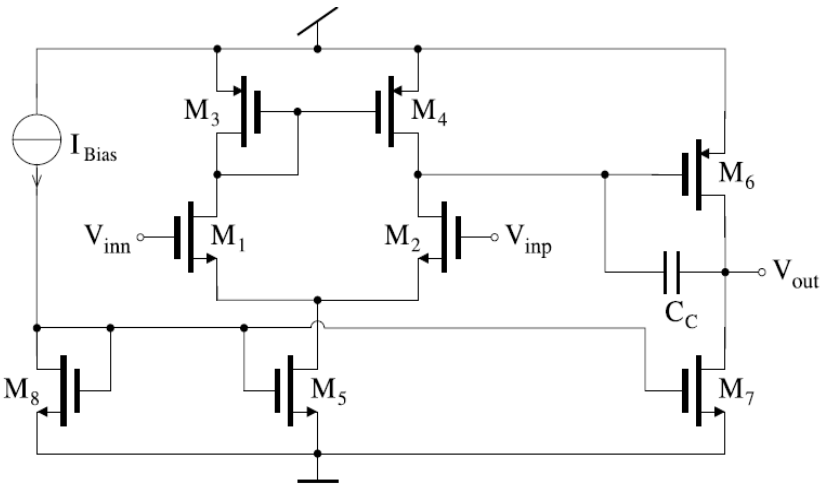
	Center Frequency	Band-width	IIP3 (dBm)	NF (dB)	Gain (dB)
Broadband	3.1 GHz	31%	15.4	2.8-3.0	7.6-4.5
Narrowband	7.5 GHz	67%	12.8	1.3-1.7	9.5-6.5

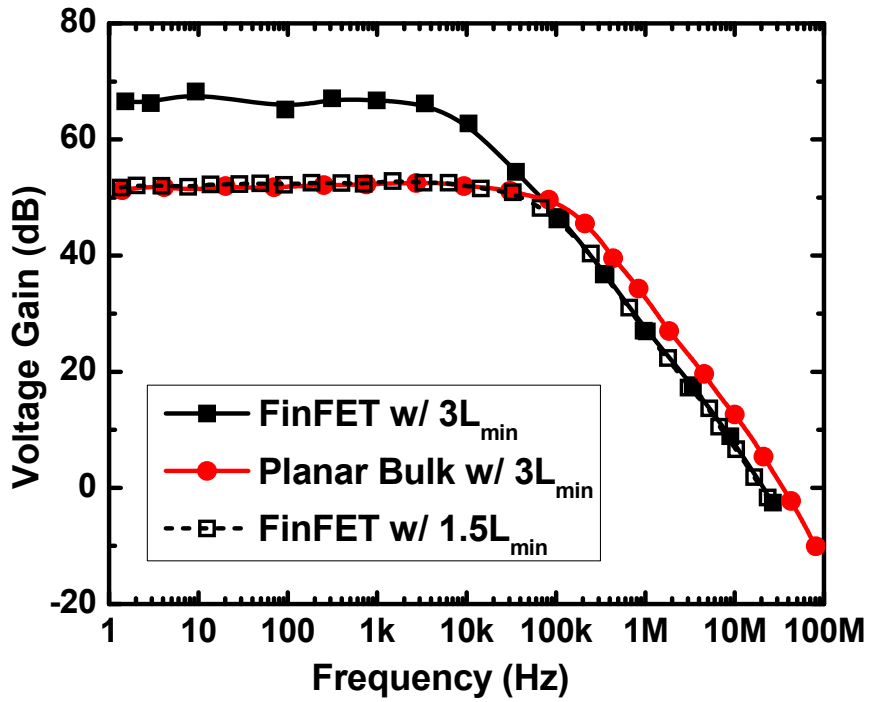
A. Mattamana, Si RF Sys. (2006)

- **FD-SOI MOSFET-based LNA shows good performance.**

FinFET-based OPA Example

Operational Amplifier Circuit Diagram





M. Fulde, *Springer Series in Adv. Microelec.* (2010)

- FinFET has higher open-loop gain (by ~20 dB)
- However, gain is lower at higher frequencies due to large $R_{S/D}$.

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