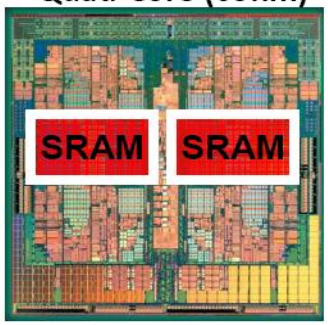
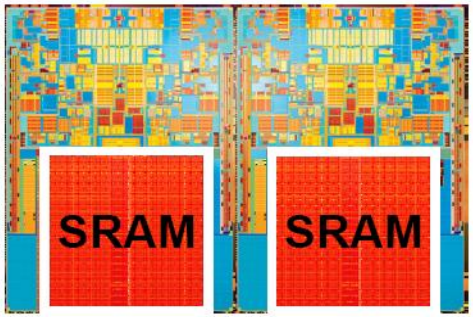
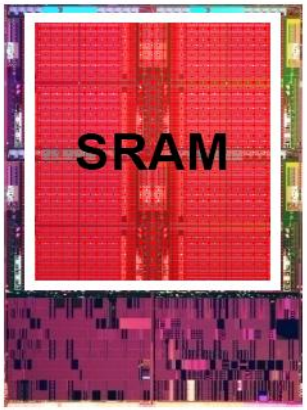
AMD Opteron Quad-Core (65nm)

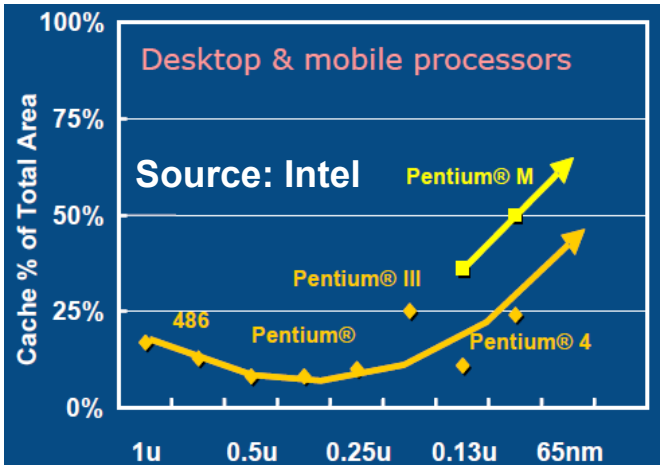


Intel Xeon Quad-Core (45nm)



Intel 22nm test chip





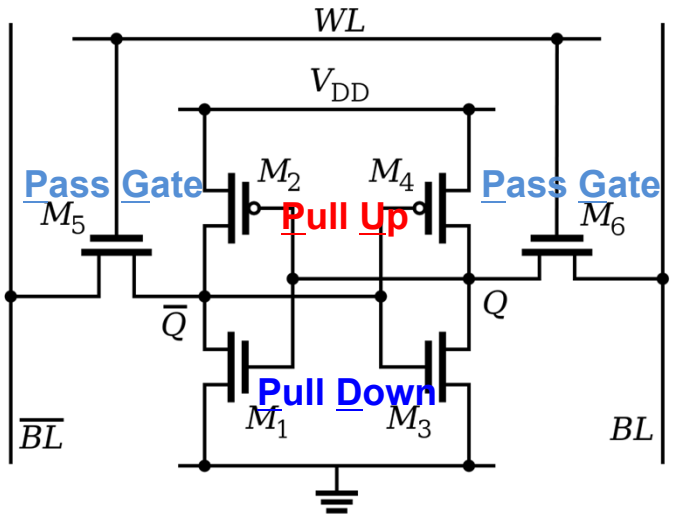
the area ratio of SRAM over logic increases …

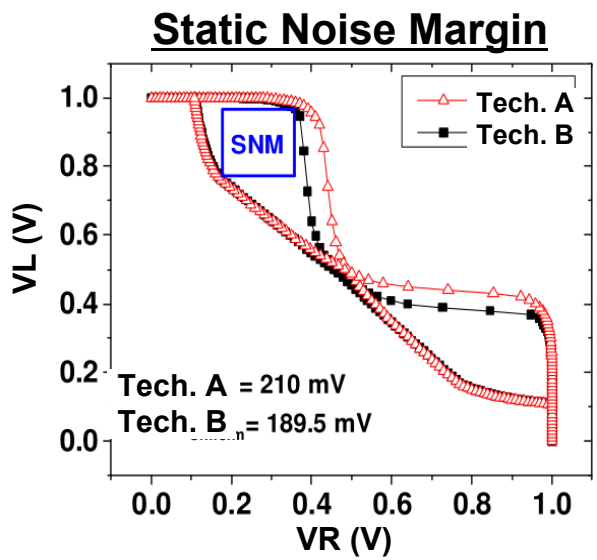
Lecture 14

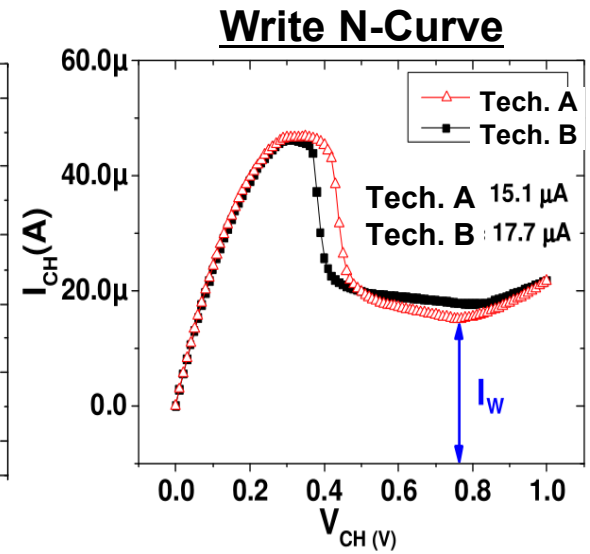
- **Advanced Technologies on SRAM**
  - Fundamentals of SRAM
  - State-of-the-Art SRAM Performance
  - FinFET-based SRAM Issues
  - SRAM Alternatives

<u>Reading</u>: multiple research articles (reference list at the end of this lecture)

Static Random Access Memory (SRAM)







Design:

- Typically consists of 6 MOSFETs (6T), including 2 cross-coupled invertors ($M_{1\text{-}4}$) and 2 access transistors ($M_{5,6}$)
- Wordlines and (differential signal) Bitlines

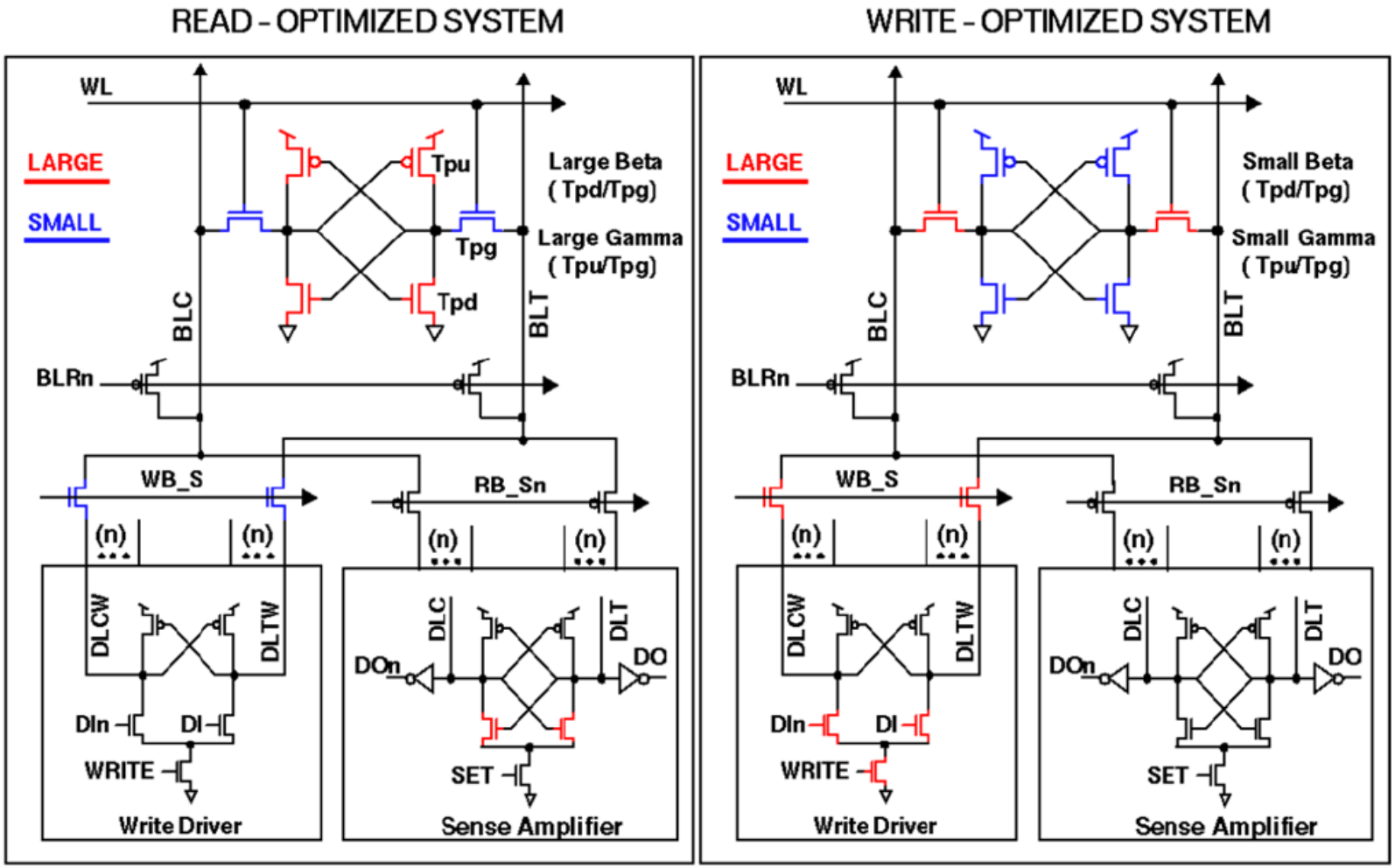
Operation:

- **Standby**: WL = 0
- **Read**: WL = 1, BL = $\overline{BL}$ = 1
  then $\overline{BL}$ discharged to 0 by M_1
- **Write**: WL = 1
  BL = 1, $\overline{BL}$ = 0 → content = 0
  BL = 0, $\overline{BL}$ = 1 → content = 1

Performance:

- SNM
- Read Current
- Write Noise Margin (WNM)
- Write Current

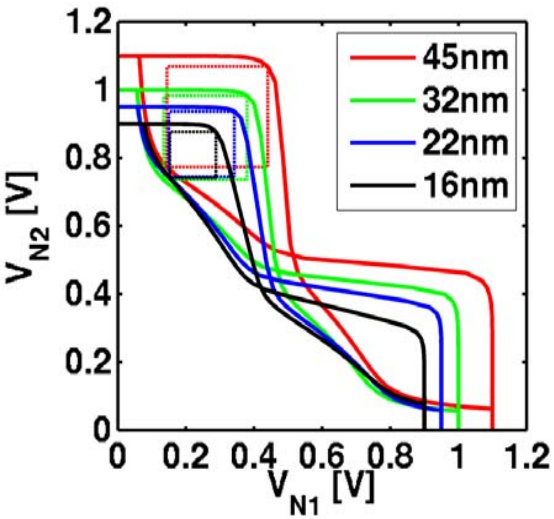
6T SRAM Design Trade-Offs: Read *vs*. Write



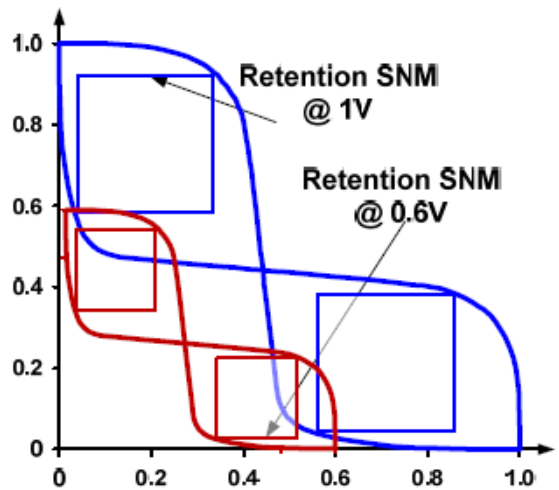
H. Pilo, IEDM Short Course (2006)

SRAM Technology Scaling Challenges

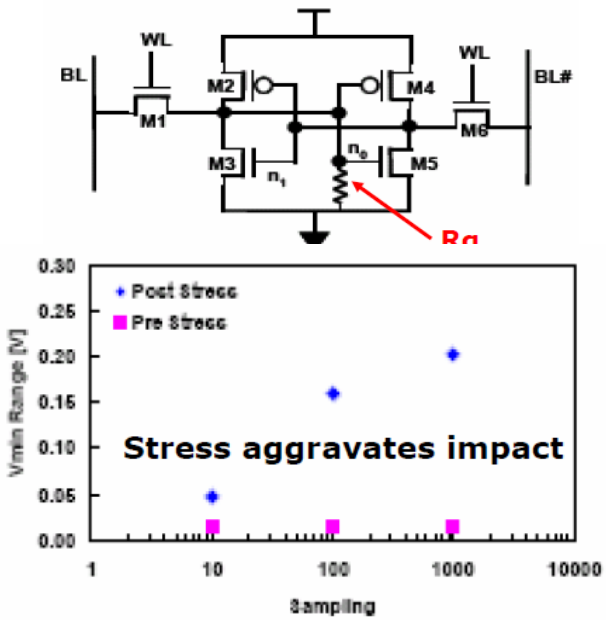
Degraded Electrostatics



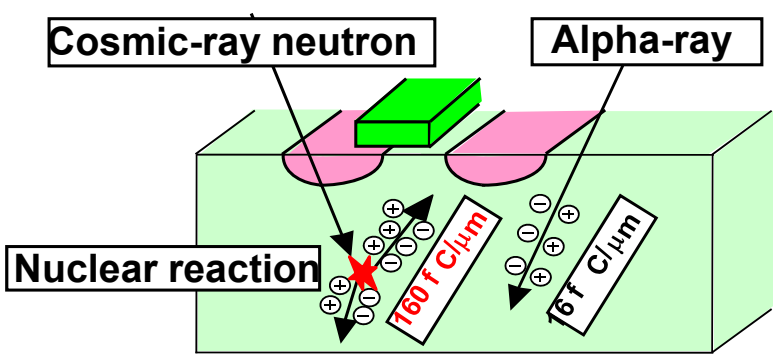
Reduced V_{DD}



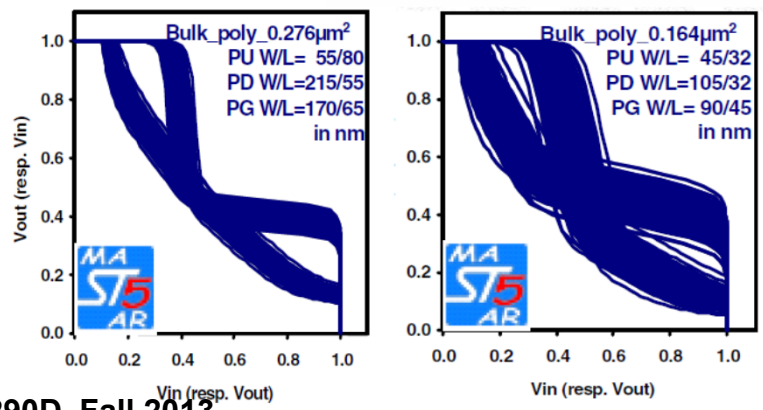
Gate Leakage



Soft-Errors



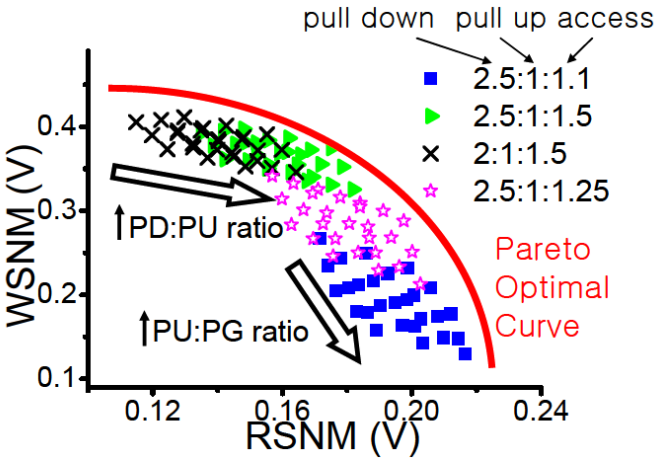
Variability



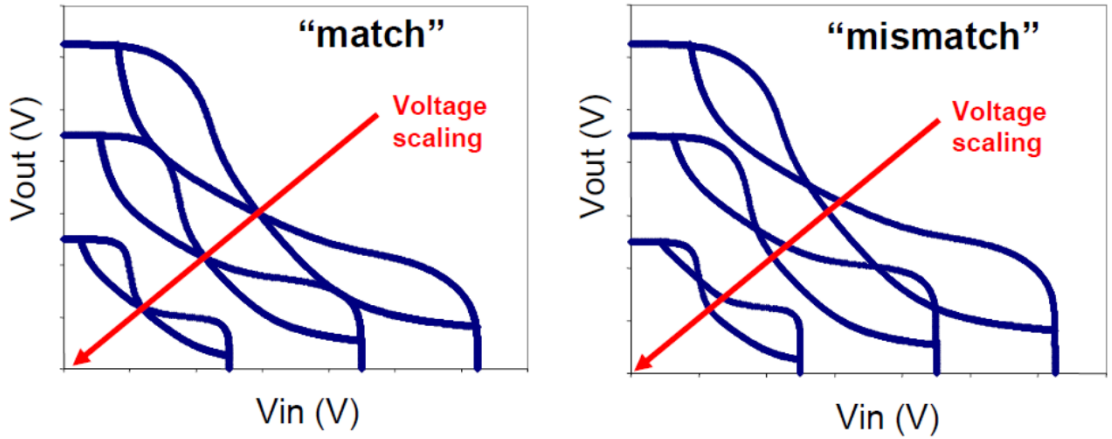
Impacts of Performance Variability

- Why variability is extremely harmful to SRAM?

- **SRAM always uses minimum transistor size, to reduce cell area.**
  → Poor immunity to random and systematic variability
- **Read *vs*. Write conflicts; Voltage loss on PG during Read**
- **V_{TH} mismatch results in significantly reduced SNM.**
  → Lowers SRAM cell yield, and limits V_{DD} scaling



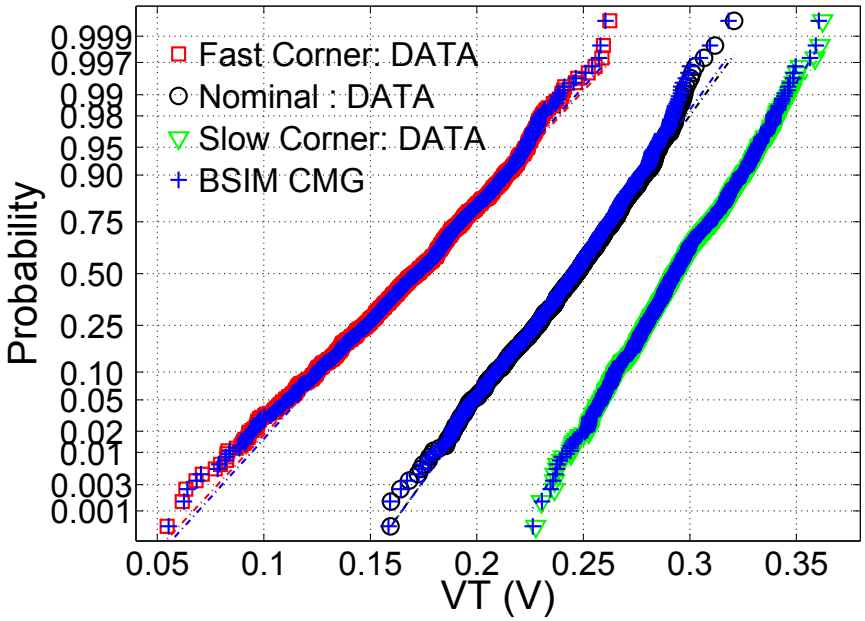
J. Luo, SSDM (2010)

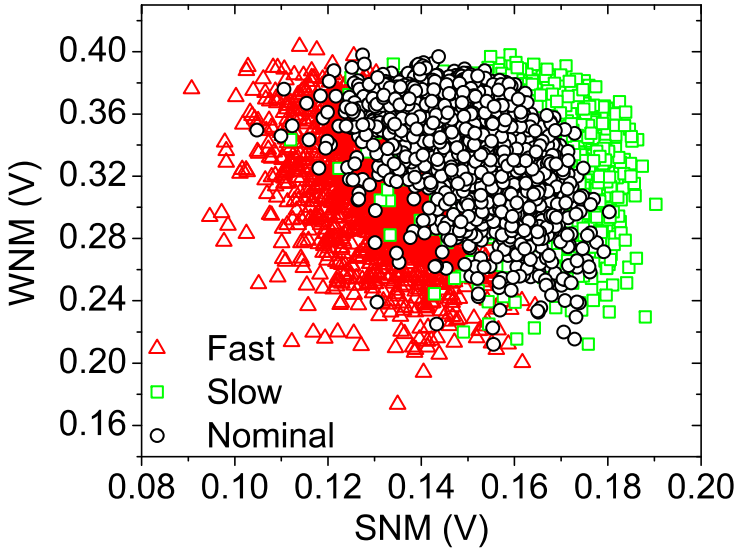


K. Zhang, VLSI (2004)

- **Immunity to short-channel effects, as well as performance variations is needed to achieve high SRAM cell yield.**

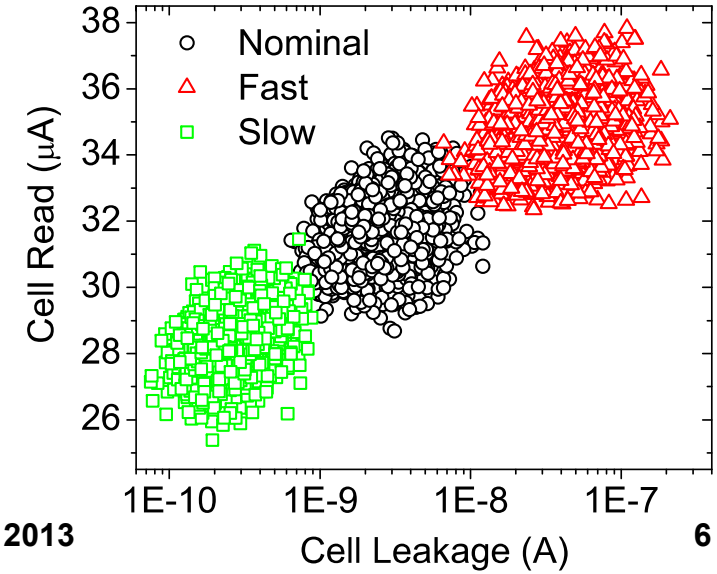
Impact of Technology Flavors





- **Different technology favors are implemented by V_{TH} engineering**
- **Fast switching device has less Read and Write stability, as well as larger cell leakage (standby power).**

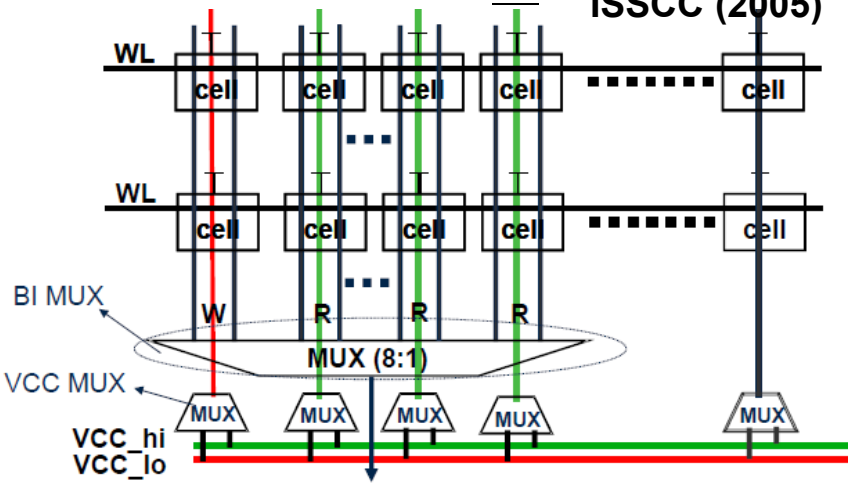
X. Wang, ESSDERC, 2012



Circuit Techniques to Improve SRAM Stability

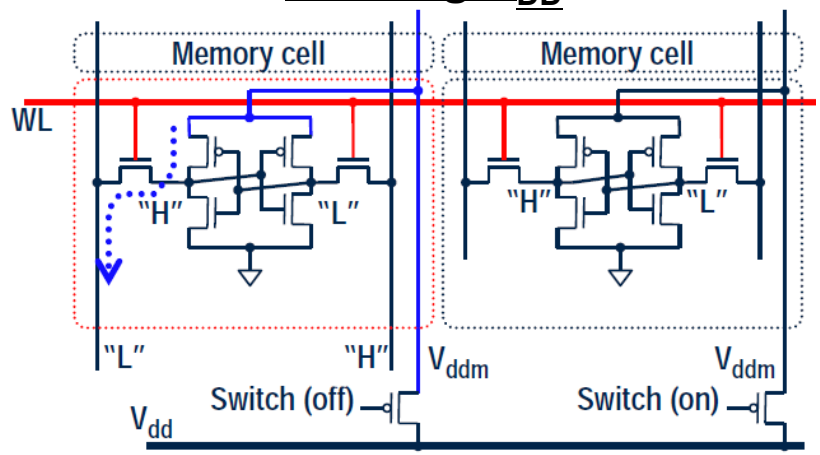
Dynamic V_{DD}

K. Zhang, ISSCC (2005)



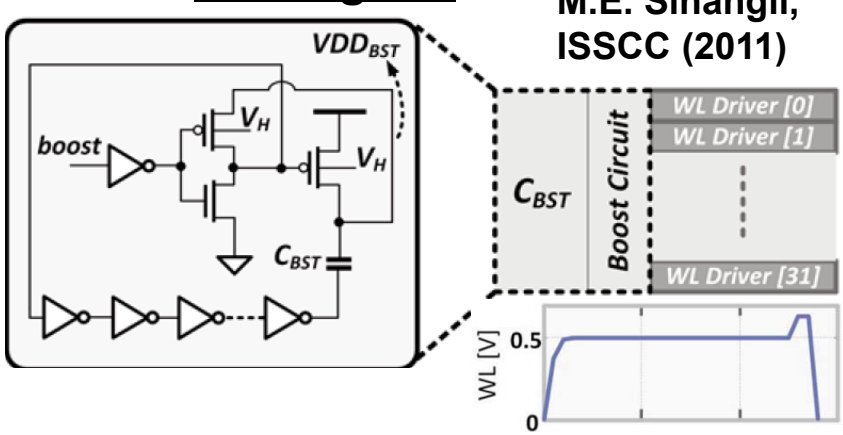
Floating V_{DD}

M. Yamaoka, ISSCC (2004)



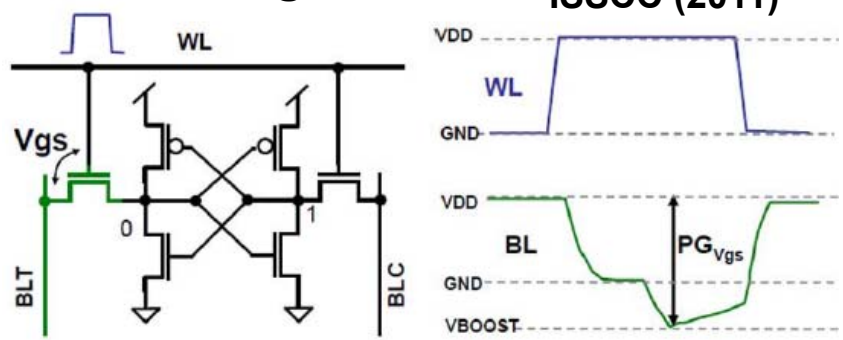
Pulsing WL

M.E. Sinangil, ISSCC (2011)



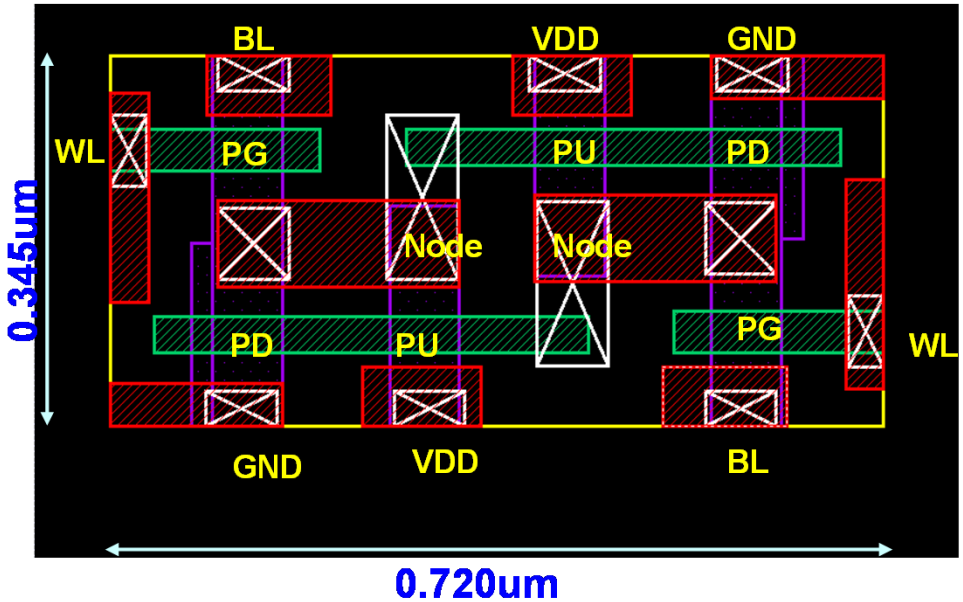
Negative BL

H. Pilo, ISSCC (2011)



45nm 6T SRAM Design Rules

PD NMOS: W/L_g = 85/34 nm
PG NMOS: W/L_g = 65/39 nm
PU PMOS: W/L_g = 65/34 nm
Contact Size : 66nm
Gate-Cont. space : 35nm
Well Isolation : 100nm
P+/P+ Isolation : 70nm
DT Ratio : 1.50
DT Ratio(W) : 1.31

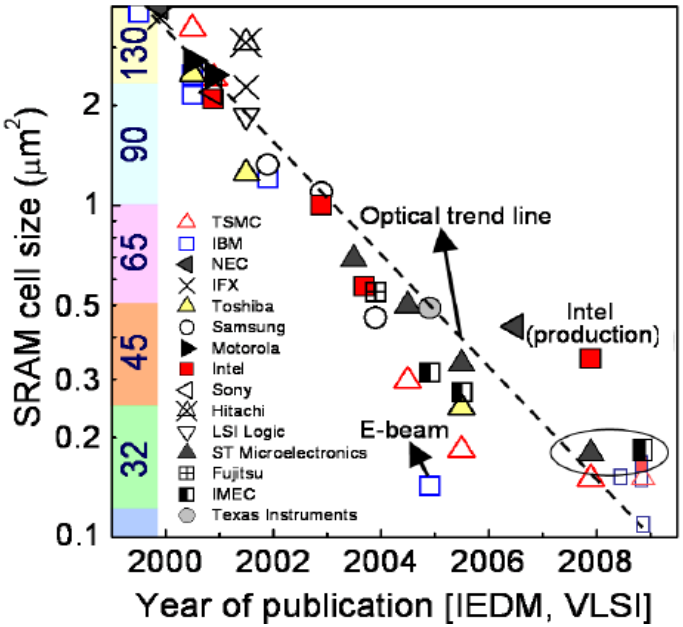


Cell Size : 0.72 × 0.345=0.248um^2

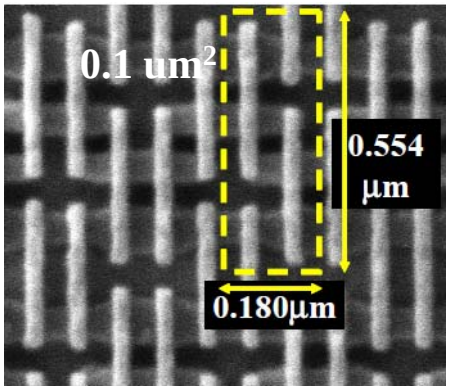
- **<u>Imposed by OPC</u>**, SRAM cell layout evolved from arbitrary shapes to predominantly straight lines and holes.
- **<u>Imposed by Double Patterning</u>**, poly-gates are oriented in the same direction

H. Nii, IEDM (2006) & after S. Yu (ASU, 2013)

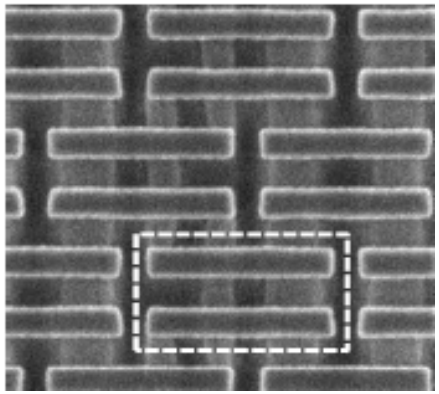
State-of-the-Art SRAM Cell Area



IBM 22nm PD-SOI

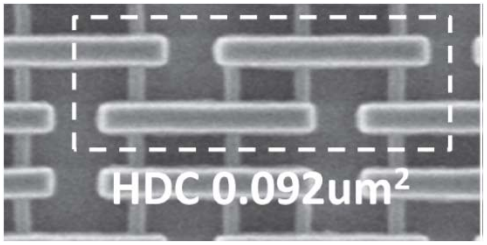


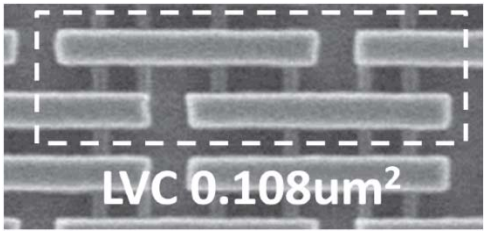
Samsung 20nm Bulk



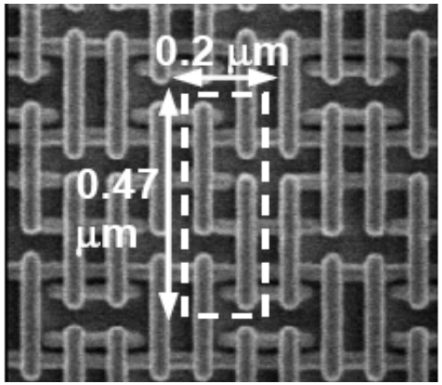
Planar Platforms

Intel 22nm Tri-Gate



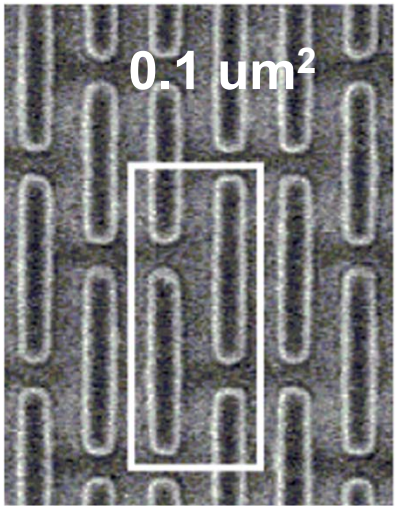


IBM 22nm FinFET



0.094 um²
0.076 um²
0.063 um²

TSMC 20nm FinFET

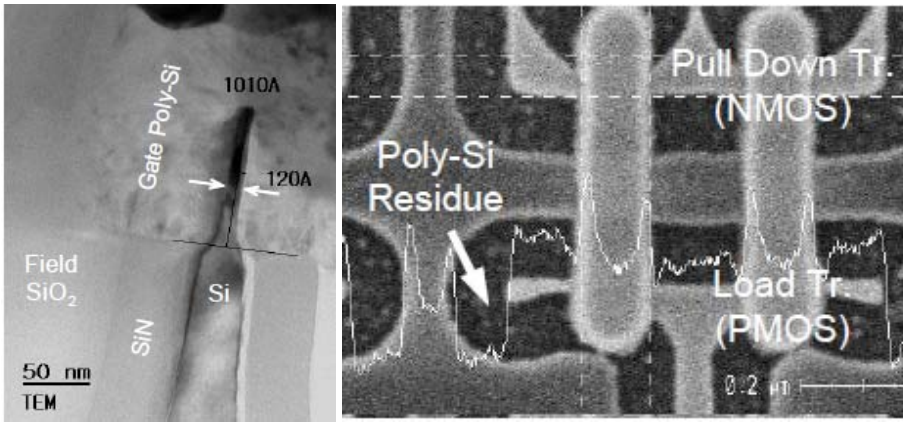


State-of-the-Art SRAM Performance

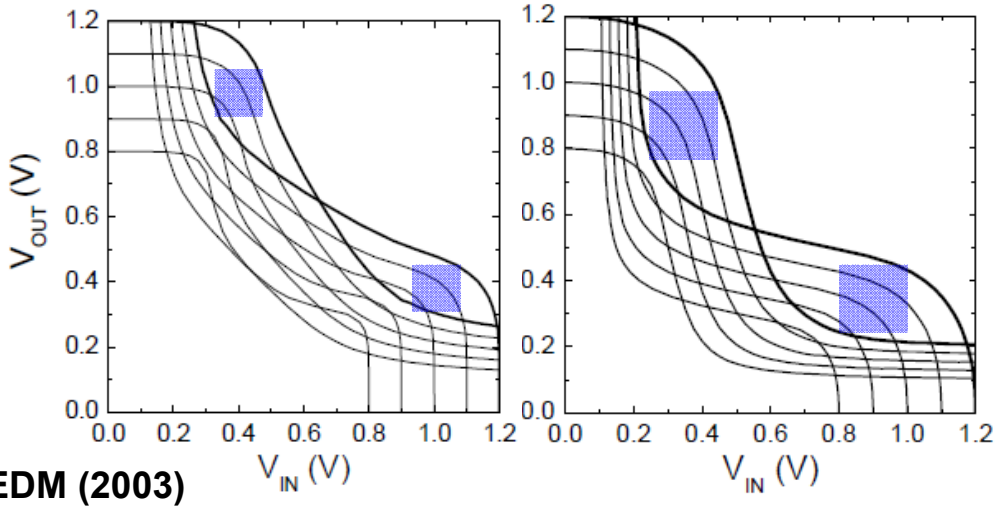
	Company	Node (nm)	Area (um^2)	$V_{DD,1}$ (V)	SNM_1 (V)	$V_{DD,2}$ (V)	SNM_2 (V)	Ref.s
Planar Bulk MOSFET	Intel	32	0.171	~0.9	~0.2			IEDM 09
	TSMC	32	0.15	1.0	0.22	0.8	0.2	
	IBM	32	0.157	0.9	0.213			IEDM 08
	UMC	28	0.124	0.9	0.179	0.7	0.144	VLSI 11
	Samsung	20		0.9	0.255			IEDM 11
	IBM	22 PDSOI	0.1	0.9	0.22	0.7	0.148	IEDM 08
FinFETs	IBM	22	0.094 0.063	0.8 0.8	0.2 0.15	0.4 0.4	0.1 0.05	VLSI 10
	TSMC	20	0.1	0.85 0.65		0.45	0.09	IEDM 10
	Intel	22	0.092 0.108					ISSCC 12

FinFET Advantages and Challenges in 6T SRAM Design

TEM & SEM of a bulk FinFET-based SRAM cell



SNM of (left) planar control & (right) FinFET SRAMs

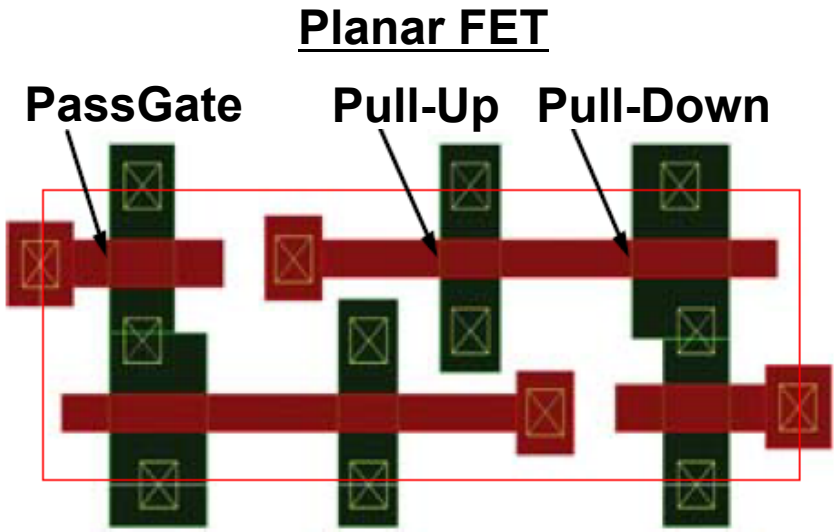


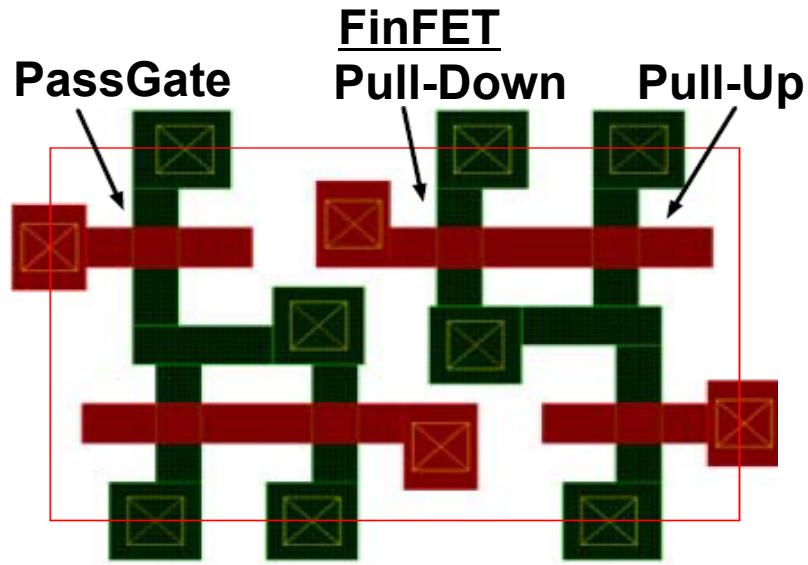
T. Park, IEDM (2003)

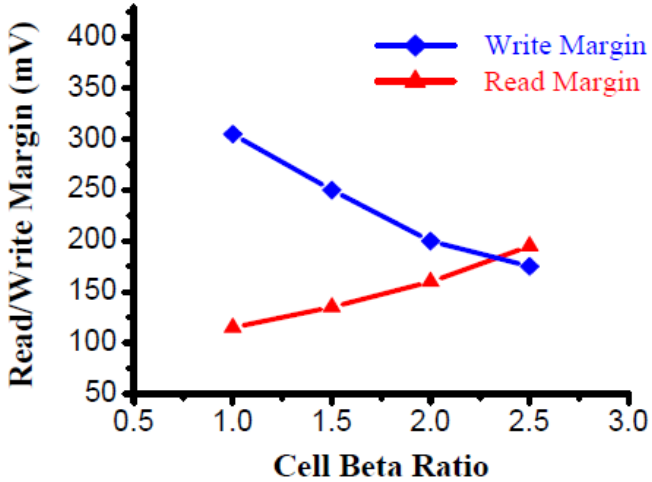
- ***Pros***:
  - ✓ Improved SS → Lower V_{TH} at given I_{OFF} → Higher I_{Read}, I_{write}
  - ✓ Reduced DIBL → Larger output resistance → larger SNM
  - ✓ Reduced performance variability (LER & RDF-induced) → larger SNM
- ***Cons***:
  - × Effective width quantization
  - × V_{TH} engineering is difficult

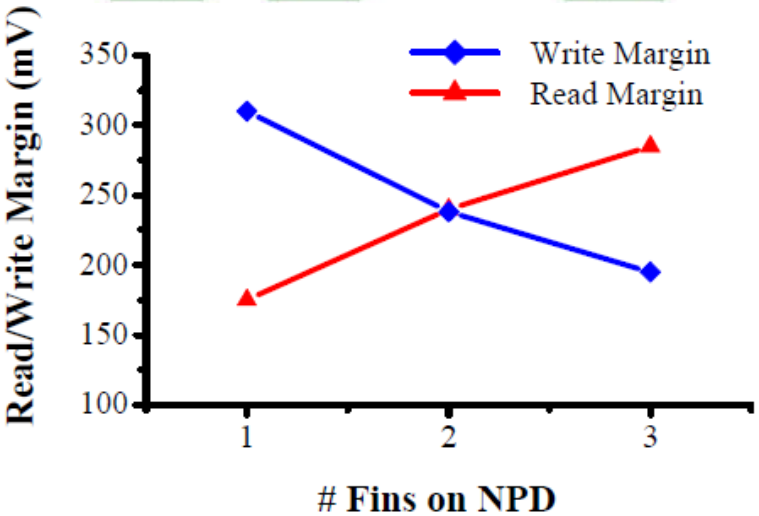
  } limited design space, have to use different L_g, hindering cell area scaling…

Planar FET *vs*. FinFET SRAM Design

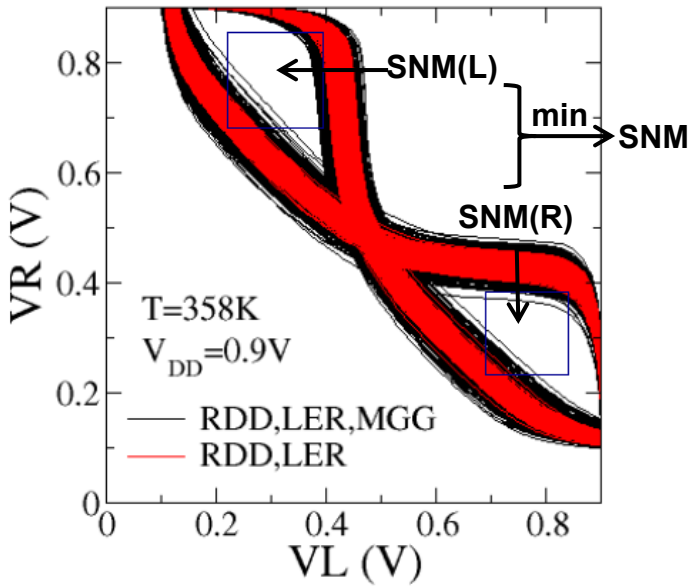


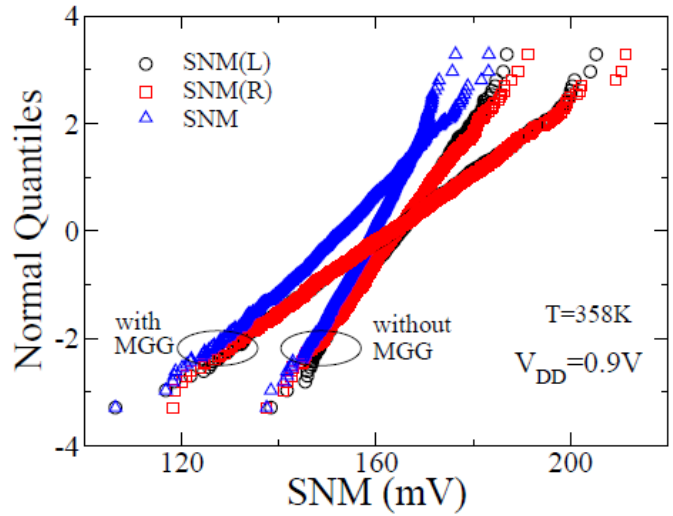


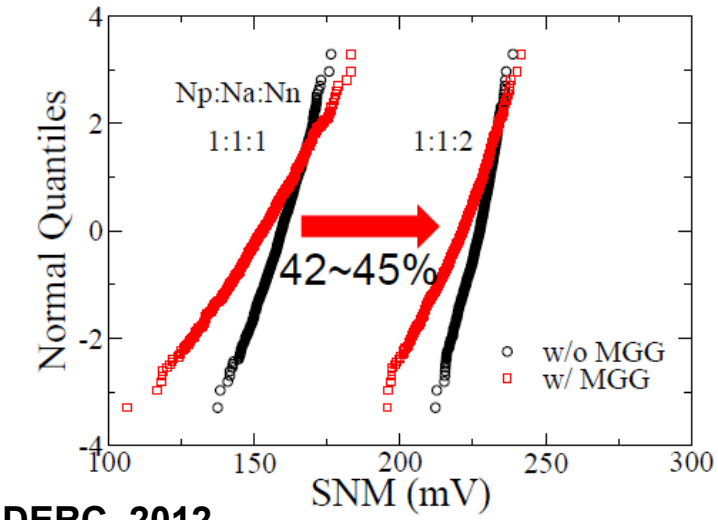




Impact of Performance Variability on FinFET-based SNM







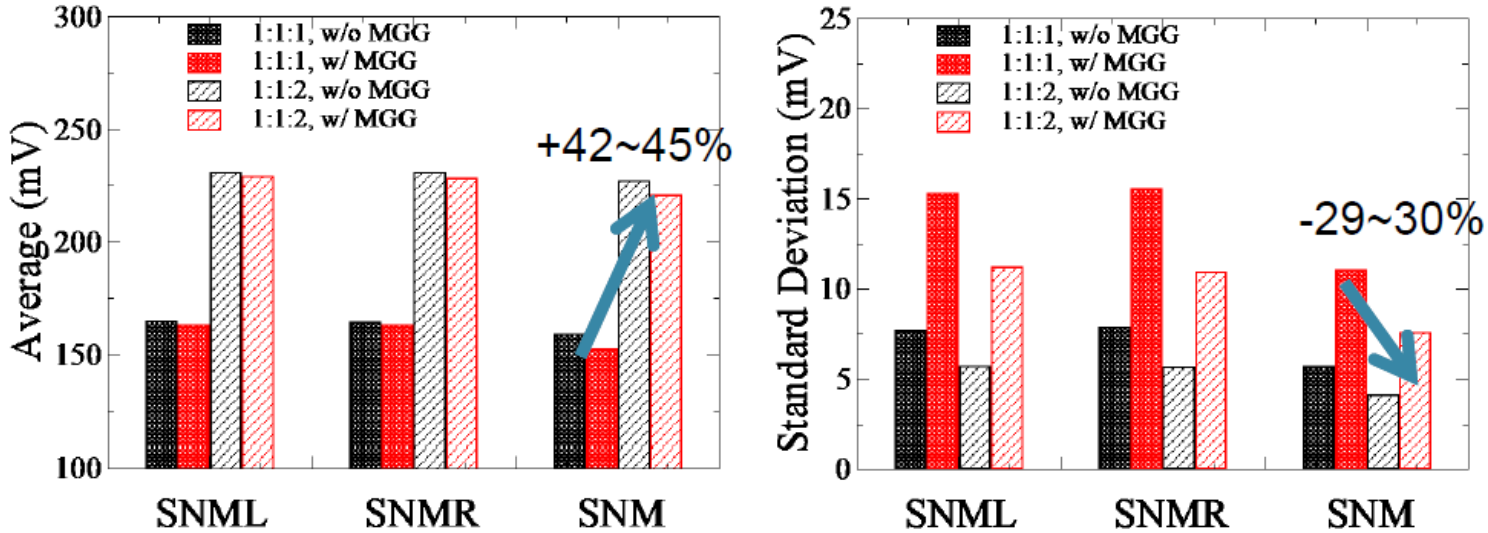
Butterfly curves subject to statistical variability sources. Left tail is close to Gaussian.

Fin number affects SNM distribution

X. Wang, ESSDERC, 2012

FinFET-based SRAM SNM Enhancement

PU: PG: PD



- **Metal-Gate Granularity (MGG) causes large SNM variation.**
- **2-fin PD design helps to increase SRAM SNM while reduces σV_{TH}, with the cost of 20% cell area increase.**

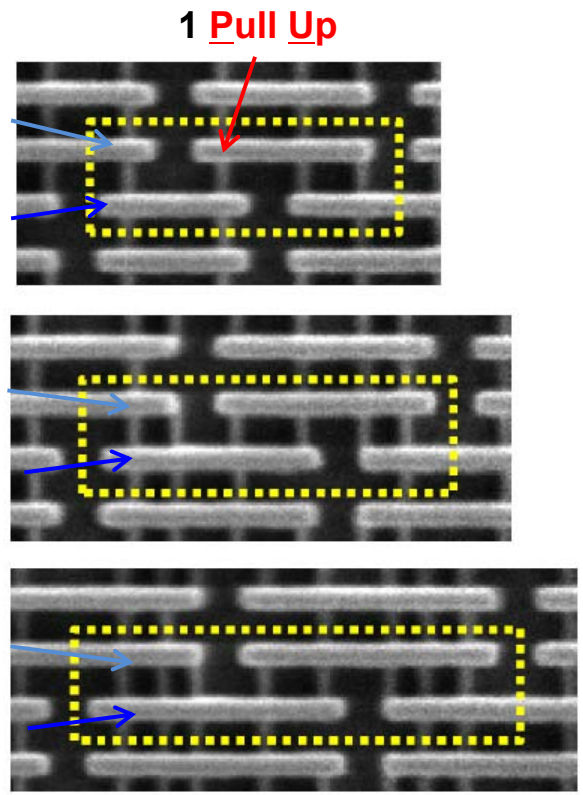
X. Wang, ESSDERC, 2012

Intel's 22nm SRAM: Tri-Gate Technology

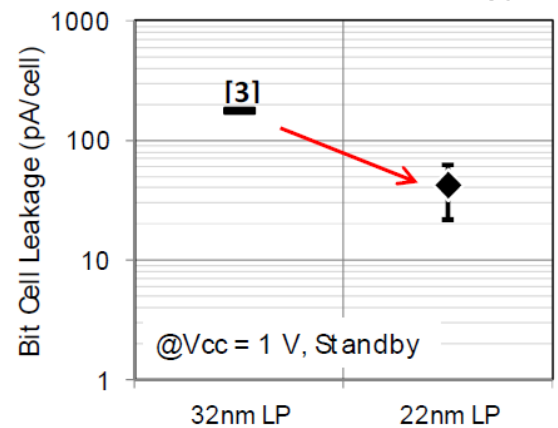
High Density & Low Leakage Cell (0.092 um²)

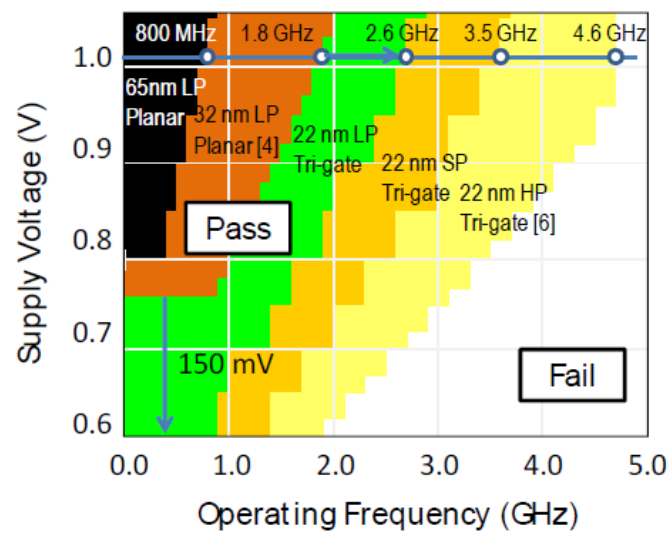
Low Voltage Cell (0.108 um²)

High Speed Cell (0.130 um²)



power & performance compared to planar bulk technology

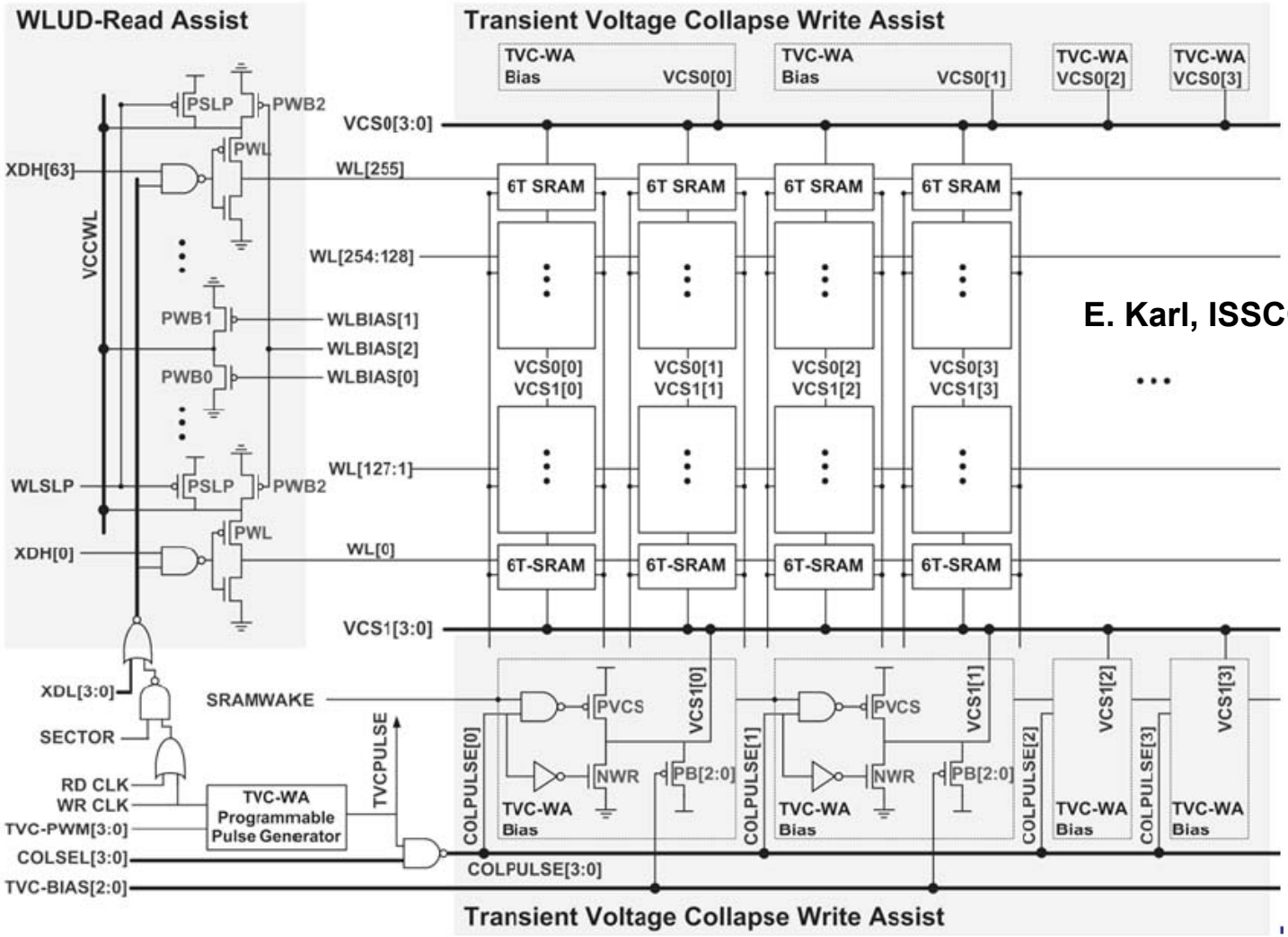




- **Different SRAM families are implemented by using different # of PD and PG fins.**
- **4-5 times standby power reduction due to supreme SCE control.**

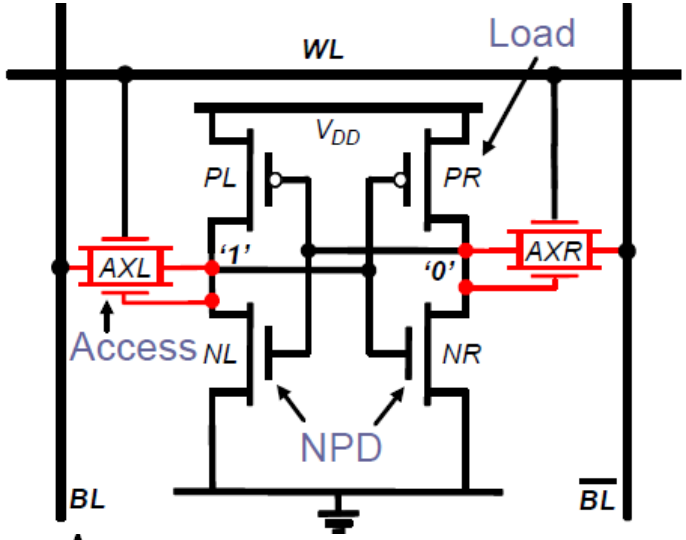
C.-H. Jan, IEDM (2012)

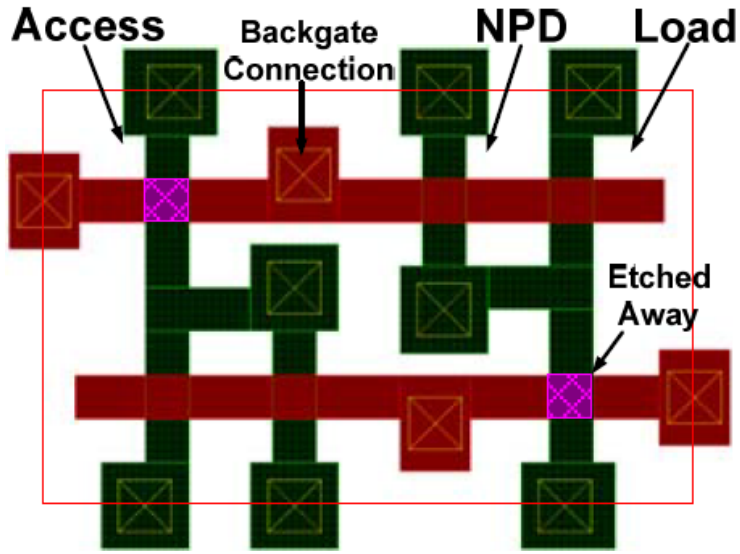
Intel's 22nm SRAM: Collapsing V_{DD} Technique

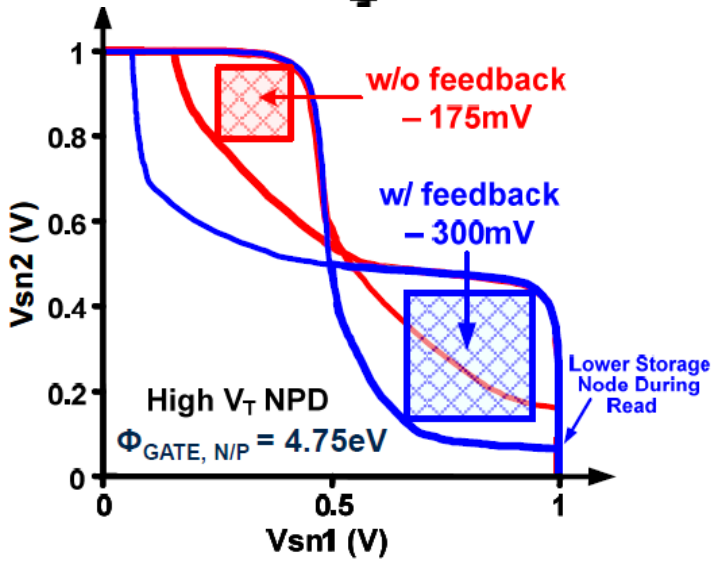


Independent-Gate FinFET-based SRAM Design

Z. Guo, ISLPED (2005)





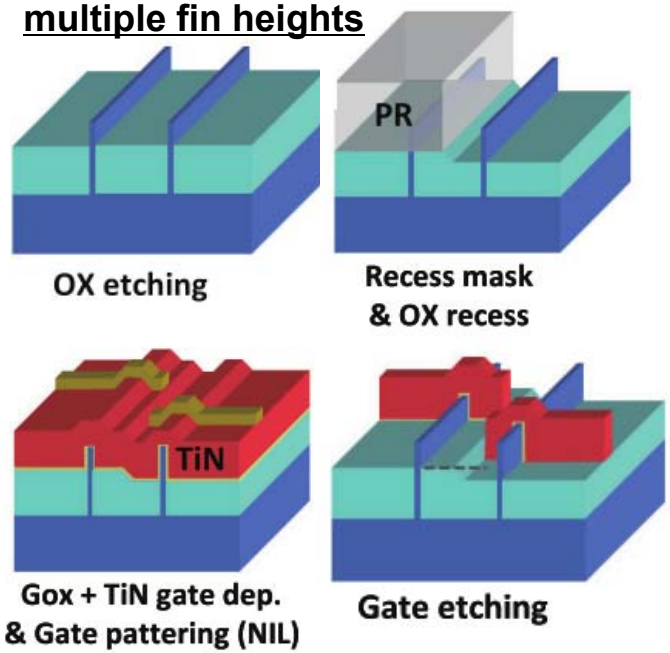


- Enhanced Read margin
- Reduced WL capacitance
- I_{READ} nearly unaffected

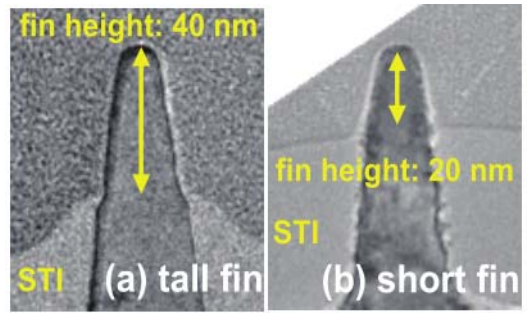
Multiple-Fin-Height FinFET-based SRAM Design

M.-C. Chen, VLSI-T (2013)

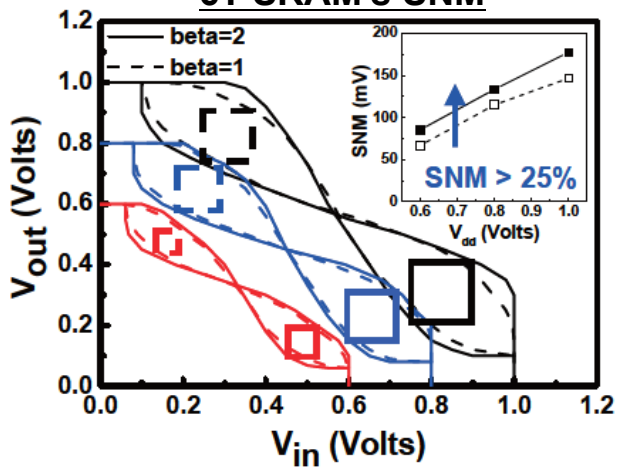
Process flow to form multiple fin heights



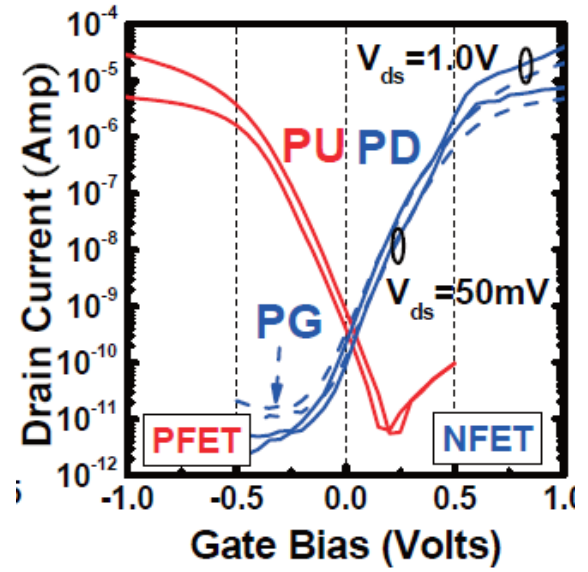
FinFET's TEM



6T SRAM's SNM

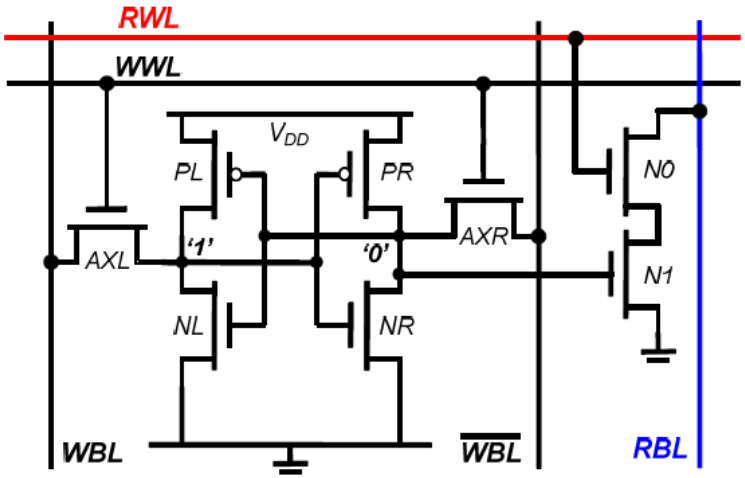


PU, PD and PG FinFETs I_d *vs.* V_g

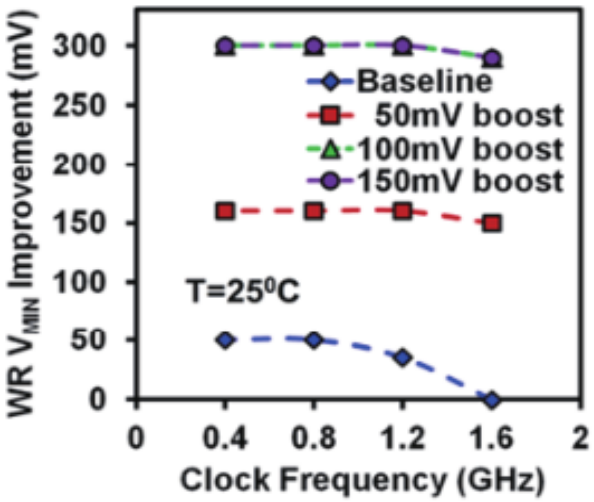


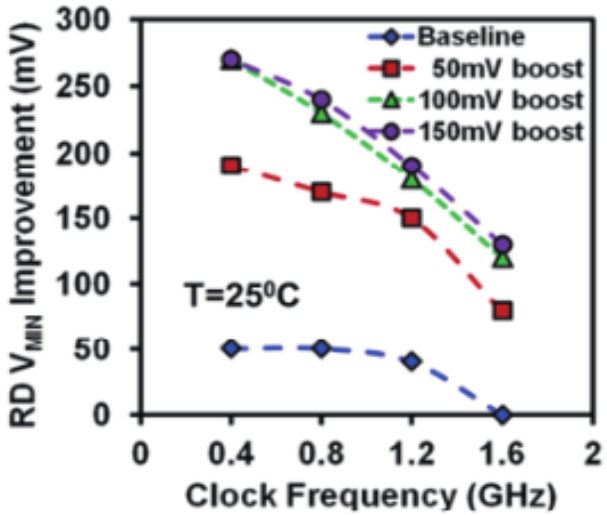
1. Single fin and larger fin heights used for PD NMOS, which reduces over 20% SRAM cell area compared to a 2-fin PD design.
2. Extra lithography steps to pattern fins to 2 heights: 20nm and 40nm

SRAM Alternatives: 8T Cell



- N_0, N_1 separates Read and Write, to lower operation voltage, and hence power consumption.
- Demonstrations on a 14KB 8T-SRAM based on Intel's 22nm Tri-Gate technology: $V_{DD,MIN}$ is lowered by 130-270mV with 27-46% less power consumption.

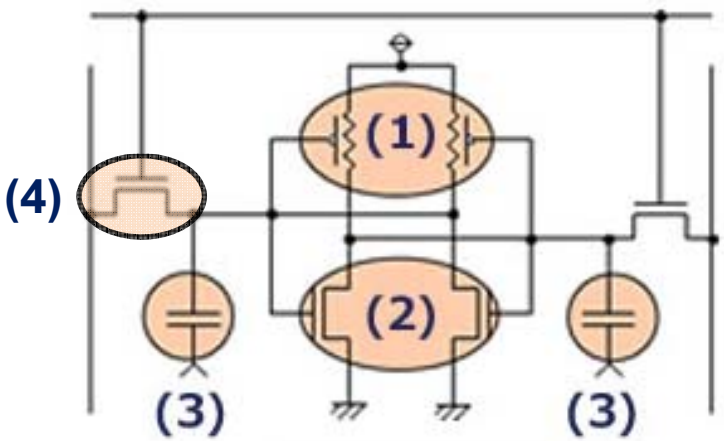


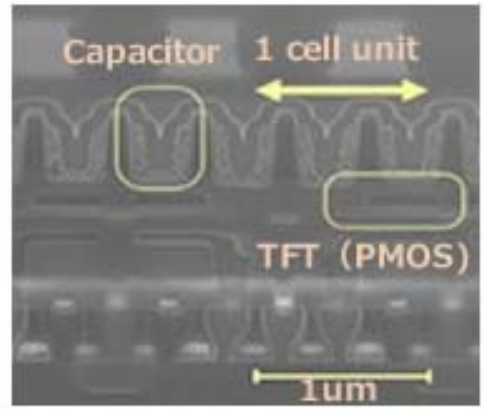


J. Kulkarni, VLSI-C (2013)

SRAM Alternatives: SDRAM & nvSRAM

Renasas' SDRAM





Source: Renasas (2012)

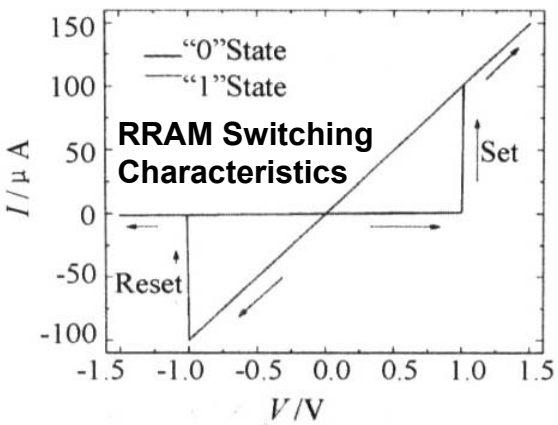
Technology:

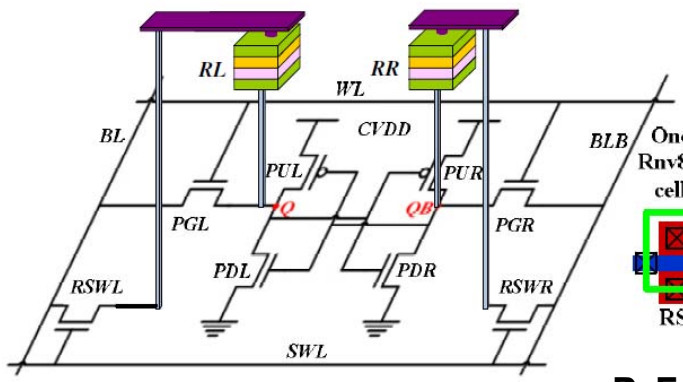
1. Poly TFET as PU PMOS
2. FEOL PD NMOS
3. BEOL MIM Capacitors
4. FEOL PG NMOS as well as the Access Transistors in 1T1R

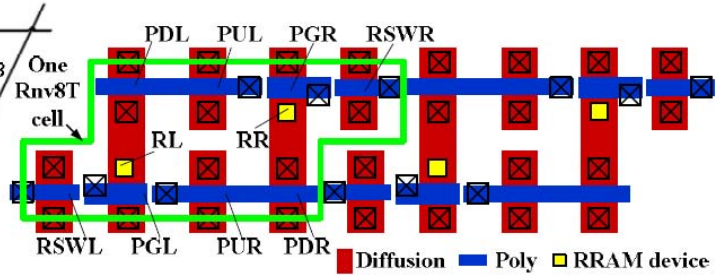
Features:

1. Ultra-low power
2. Immunity to soft errors

8T2R nvSRAM



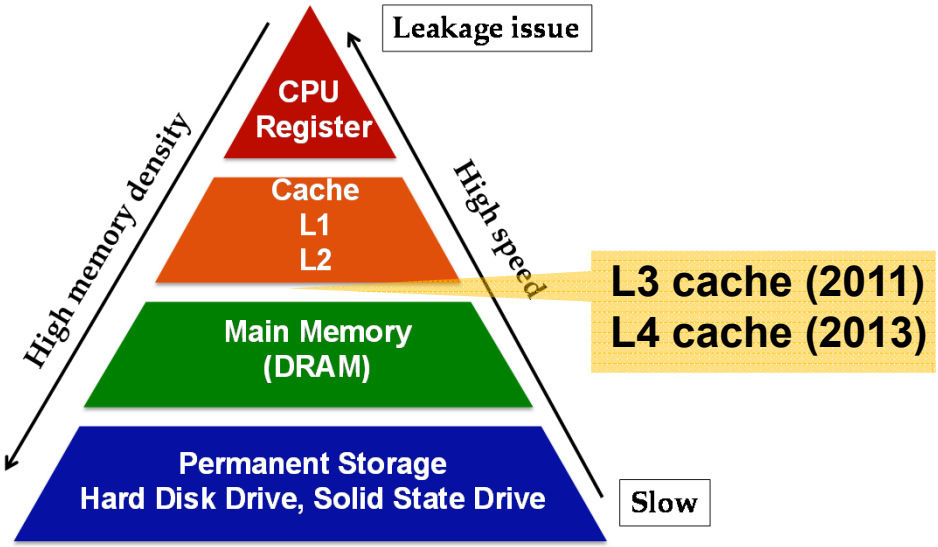




P.-F. Chiu, VLSI (2010)

SRAM Alternatives: Context Memory

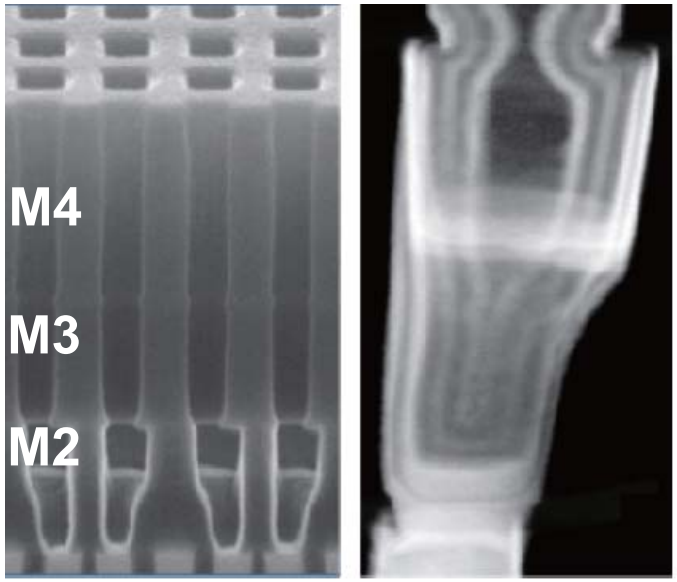
Memory Hierarchy

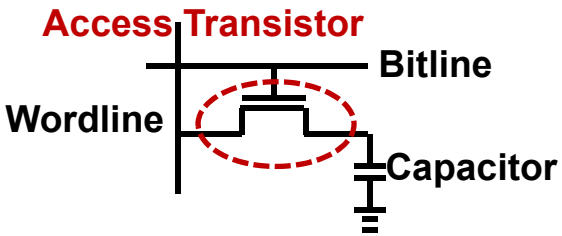


	Access Time (ns)	Feature Size (F^2)
SRAM	0.5 ~ 1	146
eDRAM	5	6

- Higher density yet lower power embedded memories are needed to bridge the performance gap between "logic" and "memory" circuits, and eventually the "*Von Neumann* Bottleneck"?

Intel's embedded DRAM at 22nm





R. Brain, VLSI (2013)

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