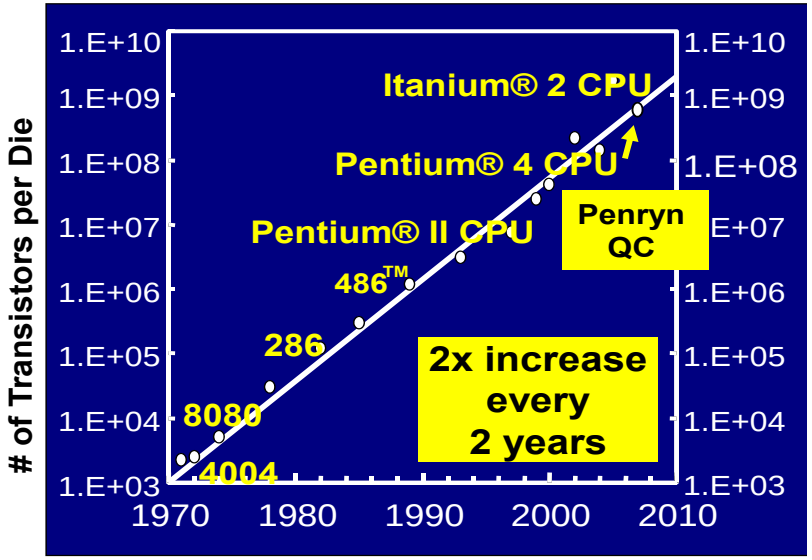
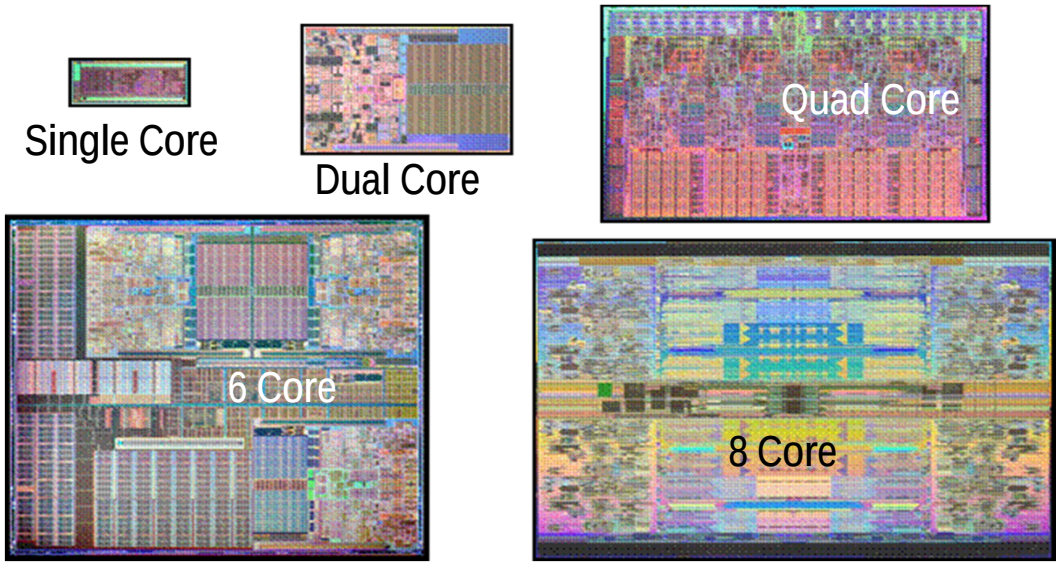




Lecture 13

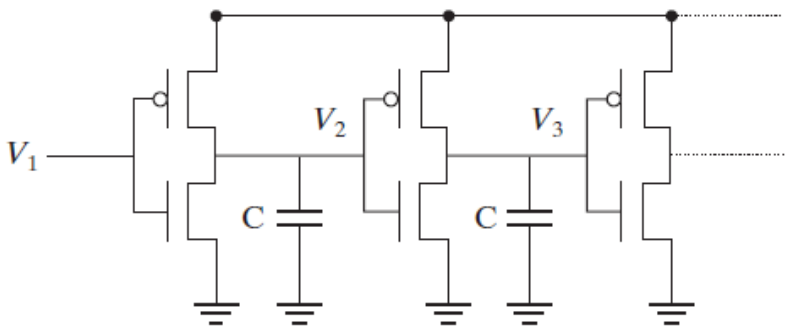
- **Advanced Technologies on Digital Circuits**
  - Performance Metrics for Digital Circuits
  - Impact of Advanced Technologies

<u>Reading</u>:

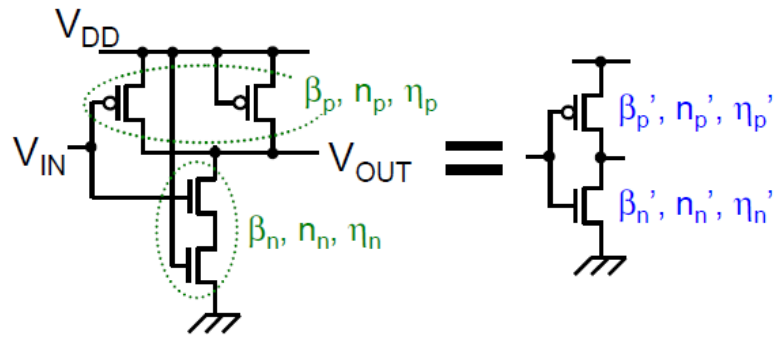
- multiple research articles (reference list at the end of this lecture)
- B. Nikolic, EE 241 course materials, UC Berkeley

Complementary Logic Gates

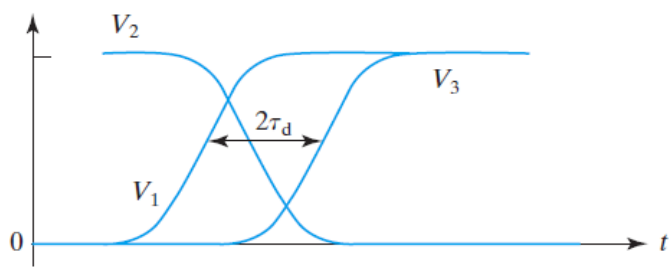
Inverter Chains



Other Combinational Logic Gates



Intrinsic Delay $\tau_d = \frac{1}{2}\left(t_{pHL} + t_{pLH}\right) \cong \frac{CV_{DD}}{2I_{EFF}}$



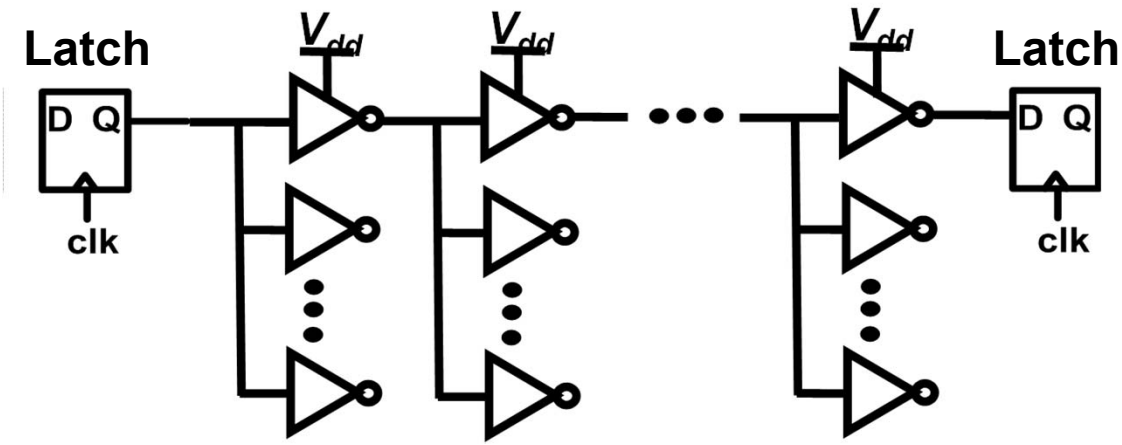
Load capacitance includes:

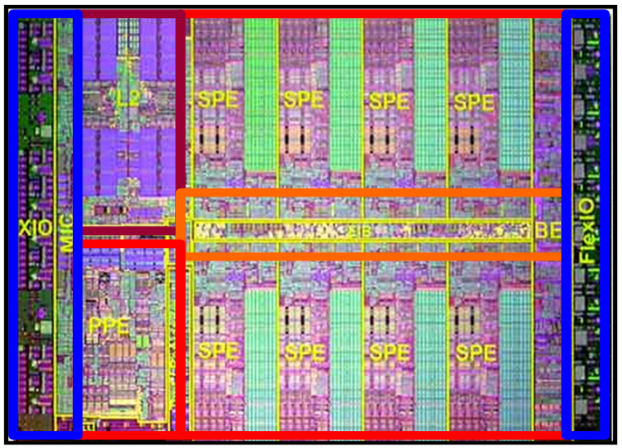
- C_{diff}
- (effective) fanout cap.s
  - C_{GG}
  - C_{fringe}
- C_{wire}

- **τ_d is reduced by increasing I_{EFF} and reducing load capacitance *C*.**

Energy & Delay of Digital Circuits

approximated model for the data path:
(this may not be the latency-optimized design, but the energy-optimized one.)





- *LD* : Logic Depth
- *F* : effective Fanout per stage
- *α* : Activity Factor

$$t_{delay} = LD \cdot F \cdot CV_{DD}/(2I_{EFF})$$

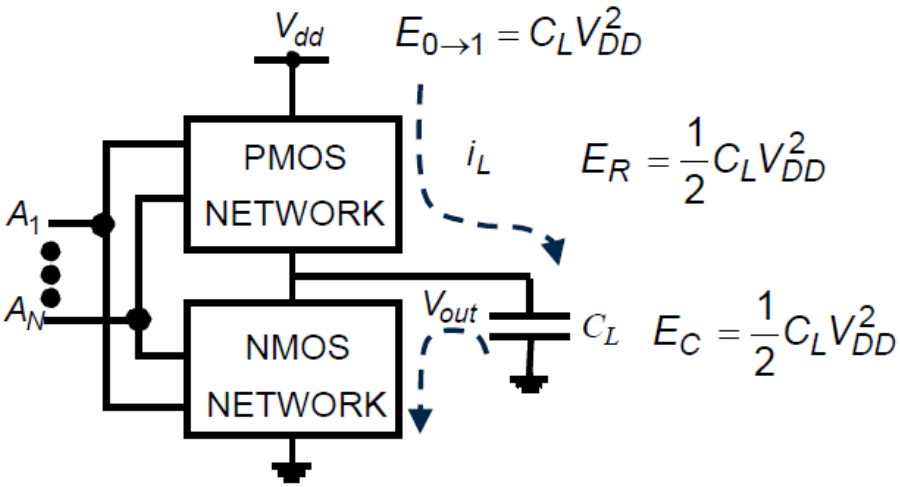
$$E_{dyn} + E_{leak} = \alpha \cdot LD \cdot F \cdot CV_{DD}^2 + LD \cdot F \cdot I_{OFF} V_{DD} t_{delay}$$

$$= \alpha \cdot LD \cdot F \cdot CV_{DD}^2 \left[1 + (LD \cdot F / 2\alpha) / (I_{EFF}/I_{OFF}) \right]$$

Courtesy of E. Alon (UC Berkeley)

Activity Factor Calculation

Energy Delivery Path during 0→1 at Output:



Energy consumed during N cycles: $E_N = C_L \cdot V_{DD}^2 \cdot n_{0\to1}$

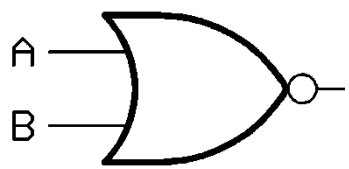
$n_{0\to1}$ – number of 0→1 transitions in *N* cycles

$$P_{avg} = \lim_{N\to\infty} \frac{E_N}{N} \cdot f = \left(\lim_{N\to\infty} \frac{n_{0\to1}}{N} \right) \cdot C_L \cdot V_{DD}^2 \cdot f$$

$$\alpha_{0\to1} = \lim_{N\to\infty} \frac{n_{0\to1}}{N}$$

$$\boxed{P_{avg} = \alpha_{0\to1} \cdot C_L \cdot V_{DD}^2 \cdot f}$$

Example: A 2-input NOR Gate



Truth Table

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Assume signal probabilities

$p_{A=1} = 1/2$

$p_{B=1} = 1/2$

Then transition probability

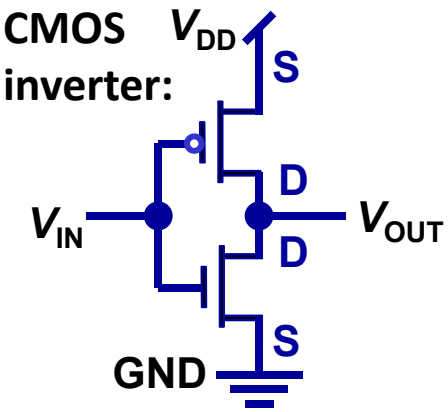
$p_{0\to1} = p_{Out=0} \times p_{Out=1}$

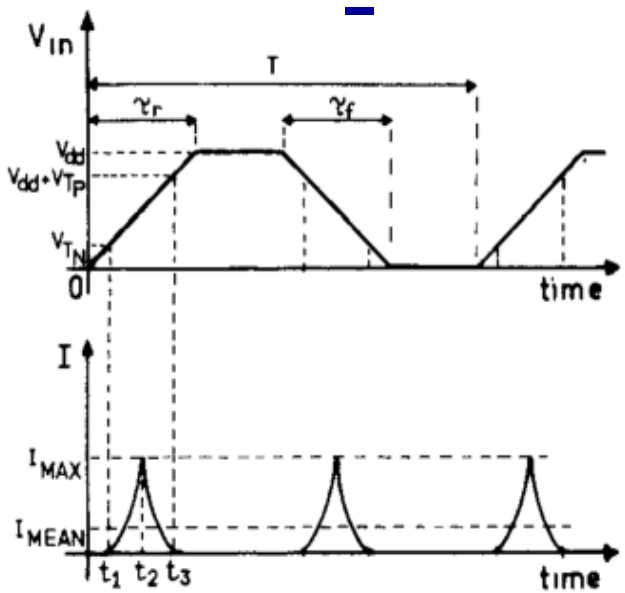
$= 3/4 \times 1/4 = 3/16$

Courtesy of B. Nikolic (UC Berkeley)

Short-Circuit Energy

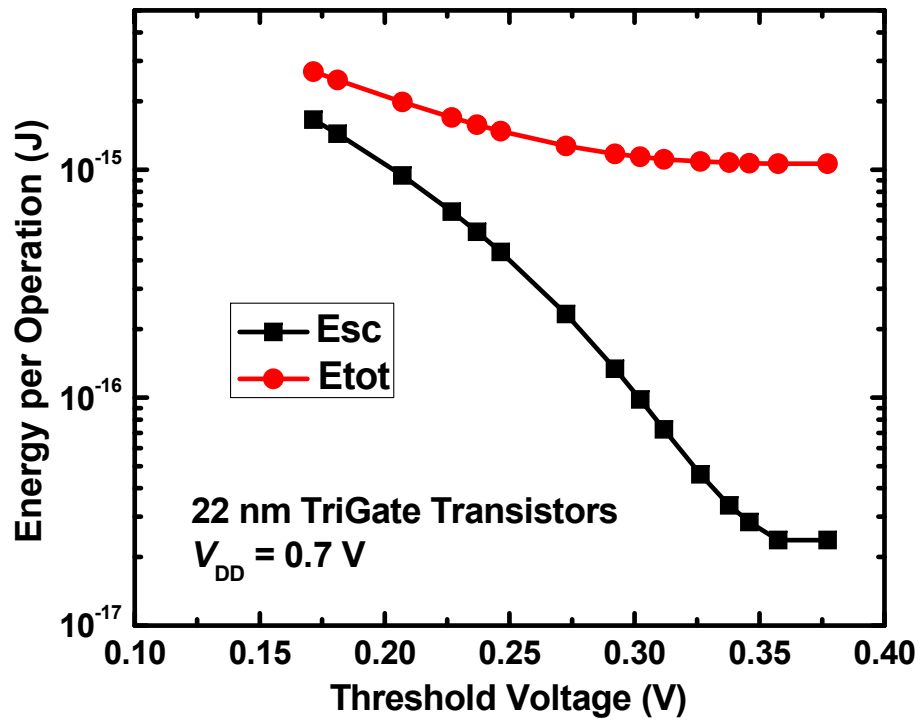
CMOS inverter:





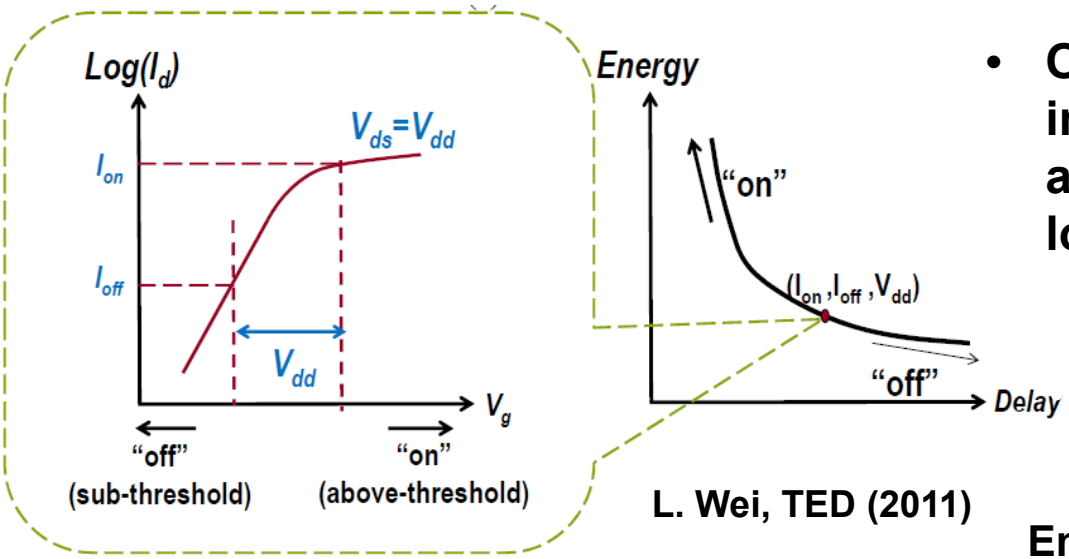
H.J.M. Veendrick, JSSC (1984)

Impact of V_{TH} on CMOS short-circuit energy



- Short circuit energy can be mitigated by adjusting $|V_{T,P}| + |V_{T,N}| > V_{DD}$

Energy *vs*. Delay Plots

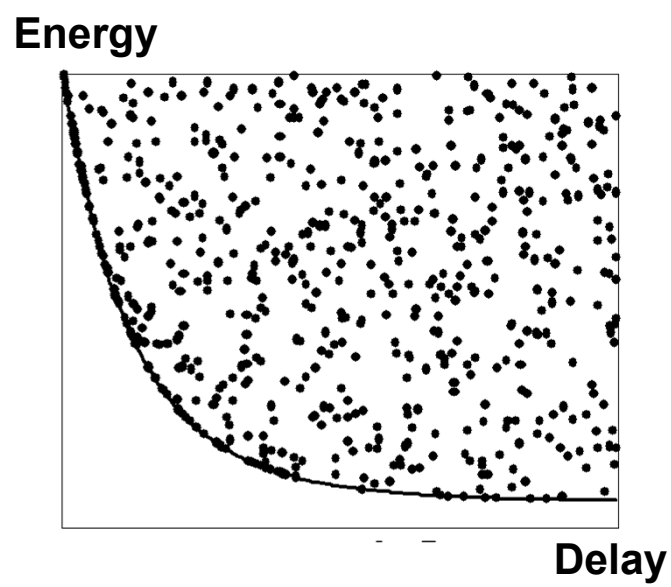


L. Wei, TED (2011)

- **Obviously, there exists the inherent trade-off between energy and delay (1 / performance) in logic circuits:**

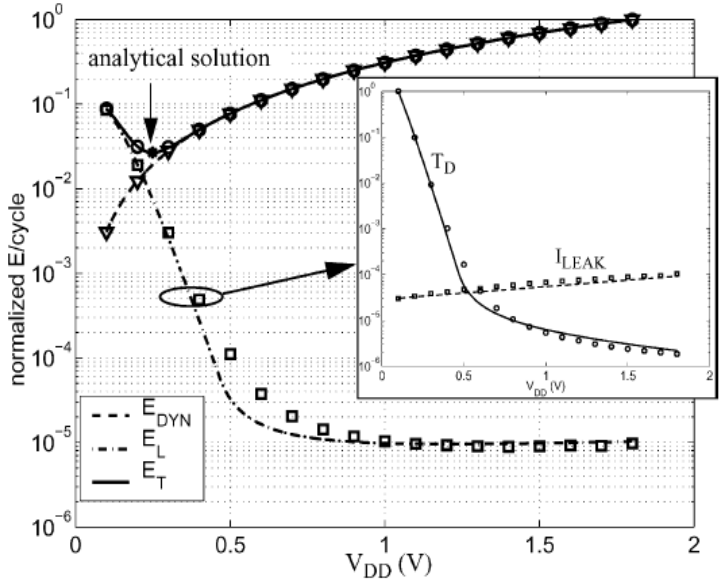
$$t_{delay} = LD \cdot F \cdot CV_{DD}/(2I_{EFF})$$

$$E_{dyn} + E_{leak} = \alpha \cdot LD \cdot F \cdot CV_{DD}^2 + LD \cdot F \cdot I_{OFF} V_{DD} t_{delay}$$



- **Optimizations needed for:**
  - V_{DD}
  - I_{ON}, I_{OFF} or I_{ON}/I_{OFF} ?
  - Transistor sizing
  - Logic structure (*LD*, *α*, *F*)
  - System architecture

Optimal V_{DD} and I_{ON}/I_{OFF}



Total energy of a logic chain:

$$E = E_{\text{dyn}} + E_{\text{leak}} = aL_dFCV_{\text{dd}}^2 + L_dFI_{\text{off}}V_{\text{dd}}t_{\text{delay}}$$

Derive *E vs.* V_{DD}, to find the minimum *E*:

$$\frac{\partial E}{\partial V_{DD}} = 2\alpha \cdot LD \cdot F \cdot CV_{DD} + 2LD \cdot F \cdot CV_{DD} e^{\frac{-V_{DD}}{m\frac{kT}{q}}} - \frac{LD \cdot F \cdot CV_{DD}{}^2}{m\,kT/q} e^{\frac{-V_{DD}}{m\frac{kT}{q}}} = 0$$

$$\rightarrow V_{DD,opt} = \mathrm{m} \cdot {}^{kT}/_{q}\left(2 - lambertW\left(\frac{-4\alpha}{LD \cdot F}e^2\right)\right)$$

- **Note that the optimal V_{DD} occurs at MOSFET sub-threshold region.**

B.H. Calhoun, JSSC (2005)

Derive *E vs.* V_{DD}, at a fixed t_{delay}

$$\frac{I_{\text{on}}}{I_{\text{off}}} = -\gamma\frac{L_dF}{4a}\frac{S_{\text{eff}}}{S_{\text{off}}}lambertW\left(-\frac{4a}{\gamma L_dF}\frac{S_{\text{off}}}{S_{\text{eff}}}\exp\left(\frac{S_{\text{off}}+S_{\text{on}}}{S_{\text{eff}}}\right)\right)$$
$$= -\gamma\frac{L_dF}{4a}lambertW\left(-\frac{4a}{L_dF\gamma}e^2\right) \approx 2.02\frac{L_dF}{a}$$

The E_{dyn}/E_{leak} under optimum I_{ON}/I_{OFF}:

$$\frac{E_{\text{dyn}}}{E_{\text{leak}}} = \frac{a}{\gamma L_dF}\frac{2I_{\text{on}}}{I_{\text{off}}} = \frac{\beta}{2} \approx 4.04$$ **(for a MOSFET)**

- **Pick V_{DD}, V_{TH} to minimize energy for given performance (1/delay)**
  - **Assuming work function (V_{TH}) can be freely tuned**
- **Result: optimal $I_{ON}/I_{OFF} \propto LD \cdot F / \alpha$**

H. Kam, TED (2012)

Application Oriented Energy Optimization

α: Carrier saturation index	U_T: Thermal voltage
n: Subthreshold swing parameter	η: DIBL coefficient
a: Activity factor	ξ: Active time ratio

$$I_{ON} \propto \begin{cases} e^{\left(\frac{(1+\eta)V_{DD}-V_{TH}}{nU_T}\right)} & (V_{DD} < V_{TH}) \\ ((1+\eta)V_{DD} - V_{TH})^{\alpha} & (V_{DD} > V_{TH}) \end{cases}$$

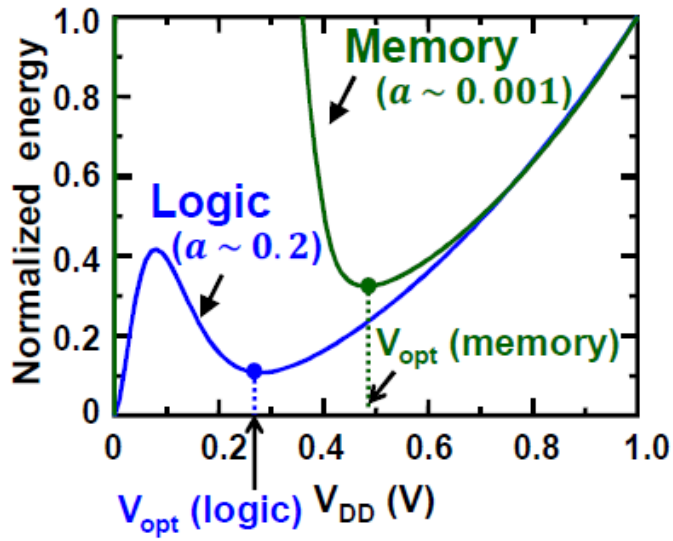
$$I_{OFF} \propto e^{\left(\frac{\eta V_{DD}-V_{TH}}{nU_T}\right)}$$

$$P \propto \underbrace{\xi I_{ON} V_{DD}}_{\text{Dynamic power}} + \underbrace{I_{OFF} V_{DD}}_{\text{Leakage power}}$$

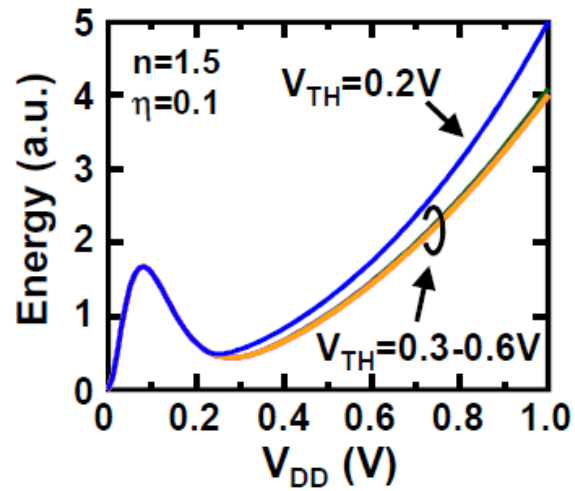
$$D \propto V_{DD} / I_{ON}$$

Simplified energy model

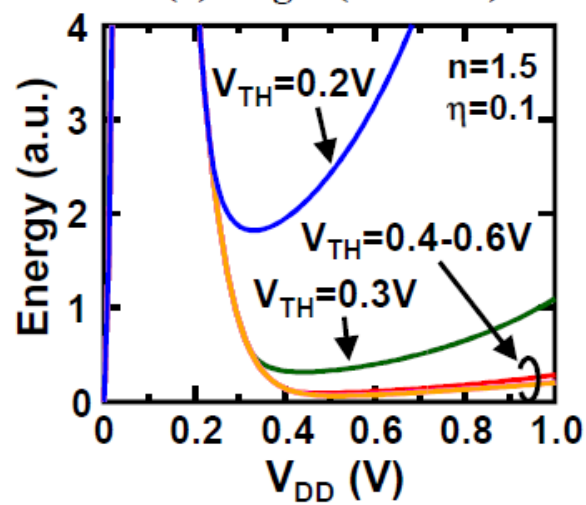
$$E = P \cdot D$$
$$\propto V_{DD}^{\ 2}(\xi + I_{OFF}/I_{ON})$$
$$\xi \propto a$$



H. Fuketa, IEDM (2012)



(a) Logic ($a \sim 0.2$)



(b) Memory ($a \sim 0.001$)

Energy *vs*. Delay Optimizations: To Probe Further

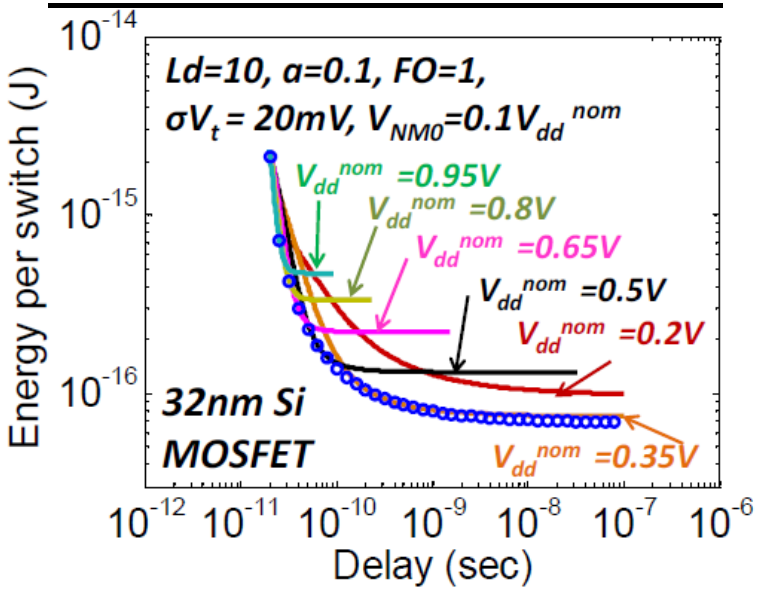
Designs

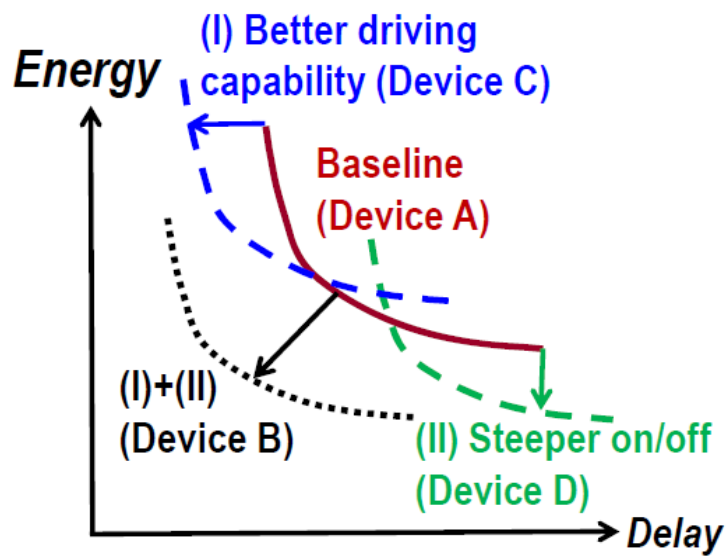
- Downsizing transistors (↓ C_L)
- Reducing clock frequency (↓ f_{clk})
  - ➢ lowers the performance
- Reducing activity factor
  - ➢ requires logic restructuring

Technology

- Increasing threshold (↑ V_{TH})
- Lowering the supply voltage (↓ V_{DD})
  - ➢ Lowers the performance
- Improving electrostatics + mobility
- Reducing parasites

Pareto Curve of minimum *E vs. D*

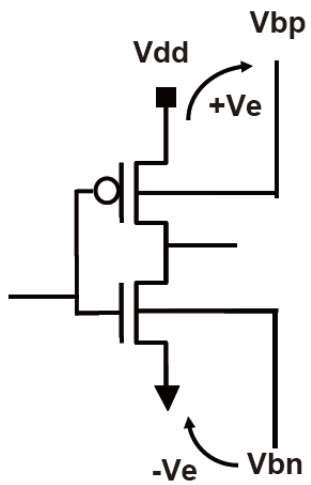




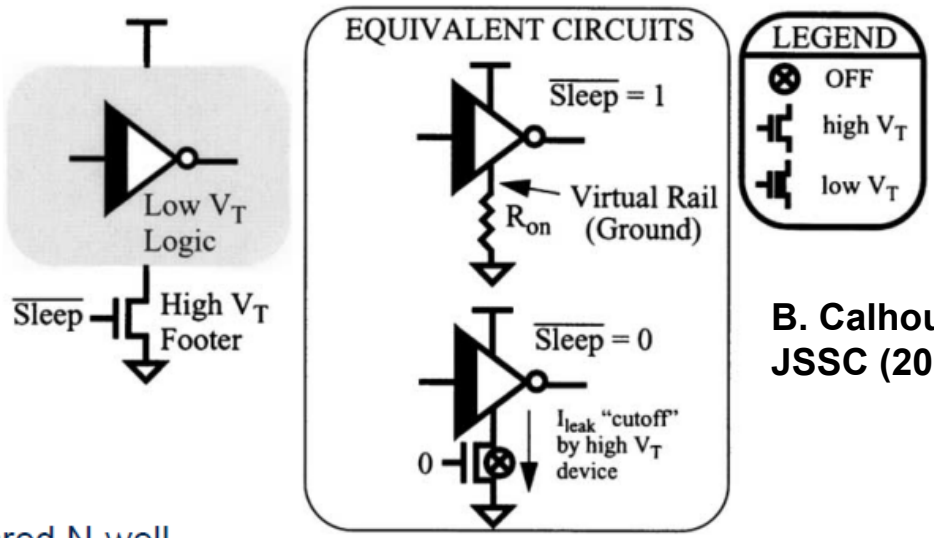
L. Wei, TED (2011)

Power Gating Techniques

Dynamic V_{TH} Tuning

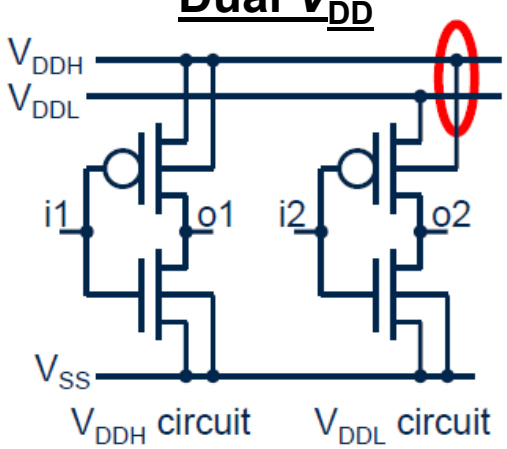


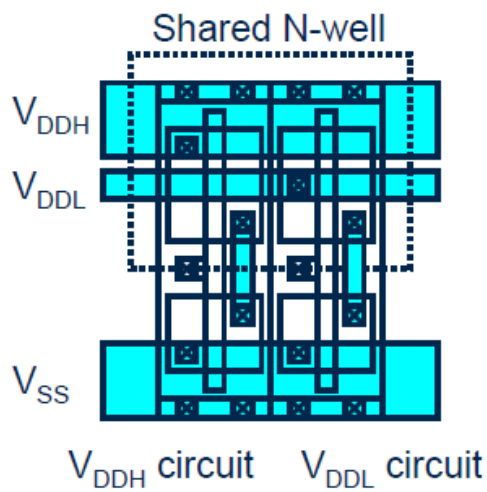
Sleep Transistors

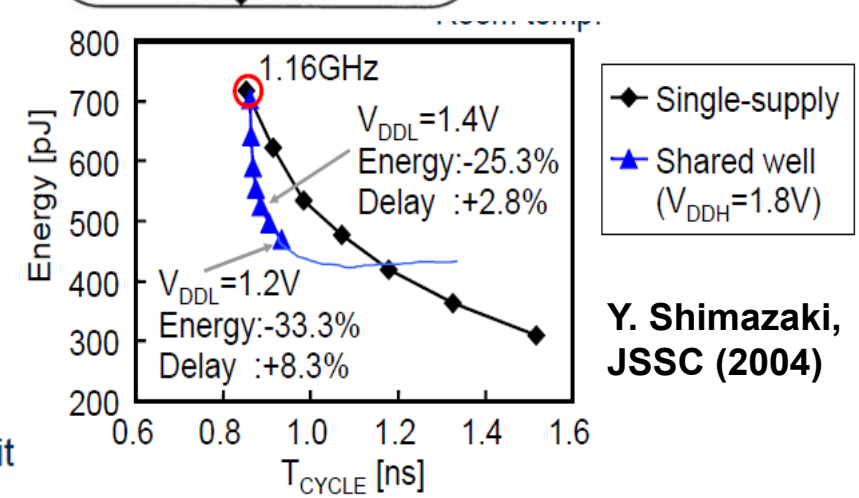


B. Calhoun, JSSC (2004)

Dual V_{DD}



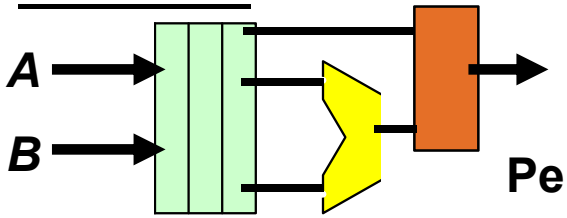




Y. Shimazaki, JSSC (2004)

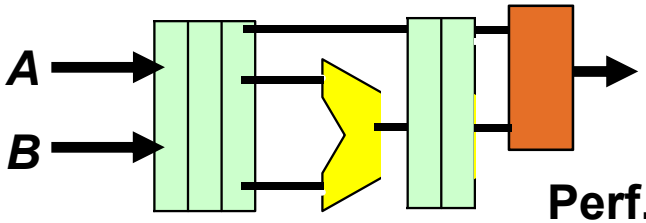
Micro-Architectural Design

Reference



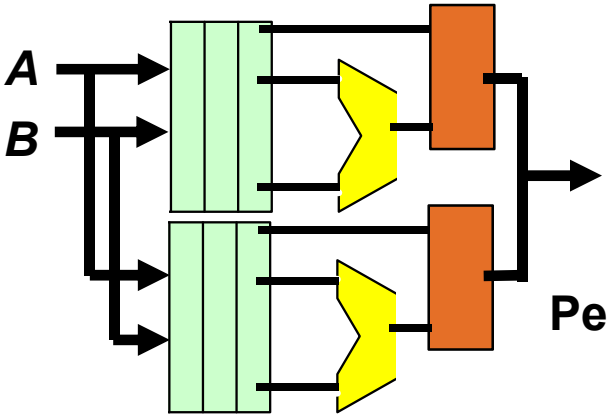
Perf. ∝ f_{clk}, E/op ~ 1 unit

Pipeline

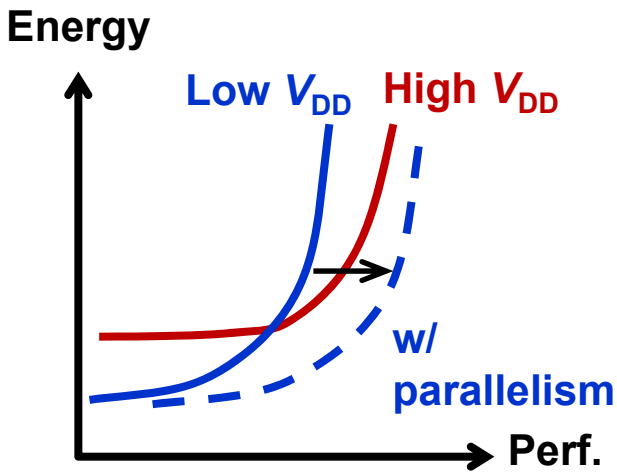


Perf. ∝ f_{clk}, E/op ~ 0.5 unit

Parallelism

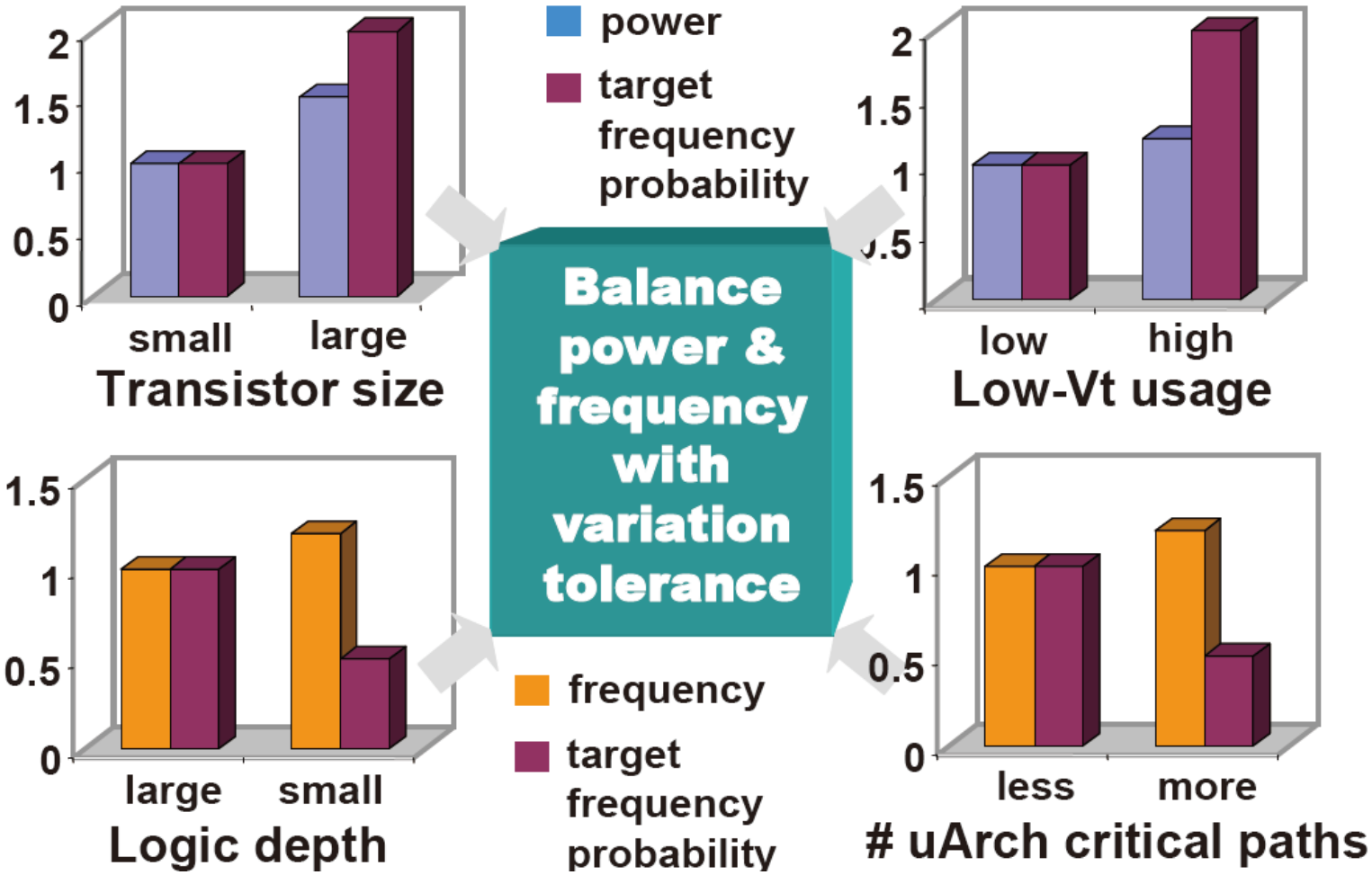


Perf. ∝ f_{clk}, E/op ~ 0.5 unit



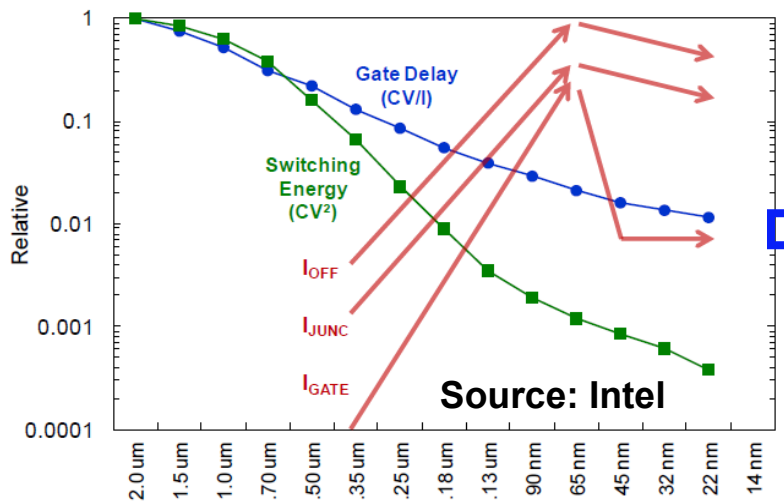
- Parallelism allow transistors operate at slower speed while maintains the same throughput per frequency.

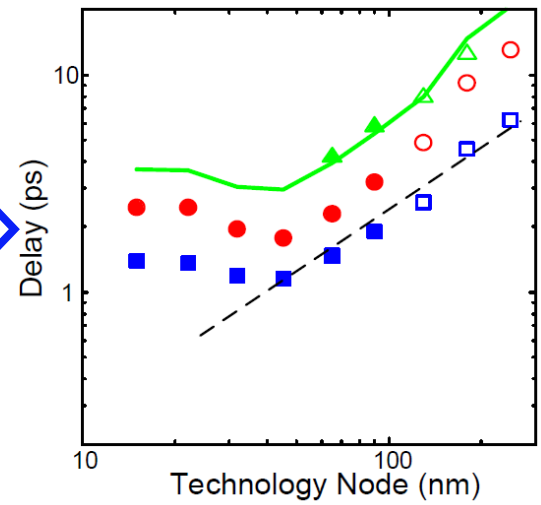
Digital Circuit Design Trade-offs

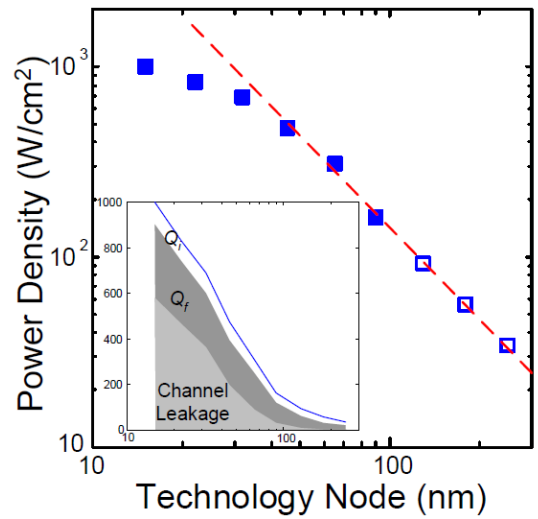


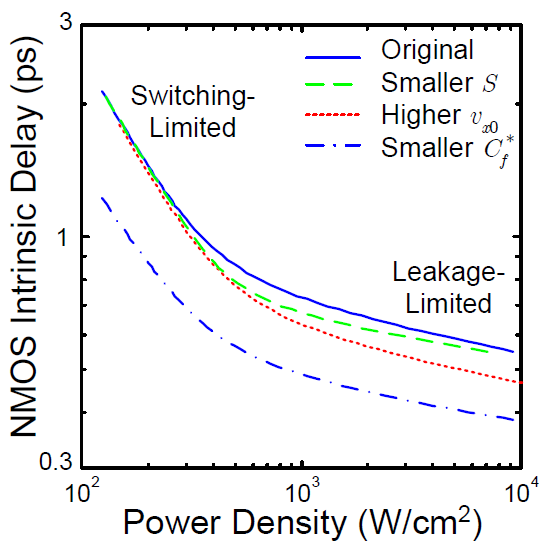
S. Borkar, VLSI-T short course (2007)

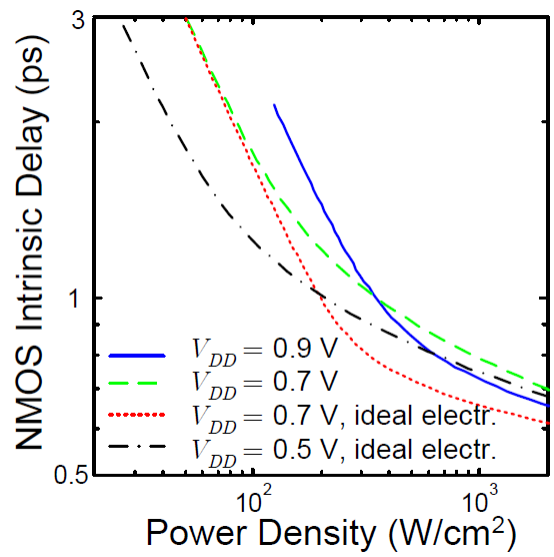
Impact of Technology Scaling











In a power-limited technology:

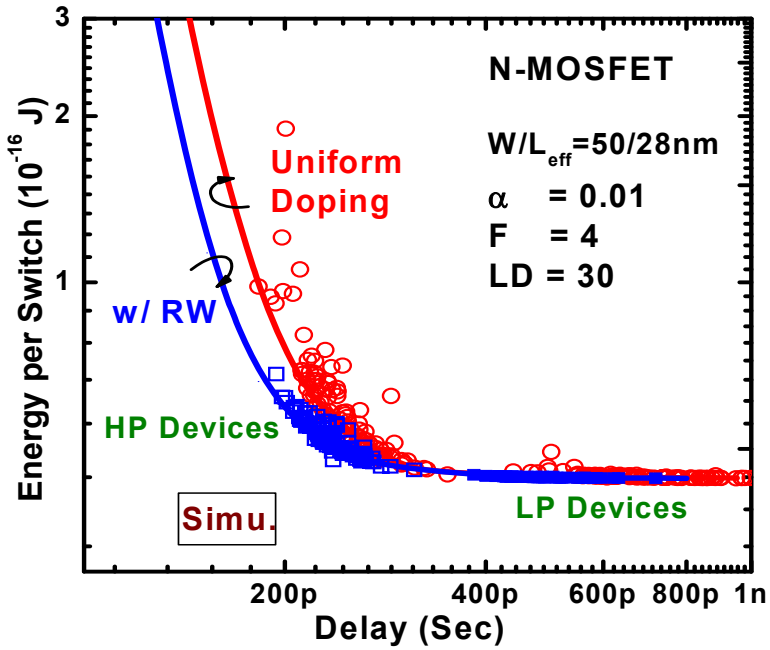
- **Parasites reduction seems the most important among all solutions (*i.e.* SS↓, μ↑)**
- **V_{DD} scaling will be helpful only for devices with good electrostatics.**

A. Khakifirooz, IEDM (2008)

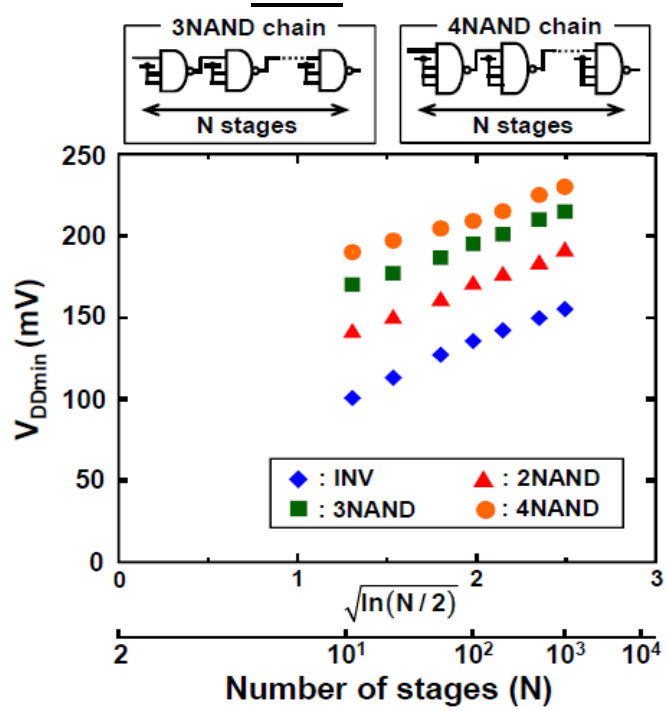
Impact of Variability

- Device variability hurts in two ways
  1. Reduces effective I_{EFF} (delay set by worst-case)
  2. Increase effective I_{OFF} (leaky devices dominate)
     - ➢ Forces increase in nominal I_{ON}/I_{OFF} and V_{DDmin} …

Energy *vs*. Delay plots under RDF



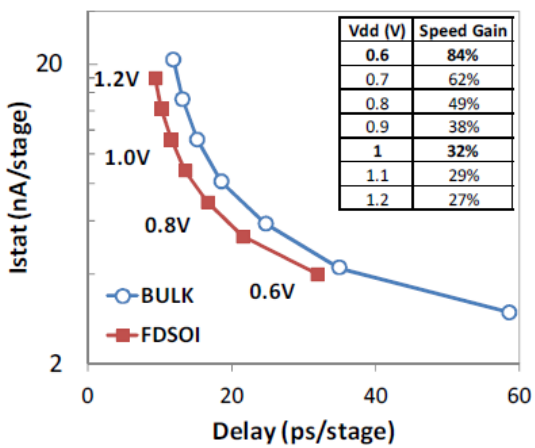
Logic V_{DDmin} *vs*. logic depth



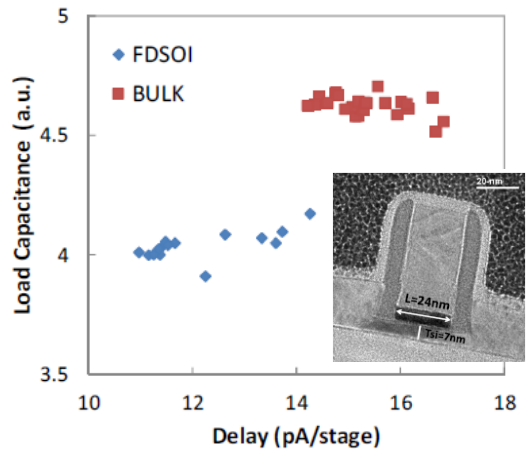
H. Fuketa, IEDM (2012)

Advancement of Thin-Body MOSFETs

UTBB FD-SOI @ 28 nm

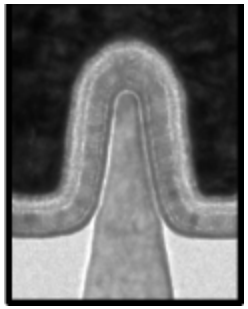


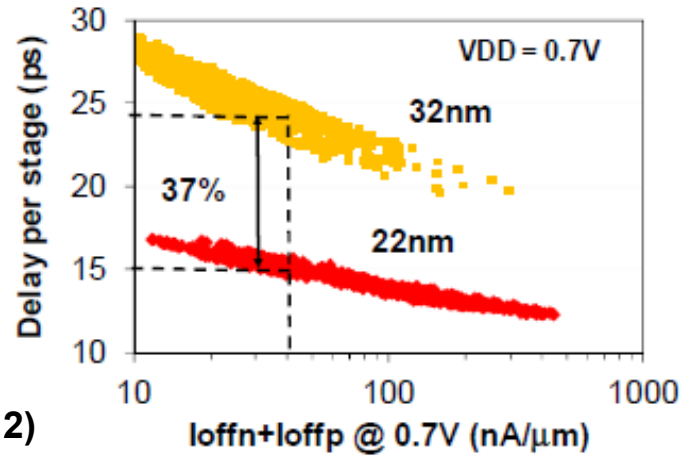
Vdd (V)	Speed Gain
0.6	84%
0.7	62%
0.8	49%
0.9	38%
1	32%
1.1	29%
1.2	27%



N. Planes, VLSI (2012)

TriGate @ 22 nm

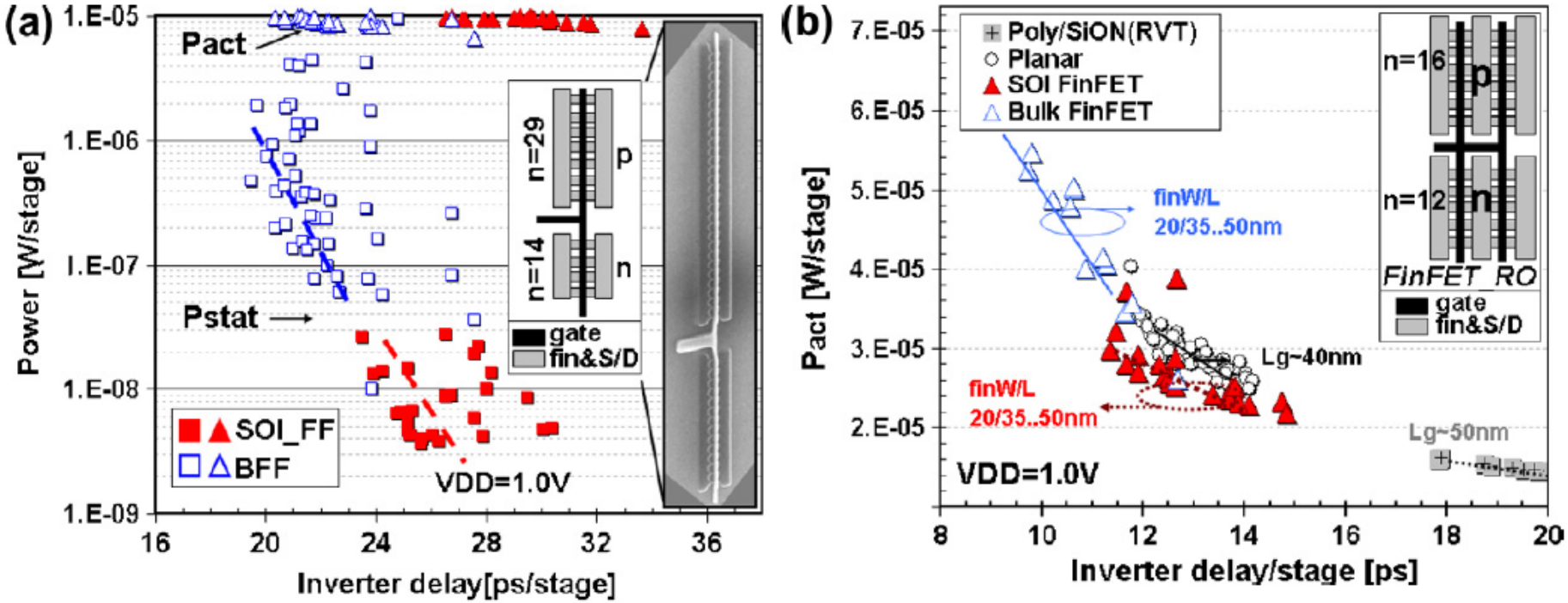




K. Kuhn, IEDM (2012)

- **Benefits of thin-body MOSFETs:**
  - **Improved I_{ON}/I_{OFF} from higher mobility and better electrostatics**
  - **Improved variability**
- **However, parasites reduction are still challenging.**
  - **SOI substrate will be extremely helpful in this regime**

Bulk *vs*. SOI FinFETs: Inverter Benchmark



T. Chiarella, SSE (2010)

- SOI FinFET fits better for low-power corner while bulk FinFET for the high-performance one.
- A balanced P/N design will benefit for bulk FinFET further.

References

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