Lecture 12

• Process-induced Variations II: Systematic
  – Lithographic Proximity Effect
  – Layout Dependent Strain
  – Well Proximity Effect

Reading: multiple research articles (reference list at the end of this lecture)
Lithography Proximity Effect (LPE)

<table>
<thead>
<tr>
<th>Design</th>
<th>Mask</th>
<th>Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>250nm</td>
<td>OPC</td>
<td>0°</td>
</tr>
<tr>
<td>180nm</td>
<td>PSM</td>
<td>90°</td>
</tr>
<tr>
<td>90nm and Below</td>
<td>OPC</td>
<td>180°</td>
</tr>
</tbody>
</table>

- Optical Proximity Correction (OPC) used to compensate for image errors due to diffraction effects by adding extra polygons to the pattern on the photomask
- Phase Shift Mask (PSM) used to reduce the light interference by changing the thickness of transmitting patterns on the photomask (i.e. creating a phase shift light)

Desired 6T SRAM Layout

- Nominal
- Underexposed
- Overexposed

Actual Layout

These resolution enhancement techniques help to reduce the pattern distortions, yet still end with round corners.
Impact of Poly Corner Rounding: Gate-Extension Dependence

- Threshold voltage
  - SCE
  - RSCE
  - DIBL
- Average channel length increasing.

- $I_{on}/I_{off}$ performance
  - [Rectangle poly]
  - [Non-rectangular poly]
  - +10%

Poly corner rounding can be improved by using multiple patterning/exposure techniques.

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1st Gate Patterning
2nd Gate Patterning

M. Choi, SPIE (2009)
Impact of Active Region Rounding: Asymmetric Source/Drain

- Large source structure provides better performance
  - 10% Ion gain or 3xloff reduction
- Large drain structure degrades performance
  - 50% Ion degradation or 3xloff leakage

M. Choi, SPIE (2009)
Due to the different thermal expansion coefficients between Si and STI, there exists biaxial compressive residual stress in the active region after processing.

STI-stress generally increases PMOS current and decreases NMOS current.

Stress relaxes exponentially with increased distance from Si/STI boundary.

R. A. Bianchi, IEDM (2002)
Layout Dependent Strain: eSiGe Source/Drain

Isolated PMOS

Nested PMOS

Comparison of Stress

V. Moroz, SISPAD (2008)
Other Sources for Layout Dependent Strain

sCESL-induced Strain
N. Xu, TDMR (2011)

sCESL

Contact-induced Strain

(a) Stress change near contact
(b) The effect of neighboring gates

PMOS

% Change in RO Frequency

45nm RO Test Structure with CESL

Conventional Model
Injection Velocity Model
Experimental Data

11/6/2013
Nuo Xu EE 290D, Fall 2013
During ion implantation, kinetic ions scatter back out of PR and become embedded in the Si near PR edge, causing $V_{TH}$ shift.

- The affected distance is ~ 1um.
- Small angle II helps, but never avoids WPE.
Another WPE: Stress-induced Enhanced/Retarded Diffusion


<table>
<thead>
<tr>
<th>Layout parameters</th>
<th>NFET</th>
<th>PFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>shrinkage</td>
<td>B</td>
<td>As</td>
</tr>
<tr>
<td>Gate-STI</td>
<td>-9%</td>
<td>-17%</td>
</tr>
<tr>
<td>Gate space</td>
<td>1%</td>
<td>1%</td>
</tr>
<tr>
<td>STI width</td>
<td>4%</td>
<td>8%</td>
</tr>
</tbody>
</table>

N-MOSFET $V_{TH}$ Shift vs. Inverse of ($l$) STI-Gate Distance and ($r$)Gate Spacing

Inversion of gate-STS distance [1/um] vs. $\Delta V_{TH}$ sat [mV]

Courses: EE 290D, Fall 2013
Design for Manufacturability (DFM)

Carrier Mobility

\[ \mu = \frac{\mu_{\text{ref}}}{1 + K \mu \left( \frac{1}{SA + L/2} + \frac{1}{SB + L/2} \right)} \]

Threshold Voltage

\[ V_{TO} = V_{TO_{\text{ref}}} + K_V \left( \frac{1}{SA + L/2} + \frac{1}{SB + L/2} - \frac{1}{SA_{\text{ref}} + L/2} - \frac{1}{SB_{\text{ref}} + L/2} \right) \]

where \[ K_V = \frac{K_{VTO}}{1 + \frac{L_{KTO}}{L_{KTO_{\text{ref}}}} + \frac{W_{KTO}}{W_{KTO_{\text{ref}}}} + \frac{P_{KTO}}{P_{KTO_{\text{ref}}}}} \]

- Compact modeling is the best solution to leverage between the accuracy and design complexity.
Monitors for Systematic Variability

Defocus and LPE

Vertial STIS & WPE

Multi-Level CESL Strain

S/D Asymmetry

45nm Si Test Chip

Ring oscillators (RO) and OFF-state transistors are often used to characterize transistors’ performance and leakage.

L. Wang & N. Xu, CICC (2010)
Summary of Systematic Variability on Planar Bulk MOSFETs

- Layout-dependent strain and WPE play the dominant role on transistor performance’s drift.

- Small active-region area cells suffer more from systematic variability.

<table>
<thead>
<tr>
<th>Layout Variation</th>
<th>Typical $I_{on}$ variation range</th>
<th>Typical $V_{th}$ variation range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length of diffusion (LOD) (SiGe or STI)</td>
<td>~30%</td>
<td>~50mV</td>
</tr>
<tr>
<td>Spacing to adjacent diffusion</td>
<td>~5%</td>
<td>~15mV</td>
</tr>
<tr>
<td>Active diffusion corners</td>
<td>~5%</td>
<td>~15mV</td>
</tr>
<tr>
<td>Poly spacing</td>
<td>~15%</td>
<td>~30mV</td>
</tr>
<tr>
<td>Poly corner rounding</td>
<td>~5%</td>
<td>~20mV</td>
</tr>
<tr>
<td>Well boundary (WPE)/ Dual stress liner (DSL)</td>
<td>~15%</td>
<td>~90mV</td>
</tr>
<tr>
<td>Contact to gate distance</td>
<td>~3%</td>
<td>~10mV</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>delay(ps)</th>
<th>leakage power(nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>25C/1.0V</td>
<td>no well proximity model</td>
</tr>
<tr>
<td></td>
<td>value</td>
<td>ratio</td>
</tr>
</tbody>
</table>

- Standard logic circuit performance shift w/ WPE

Y.-M. Sheu, CICC (2005)

- Layout-dependent strain and WPE play the dominant role on transistor performance’s drift.
Impact of Layout Dependent Strain on FinFETs

- Topologies of nested and isolated FinFET are unavoidable.
- Mobility of nested FinFET will be enhanced by ~80%.
- Stress of isolated FinFET is almost relaxed.

M. Choi, ISTDM (2012)
Strained FinFET Inverter Performance

• PMOS stress (induced by eSiGe) boosts with fin length and # of gates per fin and degrades with increasing fin pitch.
• NMOS stress (induced by tensile STI) boosts with increasing fin pitch, and degrades with increasing # of gates per fin.
• For a CMOS inverter, the best configuration comes from a multiple-gate yet moderate fin-pitch design.

M. G. Bardon, VLSI-T (2013)
References