UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 290D Advanced Topics in Semiconductor Technology — Fall 2013
- *Three-Dimensional Transistor Technologies* — Dr. Xu

Homework #1 Semiconductor Device Physics

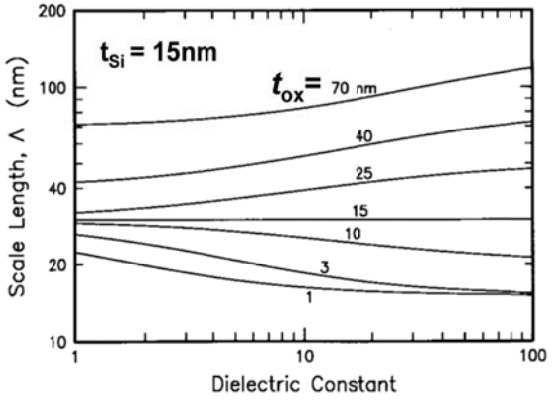
Problem 1 MOSFET Electrostatics

1) In a planar bulk MOSFET, substrate biasing can be used as a knob to tune threshold voltage. Substrate is always reverse biased, to suppress the leakage current (through Source/Drain and substrate PN junctions). Under substrate biasing, how does SS, DIBL and I_{OFF} *vs*. I_{EFF} plots change, compared to the zero biasing case (substrate is grounded)?

2) High-κ Will be Harmful? – In some cases…

a) In a planar UTBB MOSFET, thin BOX region helps to relax the Si body thickness scaling requirement, to maintain a decent electrostatic integrity. Think about if the BOX region is made of Al_2O_3 instead of conventional SiO_2, discuss qualitatively how the SS and DIBL change, for both long-channel and short-channel MOSFETs. (Hint: think about the fringe electric field effect through BOX)

b) This part extends the above discussion further, to reveal that the role of high-κ in MOSFET electrostatics is not a simple EOT problem. The figure below is a simulation results from a Si UTB MOSFET (with t_{Si} = 15 nm and thick BOX) showing scale length (Λ) *vs*. dielectric constant (ε_r) of top gate oxide, under a wide range of oxide thickness (t_{ox}). Results show, interestingly, at thin t_{ox} region, one can see a reduction of Λ *vs*. ε_r. However at thick t_{ox} region, Λ increases with ε_r. Can you explain this? (data source: D.J. Frank *et al*., IEEE EDL, 1998)



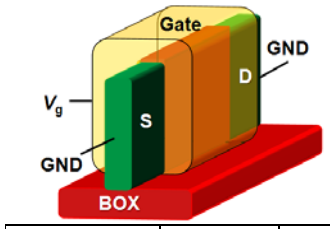
3) Why high-level channel doping is no longer required in thin-body MOSFETs?

4) Given the lithography constraints (*i.e*. assuming the minimum pattern size by lithography is fixed), explain succinctly why an aspect-ratio of 1:1 multiple-gate MOSFET is not preferred in both high-performance and low-power applications? (Hint: think about the scale length and layout efficiency)

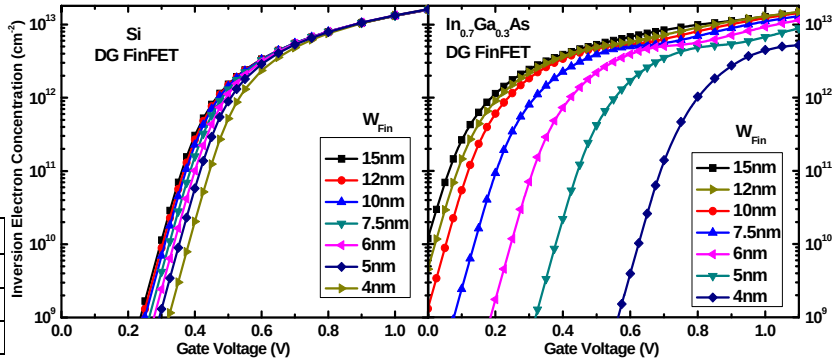
Problem 2 Bandstructure and Quantum Confinement

1) With the Si conduction band model introduced in Lec.4, how does the overall electron's transport effective mass ($m_{//}^*$, *i.e*. m^* along current direction) change with increasing gate voltage (V_g), for (100) and (110) wafers, and for both planar bulk MOSFETs and FinFETs?

2) Your friend has been educated by his professor for a long time that III-V compounds (*e.g*. $In_{0.7}Ga_{0.3}As$) would be the ultimate channel material used for digital MOSFETs, simply due to their high mobility feature. However, one day he came to you to show some of his measured N_{inv} *vs*. V_g curves (shown below) from Si (as a control device) and $In_{0.7}Ga_{0.3}As$ Fin-shape capacitors with exactly same dimensions (T_{ox}, W_{Fin} and H_{Fin}). He saw some weird results and felt frustrated.



	Si	$In_{0.7}Ga_{0.3}As$
Dielectric Constant	11.7	14.3
Ave. Effective Mass	$0.42m_0$	$0.0344m_0$
Effective DOS (N_c)	3.2e19 cm^{-3}	1.6e17 cm^{-3}



Based on your knowledge and the parameters in the table above, can you help him to address:

a) Generally, with the same gate length (L_g), to achieve the same electrostatic integrity, $In_{0.7}Ga_{0.3}As$ FinFETs require smaller W_{Fin} than Si FinFETs, why? Assuming at 10 nm node, digital devices use L_g = 14 nm, EOT = 0.9 nm, to achieve DIBL < 80 mV/V, what is the required W_{Fin} for Si and $In_{0.7}Ga_{0.3}As$ FinFETs?

b) Why by changing W_{Fin}, there appears a shift of the N_{inv} *vs.* V_g curve? What does this variation correspond to in a MOSFET performance metrics? Why as W_{Fin} shrinks, the shift becomes larger (per W_{Fin} reduction)?

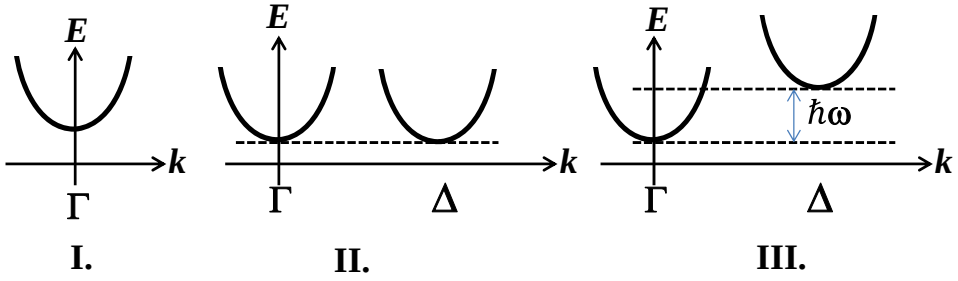
c) Why with the same range of W_{Fin} change, $In_{0.7}Ga_{0.3}As$ FinFETs show more variations than Si FinFETs?

d) Why there exist kinks at high V_g for $In_{0.7}Ga_{0.3}As$ FinFETs?

e) Regarding the quantum capacitance model introduced in Lec.4, draw qualitatively the gate capacitance *vs.* gate voltage (C_g *vs.* V_g) curves for Si and $In_{0.7}Ga_{0.3}As$ FinFETs. Identify all the possible differences.

Problem 3 Scatterings and Carrier Mobility

1) Your friend at material science department has recently synthesized three types of compound semiconductors, with their conduction bands (*E vs. k*) illustrated as below:



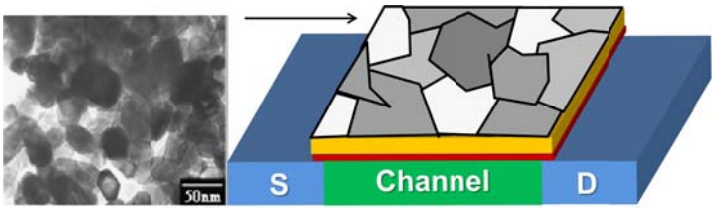
Assuming all valleys have the same effective mass (m^*) value and parabolic shape and are exactly isotropic, can you tell your friend which material has the highest electron mobility and which one has the lowest? (Hint: think about the impacts of scattering types on scattering rates)

2) Universal mobility curve.

a) Explain succinctly why universal mobility curve can make the carrier mobility curves "overlapped" at moderate and high *E*-field regions, regardless of the channel doping concentration? And why it won't be that universal at low *E*-field region? (Hint: think separately about the different scattering mechanisms)

b) What does the coefficient before Q_{inv} in E_{eff} formula depend on? Use pictures to briefly illustrate.

3) Metal Gate Granularity (MGG)-induced scatterings have been considered as the becoming important scattering mechanisms in recent CMOS technology nodes, whose principles are similar to surface roughness (SR)-induced scatterings. Think about a metal gate used in a MOSFET device, due to the post-metallization annealing can result in crystallization of the metal, it always consists of different crystallographic orientations with different workfunctions seen by the channel, as shown below. When carriers are traveling along the channel, they actually feel the MGG scattering potentials.



a) Is this scattering elastic or inelastic? Explain your reasons. (Hint: think about SR scattering mechanism)

b) Do you expect MGG scatterings to be more severe at high E_{eff} or low E_{eff}? Why? (Hint: think about the impact of workfunction fluctuations on E-field as the dependence of N_{inv})

c) With this respect, would you adopt a Gate-First or a Gate-Last approach to your high-performance MOSFET? Why?