PROBLEM SET #2

Issued: Tuesday, Feb. 11, 2014

Due (at 9 a.m.): Friday, Feb. 21, 2014, in the EE C247B HW box near 125 Cory.

1. You are given a wafer with the cross-section shown in Figure PS2.1-1 and intend to release etch the structure, i.e., to leave only the polysilicon structure atop the blanket nitride/oxide layer. To perform the release, you need to do the following steps:

i. Etch polysilicon via RIE and stop on the sacrificial oxide layer (The etch rate and selectivity of the polysilicon etch are given in Table2.1-1).

ii. Remove photoresist (PR).

iii. Dip the wafer in HF to etch the sacrificial oxide until polysilicon structures are fully released. (Assume this wet etch is completely isotropic with characteristics given in Table 2.1-2.)

Due to topography across the wafer, a given layer thickness might not be the same over the entire wafer. So when you etch a given layer, you must etch a bit longer than what you calculate from knowledge of thickness and etch rate to make sure all material is removed from unmasked areas. It is common practice to etch for at least 20% longer than the calculated time (i.e., to do a 20% overetch). Include this overetch in your calculations for this problem.

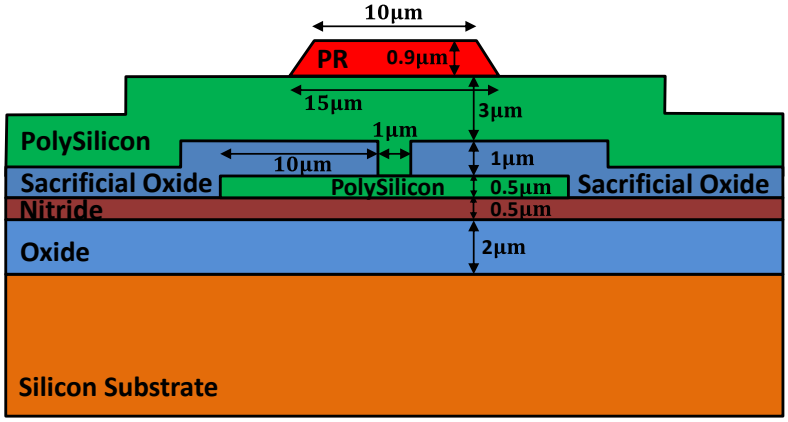

Fig. PS2.1-1

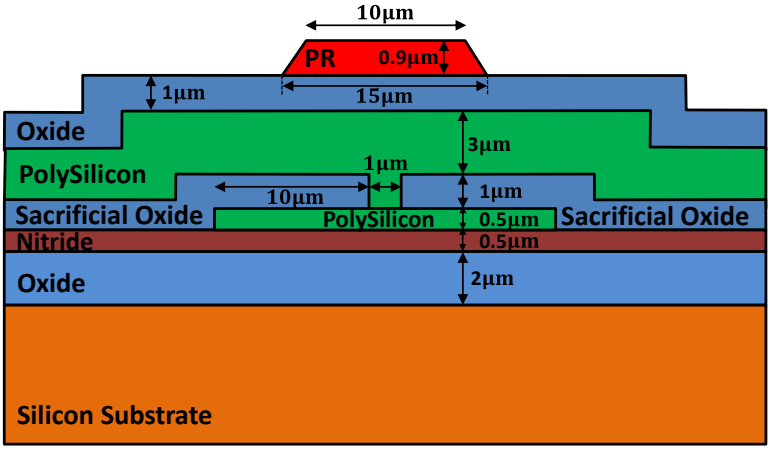

Fig. PS2.1-2

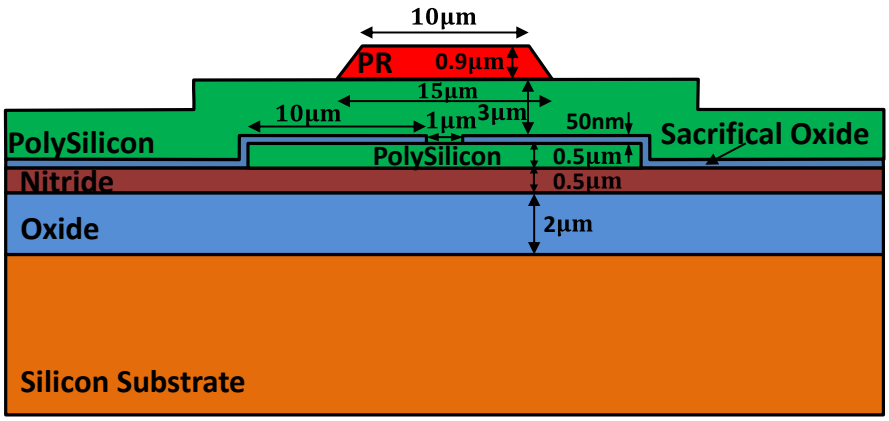

Fig. PS2.1-3

Table 2.1-1

Polysilicon etch rate	0.5 µm/min
Selectivity over Oxide	5:1
Selectivity over Nitride	10:1
Selectivity over Photoresist	2:1

Table 2.1-2

Oxide wet etch rate	0.3 µm/min
Selectivity over polysilicon	100:1
Selectivity over Nitride	20:1
Selectivity over Photoresist	5:1

Table 2.1-3

Oxide dry etch rate	0.3 µm/min
Selectivity over polysilicon	14:1
Selectivity over Photoresist	4:1

Table 2.1-4

Polysilicon DRIE etch rate	1.5 µm/min
Selectivity over oxide	100:1
Selectivity over Photoresist	50:1

(a) How long should you etch (including the 20% overetch) to remove all the unprotected polysilicon? Draw the wafer cross-section immediately after the polysilicon etch step. You can assume the RIE etch is completely anisotropic.

(b) Suppose a 1μm oxide hard mask layer is deposited atop the polysilicon film before photo-resist deposition and patterning, as shown in Fig. PS2.1-2. You first dry etch the oxide in an RIE system with etch rate and selectivity given in Table 2.1-3. You follow with an RIE etch as in Table 2.1-1 to define the polysilicon structure using the patterned oxide layer as a hard mask. How long should you dry etch the oxide layer (including a 20% overetch)? Draw the wafer cross-sections immediately after the oxide etch step and after the polysilicon etch step. (To make sure you are not affected by the results you calculated in part (b), assume an 8 min polysilicon etch after etching the oxide.)

(c) After the polysilicon etch step in part (b), you release the structure in HF, as indicated in step iii of the process flow. How long does it take to completely release the structure? Draw the wafer cross-section immediately after the release step. Assume the wet etch is completely isotropic.

(d) Assume now the sacrificial oxide layer thickness is reduced to only 50nm, as shown in Fig. 2.1-3. To avoid etching through the sacrificial oxide to the polysilicon underneath, you now choose the high-selectivity BOSCH DRIE process with etch rate and selectivity given in Table 2.1-4. How long should you etch the polysilicon layer now (including the 20% overetch)? Is 50nm oxide thick enough to protect the polysilicon below? How long does it take to completely release the structure with 50nm thick sacrificial oxide?

(e) What are the drawbacks of the BOSCH DRIE process?

2. Figure PS2.2-1 presents a 2μm-thick polysilicon film atop a 2μm-thick sacrificial oxide film. The polysilicon beam is initially uniformly doped with phosphorous to a concentration $N_D = 1 \times 10^{15}\text{cm}^{-3}$. Suppose you want to make the beam more conductive by diffusing boron atoms into the n-type polysilicon material. To do so, you first place the wafer into a pre-deposition furnace alongside solid-source boron wafers for 30min at 1000°C. You then drive in the dopants (with no boron source) for 60min at the same temperature.

[Assume for this problem that the diffusion coefficient D_o of poly-silicon is 10 times larger than that of single crystal silicon (SCS). Also, assume that the solid-solubility limit and electrically active concentration limits, as well as carrier mobility of polysilicon, are the same as SCS. Some of this isn't actually entirely true, but it makes the problem more tractable.]

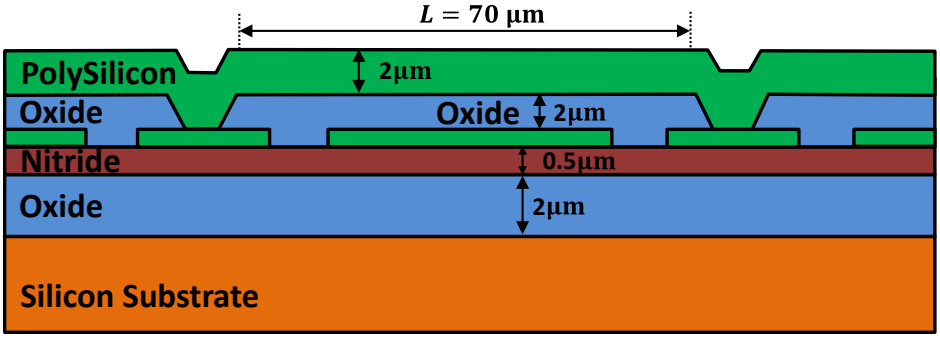

Fig. PS2.2-1

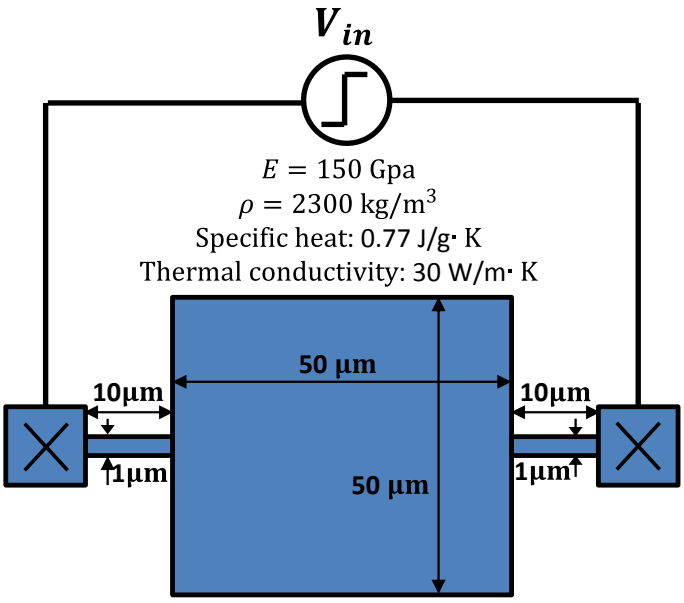

Fig. PS2.2-2

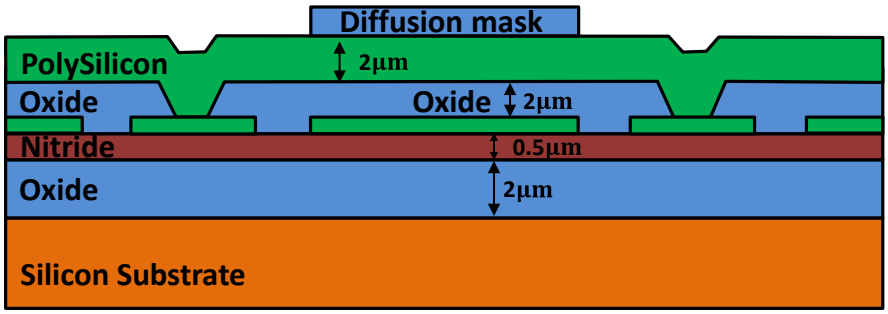

Fig. PS2.2-3

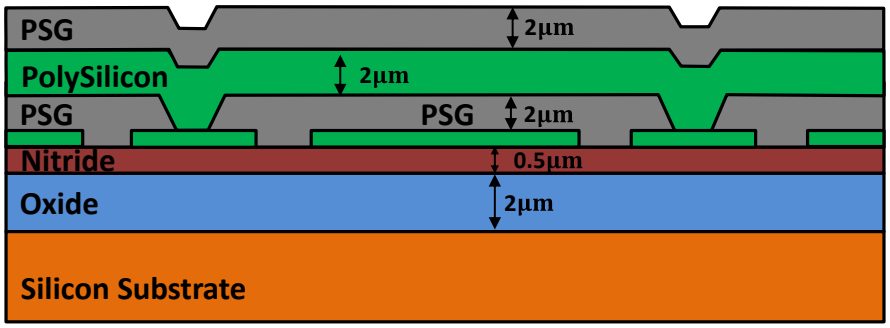

Fig. PS2.2-4

Table 2.2-1

	P	SiO_2
Density (g/cm^3)	2.34	2.2
Molar Mass (g/mol)	31	60

(a) Derive an expression for the distribution of boron atoms after the pre-deposition step and plot it as a function of depth. What is the total number of dopant atoms per unit area?

(b) Derive an expression for the distribution of boron atoms after the drive-in step and plot it as a function of depth. As discussed in lecture, you can assume the pre-deposition step equates to a thin layer of highly doped silicon at the surface of the wafer and then use the total number of dopant atoms per unit area to find the Gaussian function.

(c) The depth at which the concentration of diffused dopant atoms is the same as the background concentration is defined to be the junction depth. What is the junction depth at the end of the process?

(d) Suppose the above drive-in process is not the only high-temperature step in your process, but entails the following subsequent steps:

1. An LTO deposition at a temperature of 400℃ over a time period of 100 min.
2. Polysilicon deposition at a temperature of 600℃ over a time period of 120 min.
3. A rapid thermal anneal at temperature of 1050℃ over a time period of 1 min.

i. Rank the four thermal steps from the greatest effect on the boron diffusion profile to the least.

ii. What is the new doping depth after these additional three steps?

(e) Using the doping depth you get from (c), what is the sheet resistance of the doped polysilicon layer? Remember that the dopant concentration is a function of depth, so use the distribution function derived in (b) to find the exact sheet resistance. Assume the hole mobility in polysilicon is constant at 450 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ at room temperature and the pn-junction depletion width is negligible in comparison to junction depth.

(f) Suppose we use the layout as shown in Figure PS2.2-2 to pattern the polysilicon film to generate a MEMS accelerometer. If we apply a 100mV voltage across the two anchors, what is the steady state temperature of the proof mass? Assume the temperature of the silicon substrate and the anchors of the structure is constant at 20℃.

(g) A diffusion mask can help selectively dope certain areas in the polysilicon film. Ideally, by using a diffusion mask as shown in Figure PS2.2-3, the area underneath the diffusion mask will not be doped. However, in reality, lateral diffusion compromises the selectivity of this doping method. Calculate the lateral distance from the edges of the diffusion mask where the dopant concentration drops to 0.1% of the surface dopant concentration. (Assume the selective diffusion experiences the same pre-deposition and drive-in steps, i.e., pre-deposition alongside solid-source boron wafers for 30min at 1000^{o}C, and drive-in with no boron source for 60min at the same temperature.)

(h) A polysilicon film can also be phosphorous doped from both sides by using phosphosilicate glass (PSG) films. Figure PS2.2-4 presents a 2 μm-thick polysilicon film sandwiched between two 2μm-thick PSG layers, each deposited via LPCVD so that they contain 10 wt. % of phosphorous. The wafer is then annealed at 1000℃ in an N_2 ambient.

i. Calculate the concentration of phosphorus in PSG. (Note that you may need some additional information in Table 2.2-1.)

ii. Suppose the polysilicon beam is initially uniformly doped with gallium to a concentration $N_A = 1 \times 10^{15} cm^{-3}$. If you would like to counter-dope the top and bottom sides of the polysilicon film with phosphorous to junction depths of 800 nm on each side, how long would you need to keep the wafer at 1000^{o}C in the diffusion furnace?

3. The linear coefficient of thermal expansion of the glass used for a photolithography mask is given by the expression

$$TC_F = \frac{1}{L} \cdot \frac{\partial L}{\partial T} \approx \frac{\Delta L}{L} \cdot \frac{1}{\Delta T}$$

where L is a length on the mask and T is temperature. Let's assume $TC_F = 3\ ppm/°C$ for a given mask. Suppose that an alignment accuracy of $0.2\mu m$ across an 8-inch silicon substrate is required from one layer to the next. Assume the thermal expansion of silicon is negligible in comparison and that all previous masking steps were done with masks at the same temperature as the silicon wafer.

(a) Assuming that a scanning 1:1 projection printer with global alignment is used, how close should the temperature of the mask be kept relative to the silicon wafer during alignment in order to achieve this accuracy? (In other words, what is the maximum allowable temperature deviation?)

(b) Repeat (a) for the case of 4:1 projection stepper with die-to-die alignment. Assume the die size is $1cm^2$. Is this better than for the 1:1 projection printer?