

EE247 Lecture 23

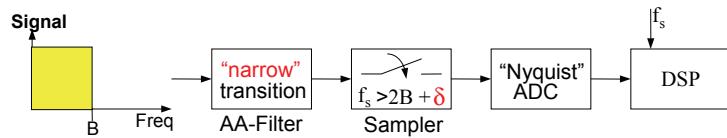
- Oversampled ADCs
 - Why oversampling?
 - Pulse-count modulation
 - Sigma-delta modulation
 - 1-Bit quantization
 - Quantization error (noise) spectrum
 - SQNR analysis
 - Limit cycle oscillations
 - 2nd order $\Sigma\Delta$ modulator
 - Practical implementation
 - Effect of various building block nonidealities on the $\Sigma\Delta$ performance
 - Integrator maximum signal handling capability
 - Integrator finite DC gain
 - Comparator hysteresis
 - Integrator non-linearity

Analog-to-Digital Converters

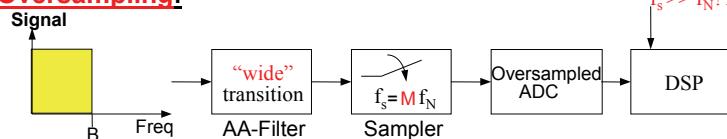
- Two categories:
 - Nyquist rate ADCs $\rightarrow f_{sig}^{max} \sim 0.5xf_{sampling}$
 - Maximum achievable signal bandwidth higher compared to oversampled type
 - Resolution limited to max. ~14bits
 -  Oversampled ADCs $\rightarrow f_{sig}^{max} \ll 0.5xf_{sampling}$
 - Maximum possible signal bandwidth lower compared to nyquist
 - Maximum achievable resolution high (18 to 20bits!)

The Case for Oversampling

Nyquist sampling:

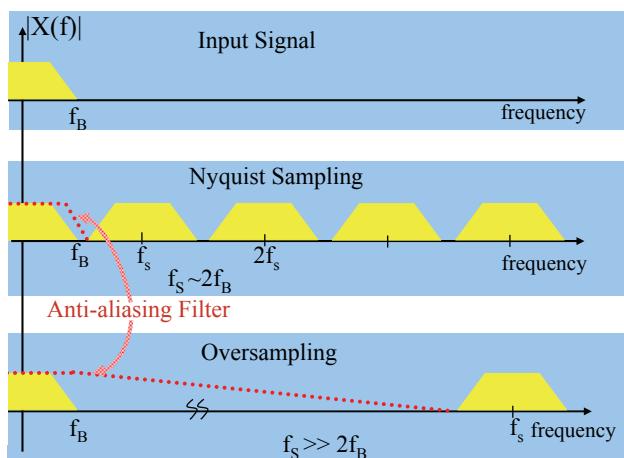


Oversampling:



- Nyquist rate $f_N \sim 2B$
- Oversampling rate $M = f_s/f_N \gg 1$

Nyquist v.s. Oversampled Converters Antialiasing Requirements

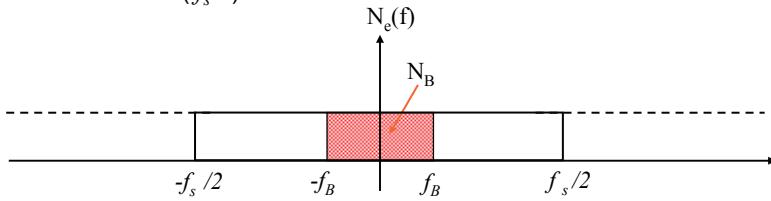


Oversampling Benefits

- Almost no stringent requirements imposed on analog building blocks
- Takes advantage of the availability of low cost, low power digital filtering
- Relaxed transition band requirements for analog anti-aliasing filters
- Reduced baseband quantization noise power
- Allows trading speed for resolution

ADC Converters Baseband Noise

- For a quantizer with quantization step size Δ and sampling rate f_s :
 - Quantization noise power distributed uniformly across Nyquist bandwidth ($f_s/2$)



- Power spectral density:

$$N_e(f) = \frac{\overline{e^2}}{f_s} = \left(\frac{\Delta^2}{12} \right) \frac{1}{f_s}$$

- Noise is distributed over the Nyquist band $-f_s/2$ to $f_s/2$

Oversampled Converters Baseband Noise

$$S_B = \int_{-f_B}^{f_B} N_e(f) df = \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12} \right) \frac{1}{f_s} df$$

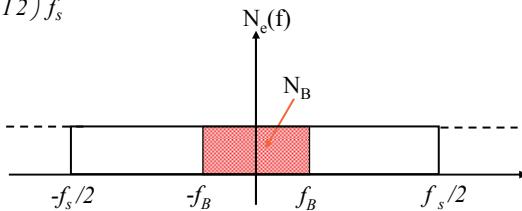
$$= \frac{\Delta^2}{12} \left(\frac{2f_B}{f_s} \right)$$

where for $f_B = f_s / 2$

$$S_{B0} = \frac{\Delta^2}{12}$$

$$S_B = S_{B0} \left(\frac{2f_B}{f_s} \right) = \frac{S_{B0}}{M}$$

where $M = \frac{f_s}{2f_B}$ = oversampling ratio



Oversampled Converters Baseband Noise

$$S_B = S_{B0} \left(\frac{2f_B}{f_s} \right) = \frac{S_{B0}}{M}$$

where $M = \frac{f_s}{2f_B}$ = oversampling ratio

2X increase in M

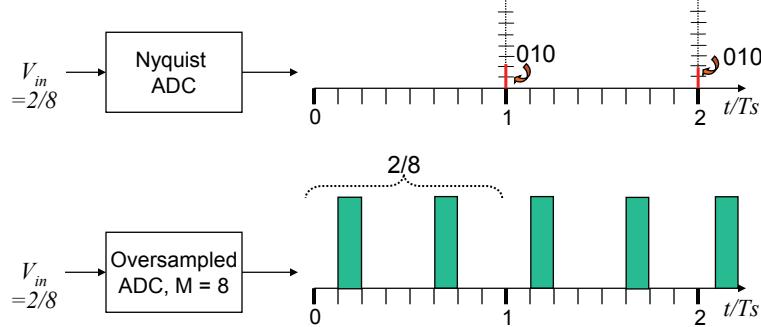
→ 3dB reduction in S_B

→ ½ bit increase in resolution/octave oversampling

To further increase the improvement in resolution:

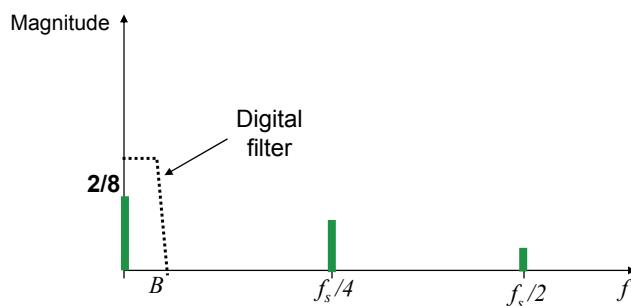
- Embed quantizer in a feedback loop
- Noise shaping (sigma delta modulation)

Pulse-Count Modulation



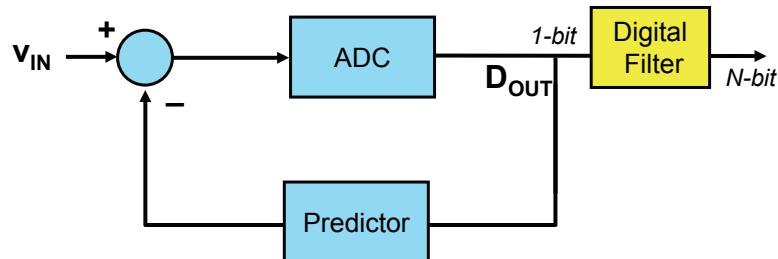
Mean of pulse-count signal approximates analog input!

Pulse-Count Output Spectrum



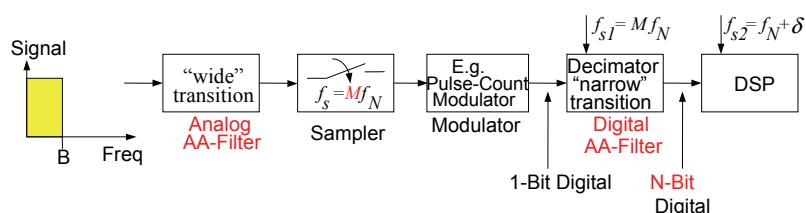
- Signal band of interest: low frequencies, $f < B \ll f_s$
- Quantization error: high frequency, $B \dots f_s / 2$
- Separate with digital low-pass filter!

Oversampled ADC Predictive Coding



- Quantize the difference signal rather than the signal itself
- Smaller input to ADC → Buy dynamic range
- Only works if combined with oversampling
- 1-Bit digital output
- Digital filter computes “average” → N-bit output

Oversampled ADC



Decimator:

- Digital (low-pass) filter
- Removes quantization noise for $f > B$
- Provides anti-alias filtering for DSP
- Narrow transition band, high-order (digital filters with high order consume significantly smaller power & area compared to analog filters)
- 1-Bit input, N-Bit output (essentially computes “average”)

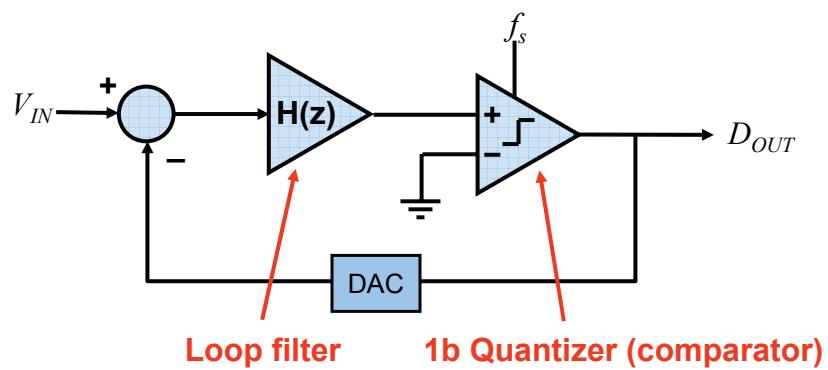
Modulator or Analog Front End (AFE)

- Objectives:
 - Convert analog input to 1-Bit pulse density stream
 - Move quantization error to high frequencies $f \gg B$
 - Operates at high frequency $f_s \gg f_N$
 - $M = 8 \dots 256$ (typical)....1024
 - Since modulator operated at high frequencies
→ need to keep analog circuitry “simple”

→ $\Sigma\Delta = \Delta\Sigma$ Modulator

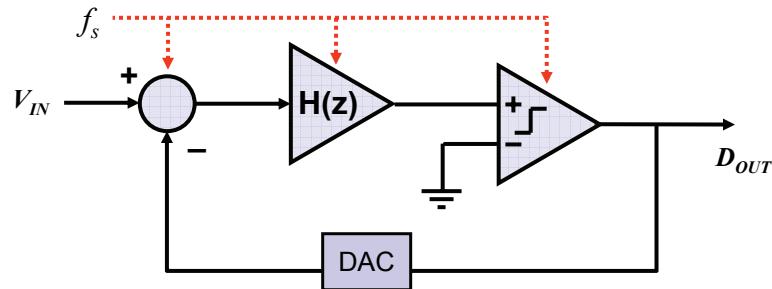
Sigma- Delta Modulators

Analog 1-Bit $\Sigma\Delta$ modulators convert a continuous time analog input v_{IN} into a 1-Bit sequence D_{OUT}



Sigma-Delta Modulators

- The loop filter H can be either switched-capacitor or continuous time
- Switched-capacitor filters are “easier” to implement + frequency characteristics scale with clock rate
- Continuous time filters provide anti-aliasing protection

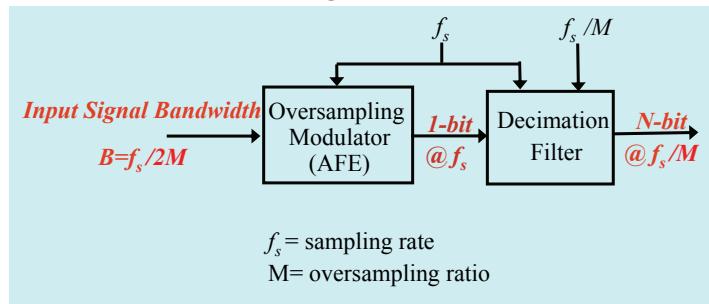


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Oversampled ADCs

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Oversampling A/D Conversion



- Analog front-end → oversampled noise-shaping modulator
 - Converts original signal to a 1-bit digital output at the high rate of $(2BM)$
- Digital back-end → digital filter (decimator)
 - Removes out-of-band quantization noise
 - Provides anti-aliasing to allow re-sampling @ lower sampling rate

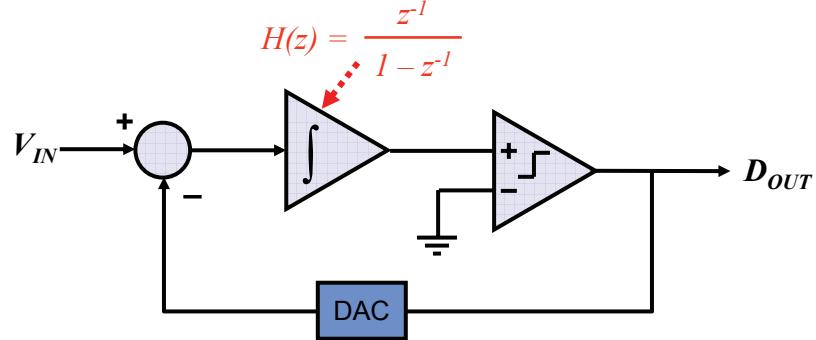
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Oversampled ADCs

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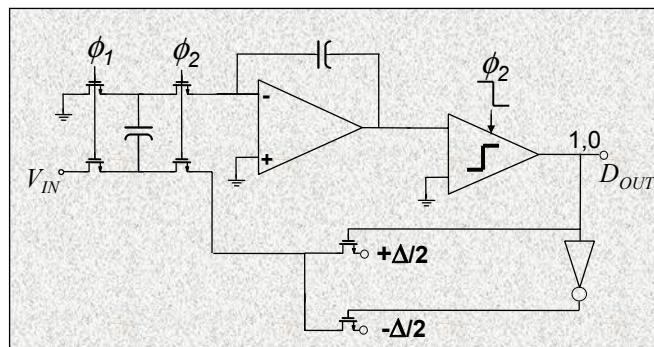
1st Order $\Sigma\Delta$ Modulator

1st order modulator, simplest loop filter → an integrator



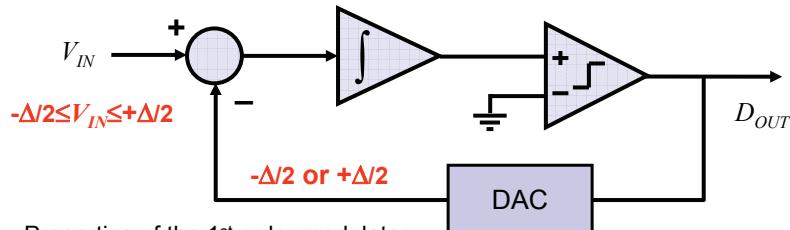
Note: Non-linear system with memory → difficult to analyze

1st Order $\Sigma\Delta$ Modulator Switched-capacitor implementation



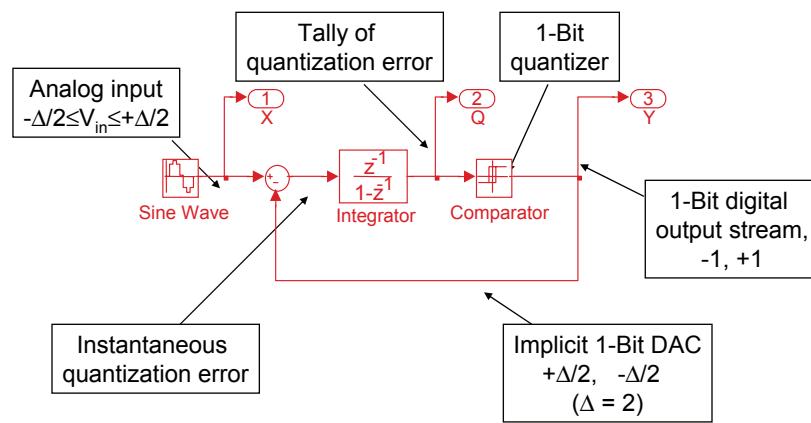
- Full-scale input range → Δ
- Note that Δ here is different from Nyquist rate ADC Δ (1LSB)

1st Order $\Delta\Sigma$ Modulator



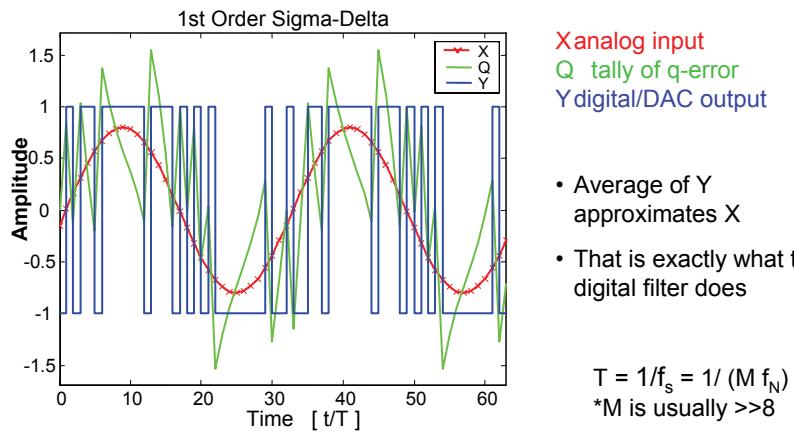
- Properties of the 1st order modulator:
 - Maximum analog input range is equal to the DAC reference levels
 - The average value of D_{OUT} must equal the average value of V_{IN}
 - +1's (or -1's) density in D_{OUT} is an inherently monotonic function of V_{IN}
→ To 1st order, linearity is not dependent on component matching
 - Alternative multi-bit DAC (and ADCs) solutions reduce the quantization error but loose this inherent monotonicity & relaxed matching requirements

1st Order $\Sigma\Delta$ Modulator



- M chosen to be 8 (low) to ease observability

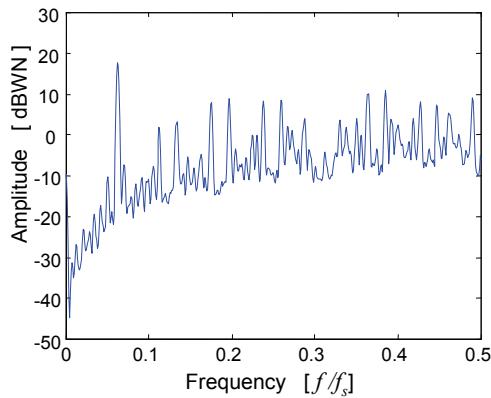
1st Order Modulator Signals



$\Sigma\Delta$ Modulator Characteristics

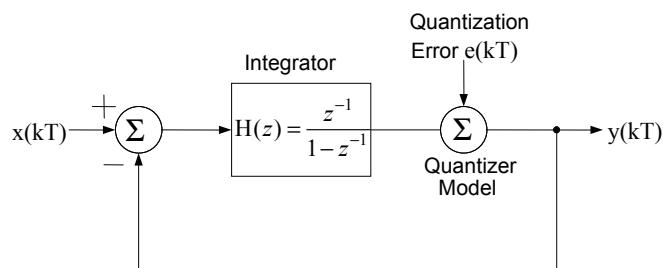
- Inherently linear for 1-Bit DAC
- Quantization noise and thermal noise (KT/C) distributed over $-f_s/2$ to $+f_s/2$
 - Total noise within signal bandwidth reduced by $1/M$
 - Required capacitor sizes $\propto 1/M$ compared to nyquist rate ADCs
- Very high SQNR achievable (> 20 Bits!)
- To first order, quantization error independent of component matching
- Limited to moderate & low speed

1st Order $\Sigma\Delta$ Modulator Output Spectrum



- Quantization noise definitely not white!
 - Skewed towards higher frequencies
 - Notice the distinct tones
- dBWN (dB White Noise) scale sets the 0dB line at the noise per bin of a random -1, +1 sequence

Quantization Noise Analysis

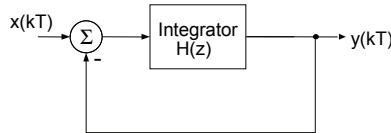


- Sigma-Delta modulators are nonlinear systems with memory → difficult to analyze directly
- Representing the quantizer as an additive noise source linearizes the system

Signal Transfer Function

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

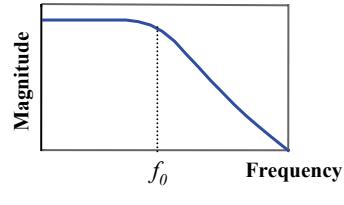
$$H(j\omega) = \frac{\omega_0}{j\omega}$$



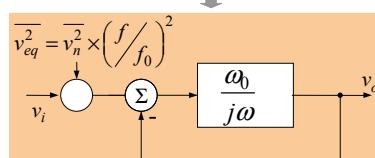
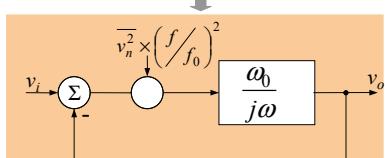
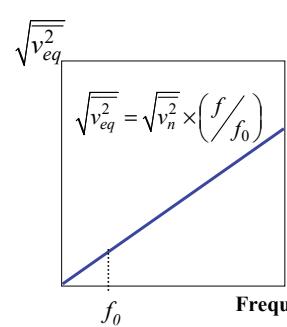
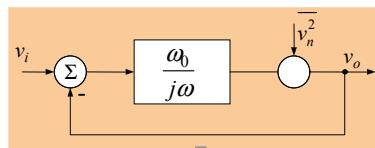
Signal transfer function
→ low pass function:

$$H_{Sig}(j\omega) = \frac{1}{1 + s/\omega_0}$$

$$H_{Sig}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} = z^{-1} \Rightarrow \text{Delay}$$

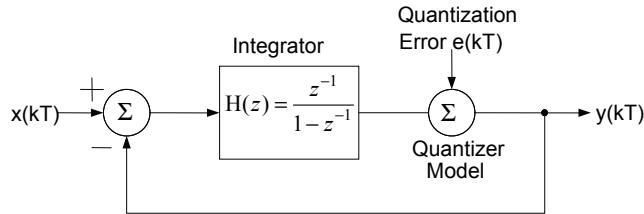


Noise Transfer Function Qualitative Analysis



- Input referred-noise → zero @ DC (s-plane)

1st Order ΣΔ Modulator STF and NTF



Signal transfer function:

$$\text{STF} = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} = z^{-1} \Rightarrow \text{Delay}$$

Noise transfer function:

$$\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1} \Rightarrow \text{Differentiator}$$

Noise Transfer Function

$$\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1} \quad \text{set } z = e^{j\omega T}$$

$$\begin{aligned} \text{NTF}(j\omega) &= (1 - e^{-j\omega T}) = 2e^{-j\omega T/2} \left(\frac{e^{j\omega T/2} - e^{-j\omega T/2}}{2} \right) \\ &= 2e^{-j\omega T/2} j \sin(\omega T/2) \\ &= 2e^{-j\omega T/2} \times e^{-j\pi/2} [\sin(\omega T/2)] \\ &= [2 \sin(\omega T/2)] e^{-j(\omega T - \pi)/2} \end{aligned}$$

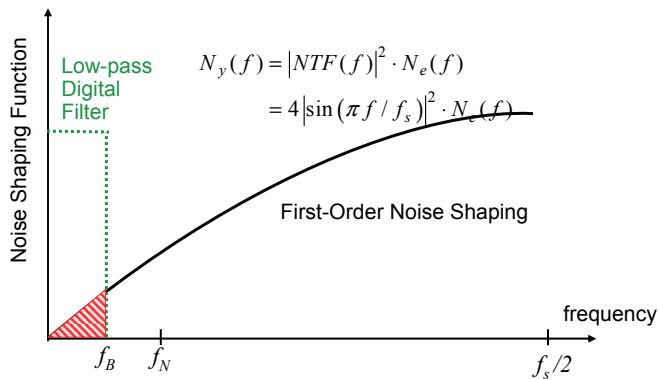
where $T = 1/f_s$

Thus:

$$|NTF(f)| = 2 |\sin(\omega T/2)| = 2 |\sin(\pi f/f_s)|$$

$$\text{Output noise power spectrum: } N_y(f) = |NTF(f)|^2 N_e(f)$$

First Order $\Sigma\Delta$ Modulator Noise Transfer Characteristics



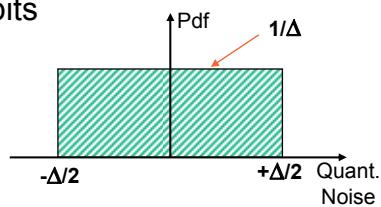
Key Point:

Most of quantization noise pushed out of frequency band of interest

Quantizer Error

- For quantizers with many bits

$$\overline{e^2(kT)} = \frac{\Delta^2}{12}$$

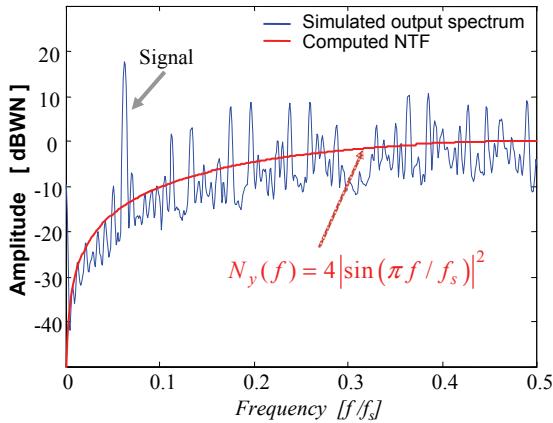


- Let's use the same expression for the 1-bit case

Use simulation to verify validity

- Experience: Often sufficiently accurate to be useful, with enough exceptions to be careful

First Order $\Sigma\Delta$ Modulator Simulated Noise Transfer Characteristic



- Confirms assumption of quantization noise being white at insertion point
- Linearized model seems to be accurate

First Order $\Sigma\Delta$ Modulator In-Band Quantization Noise

$$NTF(z) = 1 - z^{-1}$$

$$|NTF(f)|^2 = 4 |\sin(\pi f / f_s)|^2 \quad \text{for } M \gg 1$$

$$\overline{S_Q} = \int_{-B}^B S_Q(f) |NTF(z)|^2_{z=e^{j2\pi fT}} df$$

$$\approx \int_{-f_s/2M}^{f_s/2M} \frac{1}{f_s} \frac{\Delta^2}{12} (2 \sin \pi f T)^2 df$$

$\rightarrow \overline{S_Q} \approx \frac{\pi^2}{3} \frac{1}{M^3} \frac{\Delta^2}{12}$

Total in-band quantization noise

1st Order $\Sigma\Delta$ Dynamic Range

$$DR = 10 \log \left[\frac{\text{full-scale signal power}}{\text{inband noise power}} \right] = 10 \log \left[\frac{\overline{S_X}}{\overline{S_Q}} \right]$$

$$\overline{S_X} = \frac{1}{2} \left(\frac{\Delta}{2} \right)^2 \quad \text{sinusoidal input, } STF = 1$$

$$\overline{S_Q} = \frac{\pi^2}{3} \frac{1}{M^3} \frac{\Delta^2}{12}$$

$$\frac{\overline{S_X}}{\overline{S_Q}} = \frac{9}{2\pi^2} M^3$$

M	DR
16	33 dB
32	42 dB
1024	87 dB

$$DR = 10 \log \left[\frac{9}{2\pi^2} M^3 \right] = 10 \log \left[\frac{9}{2\pi^2} \right] + 30 \log M$$

$$DR = -3.4 \text{dB} + 30 \log M$$

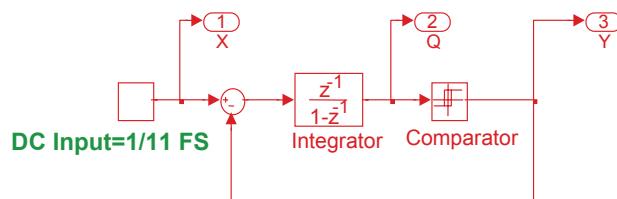
2X increase in M \rightarrow 9dB (1.5-Bit) increase in dynamic range

Oversampling and Noise Shaping

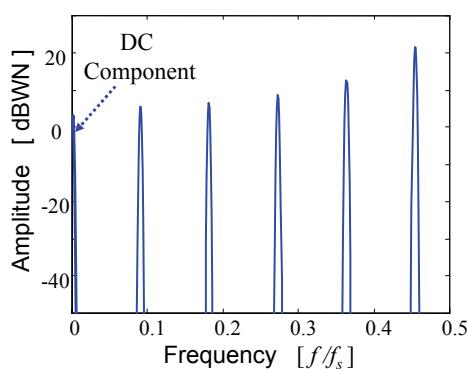
- $\Sigma\Delta$ modulators have interesting characteristics
 - Unity gain for input signal V_{IN}
 - Significant attenuation of in-band quantization noise injected at quantizer input
 - Performance significantly better than 1-bit noise quantizer possible for frequencies $\ll f_s$
- Increase in oversampling ($M = f_s/f_N \gg 1$) improves SQNR considerably
 - 1st order $\Sigma\Delta$: DR increases 9dB for each doubling of M
 - To first order, SQNR independent of circuit complexity and accuracy
- Analysis assumes that the quantizer noise is “white”
 - Not entirely true in practice, especially for low-order modulators
 - Practical modulators suffer from other noise sources also (e.g. thermal & 1/f noise)

1st Order $\Sigma\Delta$ Modulator Response to DC Input

- Matlab & Simulink model used
- Input → DC at 1/11 full-scale level



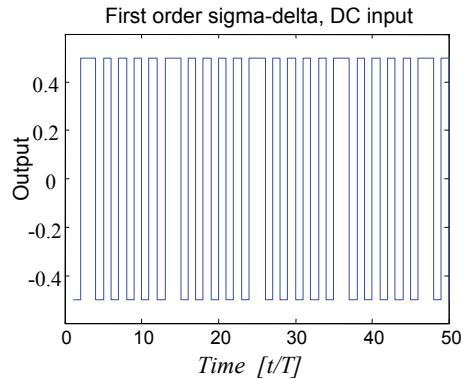
1st Order $\Sigma\Delta$ Response to DC Input



- DC input A = 1/11
- Output spectrum shows DC component plus distinct tones!!
- Tones frequency shaped the same as quantization noise
→ More prominent at higher frequencies
- Seems like periodic quantization “noise”

Limit Cycle Oscillation

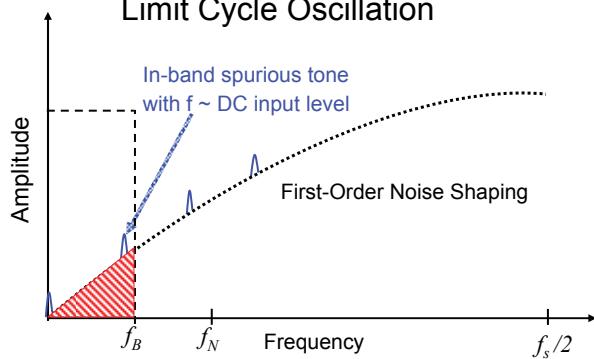
DC input 1/11 →
Periodic sequence:



1	+1	}
2	+1	}
3	-1	}
4	+1	}
5	-1	}
6	+1	}
7	-1	}
8	+1	}
9	-1	}
10	+1	}
11	-1	}

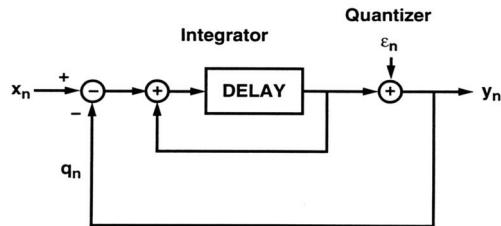
→ Average = 1/11

1st Order $\Sigma\Delta$ Limit Cycle Oscillation



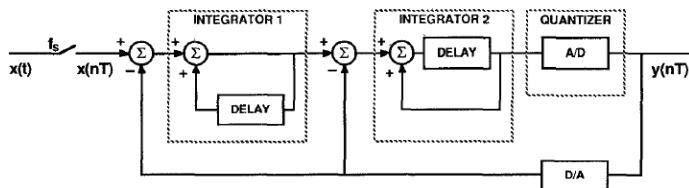
- Problem: quantization noise becomes periodic in response to low level DC inputs & could fall within passband of interest!
- Solution:
 - Use dithering (inject noise-like signal at the input): randomizes quantization noise
 - If circuit thermal noise is large enough → acts as dither
 - Second order loop

1st Order $\Sigma\Delta$ Modulator Linearized Model Analysis



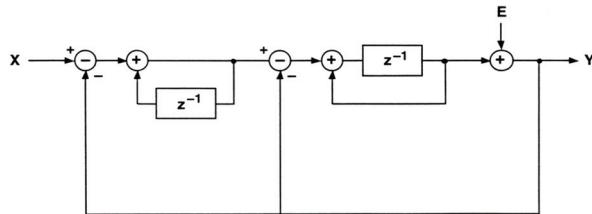
$$Y(z) = \underbrace{z^{-1}}_{\text{LPF}} X(z) + \underbrace{(1 - z^{-1})}_{\text{HPF}} E(z)$$

2nd Order $\Sigma\Delta$ Modulator



- Two integrators in series
- Single quantizer (typically 1-bit)
- Feedback from output to both integrators
- Tones less prominent compared to 1st order

2nd Order ΣΔ Modulator Linearized Model Analysis



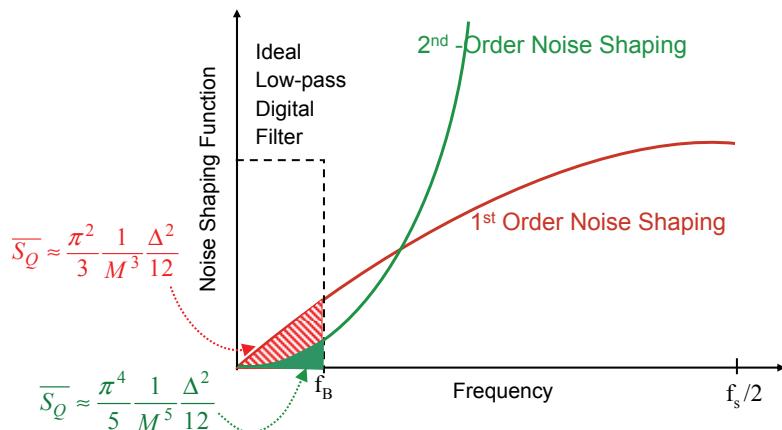
Recursive derivation: $Y_n = X_{n-1} + (E_n - 2E_{n-1} + E_{n-2})$

Using the delay operator z^{-1} : $Y(z) = \underbrace{z^{-1}}_{\text{LPF}} X(z) + \underbrace{(1 - z^{-1})^2}_{\text{HPF}} E(z)$

2nd Order ΣΔ Modulator In-Band Quantization Noise

$$\begin{aligned}
 NTF(z) &= (1 - z^{-1})^2 \\
 |NTF(f)|^2 &= \\
 &= 2^4 |\sin(\pi f / f_s)|^4 \quad \text{for } M \gg 1 \\
 \overline{S_Q} &= \int_{-B}^B S_Q(f) |NTF(z)|^2_{z=e^{j2\pi fT}} df \\
 &\cong \int_{-\frac{f_s}{2M}}^{\frac{f_s}{2M}} \frac{1}{f_s} \frac{\Delta^2}{12} (2 \sin \pi f T)^4 df \\
 &\approx \frac{\pi^4}{5} \frac{1}{M^5} \frac{\Delta^2}{12}
 \end{aligned}$$

Quantization Noise 2nd Order ΣΔ Modulator vs 1st Order Modulator



2nd Order ΣΔ Modulator Dynamic Range

$$DR = 10 \log \left[\frac{\text{full-scale signal power}}{\text{inband noise power}} \right] = 10 \log \left[\frac{\overline{S_X}}{\overline{S_Q}} \right]$$

$$\overline{S_X} = \frac{1}{2} \left(\frac{\Delta}{2} \right)^2 \quad \text{sinusoidal input, } STF = 1$$

$$\overline{S_Q} = \frac{\pi^4}{5} \frac{1}{M^5} \frac{\Delta^2}{12}$$

$$\frac{\overline{S_X}}{\overline{S_Q}} = \frac{15}{2\pi^4} M^5$$

$$DR = 10 \log \left[\frac{15}{2\pi^4} M^5 \right] = 10 \log \left[\frac{15}{2\pi^4} \right] + 50 \log M$$

$$DR = -11.1dB + 50 \log M$$

2X increase in $M \rightarrow 15dB$ (2.5-bit) increase in DR

2nd Order vs 1st Order ΣΔ Modulator Dynamic Range

M	2 nd Order D.R.	1 st Order D.R.	Resolution (2 nd order - 1 st order)
16	49 dB (7.8bit)	33dB (5.2bit)	2.6 bit
32	64 dB (10.3bit)	42dB (6.7bit)	3.6 bit
256	109 dB (17.9bit)	68.8dB (11.1bit)	6.8 bit
1024	139 dB (22.8bit)	87dB (14.2bit)	8.6 bit

- Note: For higher oversampling ratios resolution of 2nd order modulator significantly higher compared to 1st order

2nd Order ΣΔ Modulator Example

- Digital audio application
 - Signal bandwidth 20kHz
 - Desired resolution 16-bit

16-bit → 98 dB Dynamic Range

$$DR_{2nd\ order\ \Sigma\Delta} = -11.1dB + 50\log M$$

$$M_{min} = 153$$

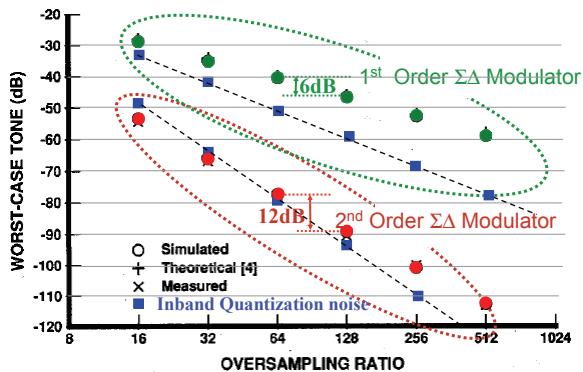
$M \rightarrow 256 = 2^8$ ($\rightarrow DR=109dB$) two reasons:

- Allow some margin so that thermal noise dominate & provides dithering to minimize level of in-band limit cycle oscillation
- Choice of M power of 2 → ease of digital filter implementation

→ Sampling rate $(2 \times 20\text{kHz} + 5\text{kHz})M = 12\text{MHz}$ (quite reasonable!)

Limit Cycle Tones in 1st Order & 2nd Order ΣΔ Modulator

- Higher oversampling ratio → lower tones
- 2nd order tones much lower compared to 1st
- 2X increase in M decreases the tones by 6dB for 1st order loop and 12dB for 2nd order loop

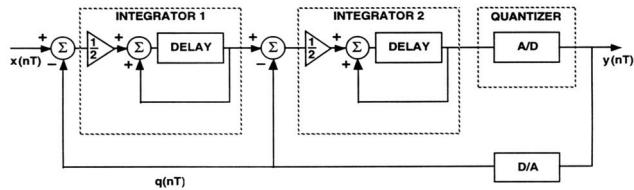


Ref: B. P. Brandt, et al., "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.
R. Gray, "Spectral analysis of quantization noise in a single-loop sigma-delta modulator with dc input," IEEE Trans. Commun., vol. 37, pp. 588-599, June 1989.

ΣΔ Implementation Practical Design Considerations

- Internal node scaling & clipping
- Effect of finite opamp gain & linearity
- KT/C noise
- Opamp noise
- Effect of comparator nonidealities
- Power dissipation considerations

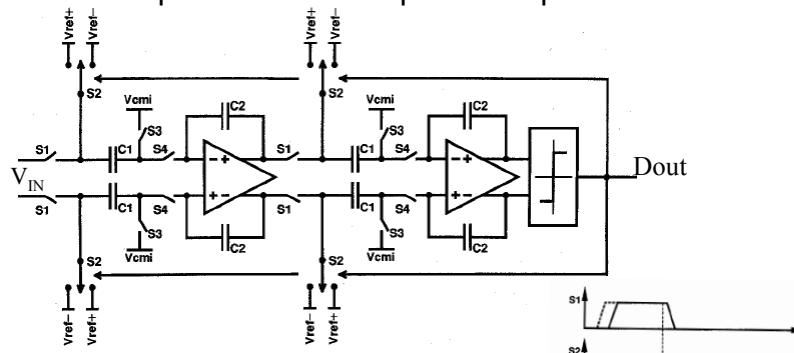
Switched-Capacitor Implementation 2nd Order $\Sigma\Delta$ Nodes Scaled for Maximum Dynamic Range



- Modification (gain of $1/2$ in front of integrators) reduce & optimize required signal range at the integrator outputs $\sim 1.7x$ input full-scale (Δ)
- Note: Non-idealities associated with 2nd integrator and quantizer when referred to the $\Sigma\Delta$ input is attenuated by 1st integrator high gain
→ The only building block requiring low-noise and high accuracy is the 1st integrator

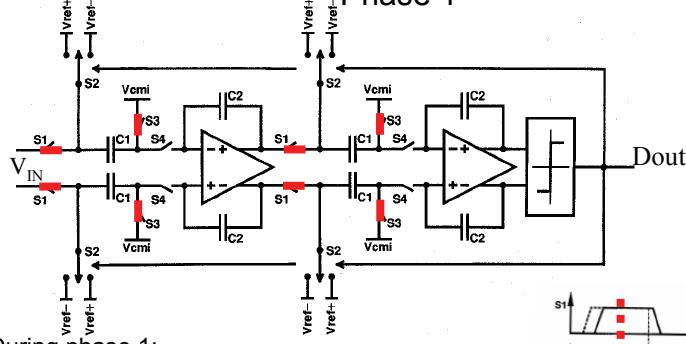
Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order $\Sigma\Delta$ Modulator Example: Switched-Capacitor Implementation



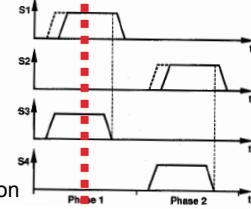
- Fully differential front-end
- Two bottom-plate integrators
- 1-bit DAC is made of switches and Vrefs

Switched-Capacitor Implementation 2nd Order $\Sigma\Delta$ Phase 1

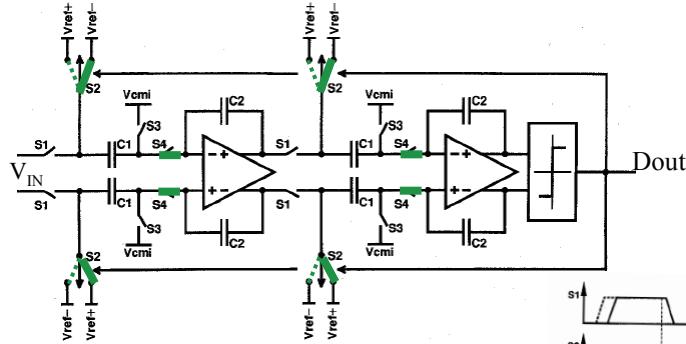


During phase 1:

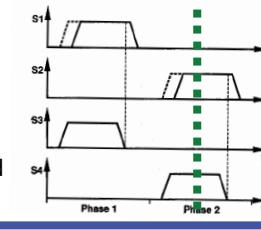
- 1st integrator samples V_{IN} on 1st stage C_1
- 2nd integrator samples output of 1st integrator
- Comparator senses polarity of 2nd intg. output \rightarrow result saved in output latch
- S_3 opens prior to $S_1 \rightarrow$ minimize effect of charge injection



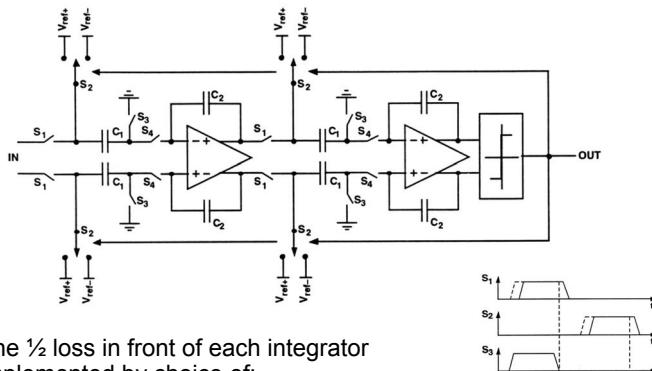
Switched-Capacitor Implementation 2nd Order $\Sigma\Delta$ Phase 2



- Note: S_2 connects integrator inputs to + or - V_{ref} , polarity depends on whether D_{out} is 0 or 1
- Input sampled during ϕ_1 – or + $C_1 \times V_{ref}$ transferred to $C_2 \rightarrow$ DAC output subtraction & integration



2nd Order ΣΔ Modulator Switched-Capacitor Implementation



- The $\frac{1}{2}$ loss in front of each integrator implemented by choice of:

$$C_2 = 2C_1 \quad \rightarrow f_0^{intg} = f_s / (4\pi)$$

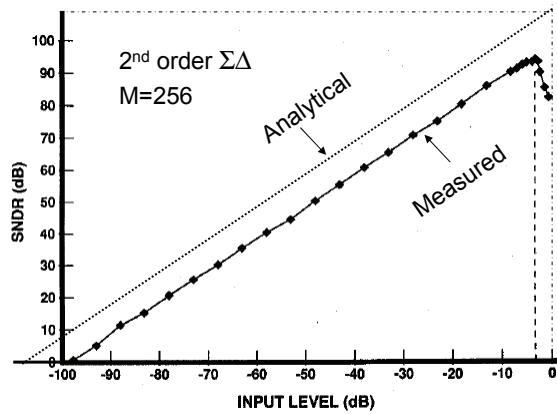
Design Phase Simulations

- Design of oversampled ADCs requires simulation of extremely long data traces due to the oversampled nature of the system
- SPICE type simulators:
 - Normally used to test for gross circuit errors only
 - Too slow for detailed performance verification
- Typically, behavioral modeling is used in MATLAB-like environments
- Circuit non-idealities either computed or found by using SPICE at subcircuit level
- Non-idealities introduced in the behavioral model one-by-one first to fully understand the effect of each individually
- Next step is to add as many of the non-idealities simultaneously as possible to verify whether there are interactions among non-idealities

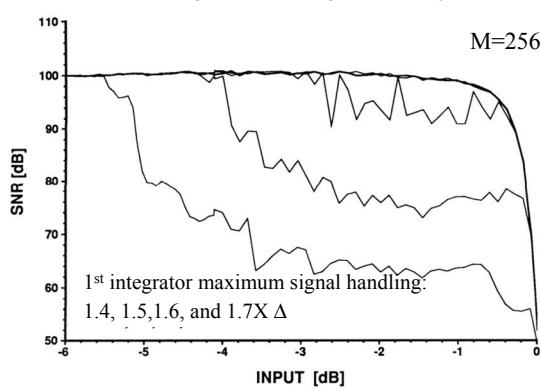
Example: Testing $\Sigma\Delta$ ADC

Note:
The Nyquist ADC tests such as INL and DNL test do not apply to $\Sigma\Delta$ modulator type ADCS

$\Sigma\Delta$ testing is performed via SNDR as a function of input signal level



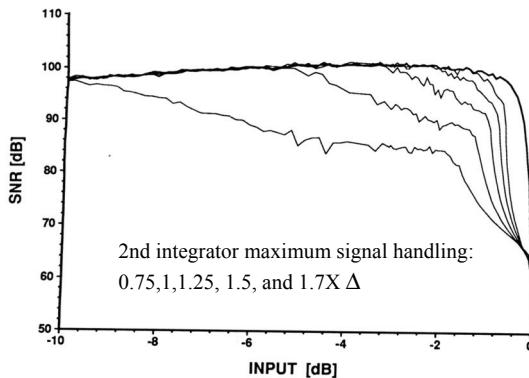
- Behavioral model
- Non-idealities tested one by one



- Effect of 1st Integrator maximum signal handling capability on converter SNR
→ No SNR loss for max. sig. handling > 1.7 Δ

2nd Order $\Sigma\Delta$

Effect of 2nd Integrator Maximum Signal Handling Capability on SNR



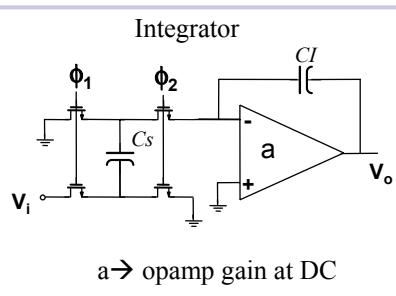
- Effect of 2nd Integrator maximum signal handling capability on SNR

→ No SNR loss for max. sig. handling > 1.7 Δ

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2nd Order $\Sigma\Delta$

Effect of Integrator Finite DC Gain

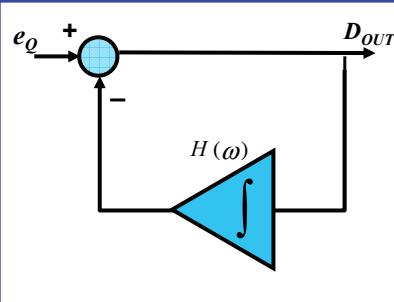
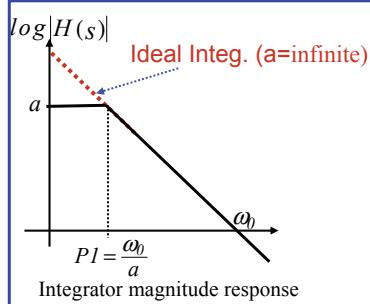


$$H(z)_{ideal} = \frac{Cs}{CI} \times \frac{z^{-1}}{1 - z^{-1}}$$

$$H(z)_{Finite DC Gain} = \frac{Cs}{CI} \times \frac{\left(\frac{a}{1 + a + \frac{Cs}{CI}} \right) z^{-1}}{1 - \left(\frac{1 + a}{1 + a + \frac{Cs}{CI}} \right) z^{-1}}$$

$$\rightarrow H(DC) = a$$

2nd Order $\Sigma\Delta$ Effect of Integrator Finite DC Gain



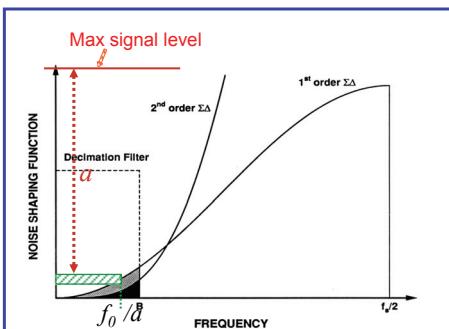
- Note: Quantization transfer function wrt output has integrator in the feedback path:

$$\frac{D_{out}}{e_Q} = \frac{1}{1 + H(\omega)}$$

→ @ DC for ideal integ: $\frac{D_{out}}{e_Q} = 0$

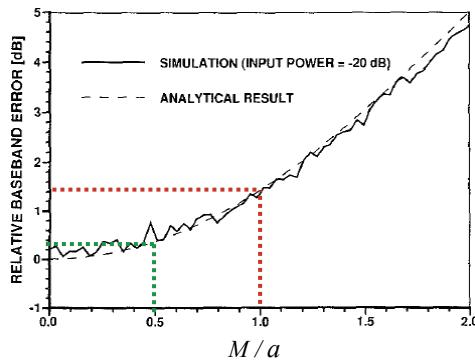
→ @ DC for real integ: $\frac{D_{out}}{e_Q} \approx \frac{1}{a}$

1st & 2nd Order $\Sigma\Delta$ Effect of Integrator Finite DC Gain



- Low integrator DC gain → Increase in total in-band quantization noise
- Can be shown: If $a > M$ (oversampling ratio) → Insignificant degradation in SNR
- Normally DC gain designed to be $\gg M$ in order to suppress nonlinearities

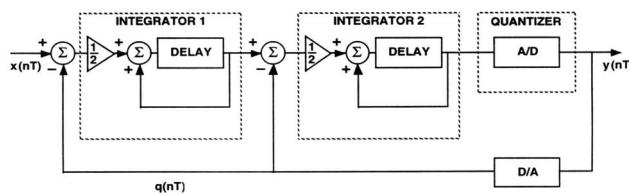
2nd Order $\Sigma\Delta$ Effect of Integrator Finite DC Gain



- Example: $a = 2M \rightarrow 0.4\text{dB}$ degradation in SNR
- $a = M \rightarrow 1.4\text{dB}$ degradation in SNR

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

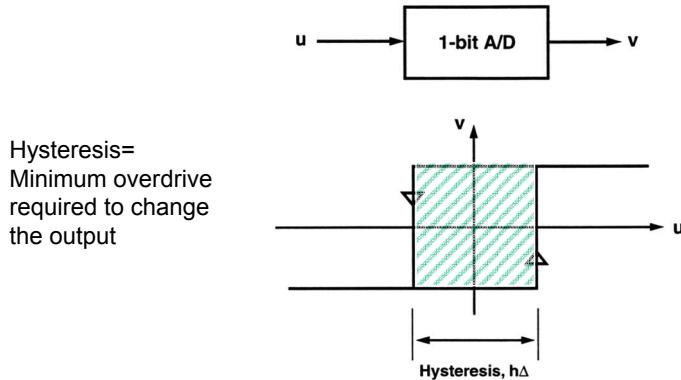
2nd Order $\Sigma\Delta$ Effect of Comparator Non-Idealities on $\Sigma\Delta$ Performance



1-bit A/D → Single comparator

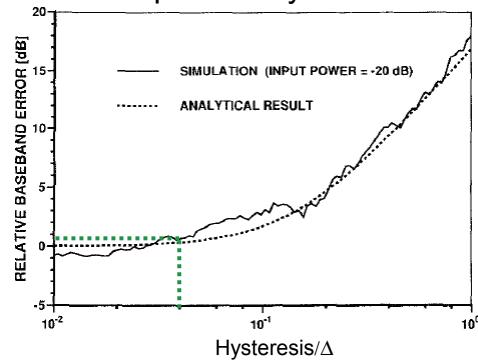
- Speed must be adequate for the operating sampling rate
- Input referred offset- feedback loop & high DC intg. gain suppresses the effect
→ $\Sigma\Delta$ performance quite insensitive to comparator offset
- Input referred comparator noise- same as offset
- Hysteresis= Minimum overdrive required to change the output

2nd Order $\Sigma\Delta$ Comparator Hysteresis



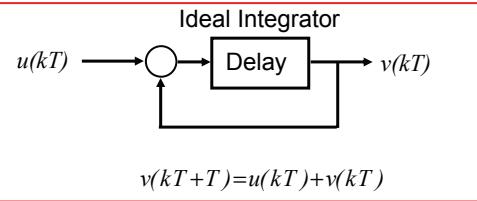
Hysteresis=
Minimum overdrive
required to change
the output

2nd Order $\Sigma\Delta$ Comparator Hysteresis



- Comparator hysteresis $< \Delta/25$ does not affect SNR
 - E.g. $\Delta=1V$, comparator hysteresis up to 40mV tolerable
- Key Point:** One of the main advantages of $\Sigma\Delta$ ADCs → Highly tolerant of comparator and in general building-block non-idealities

2nd Order $\Sigma\Delta$ Effect of Integrator Nonlinearities



With non-linearity added:

$$\begin{aligned} v(kT+T) = & u(kT) + \alpha_2 [u(kT)]^2 + \alpha_3 [u(kT)]^3 + \dots \\ & + v(kT) + \beta_2 [v(kT)]^2 + \beta_3 [v(kT)]^3 + \dots \end{aligned}$$

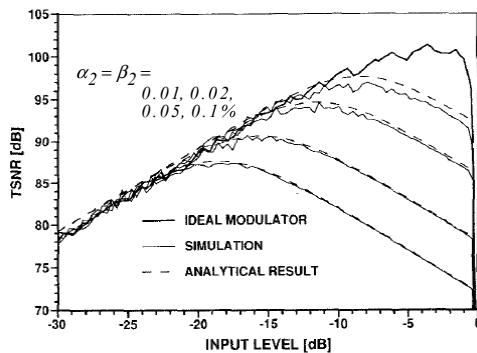
Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

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Oversampled ADCs

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2nd Order $\Sigma\Delta$ Effect of Integrator Nonlinearities (Single-Ended)



- Simulation for single-ended topology
- Effect of even order nonlinearities can be significantly suppressed by using differential circuit topologies

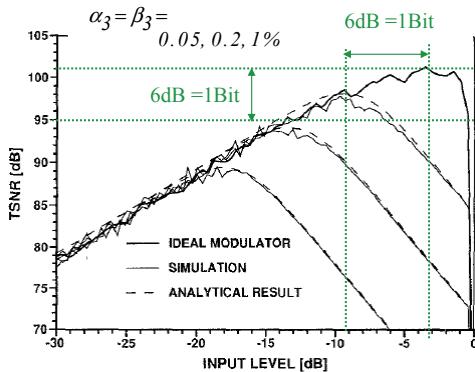
Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

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Oversampled ADCs

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2nd Order $\Sigma\Delta$ Effect of Integrator Nonlinearities



- Simulation for single-ended topology
- Odd order nonlinearities (3rd in this case)

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2nd Order $\Sigma\Delta$ Effect of Integrator Nonlinearities

- Odd order nonlinearities (usually 3rd) could cause significant loss of SNR for high resolution oversampled ADCs
- Two significant source of non-linearities:
 - Non-linearities associated with opamp used to build integrators
 - Opamp open-loop non-linearities are suppressed by the loopgain since there is feedback around the opamp
 - Class A opamps tend to have lower open loop gain but more linear output versus input transfer characteristic
 - Class A/B opamps typically have higher open loop gain but non-linear transfer function. At times this type is preferred for $\Sigma\Delta$ AFE due to its superior slew rate compared to class A type
 - Integrator capacitor non-linearities
 - Poly-Sio2-Poly capacitors → non-linearity in the order of 10ppm/V
 - Metal-Sio2-Metal capacitors ~ 1ppm/V