

EE247 Lecture 22

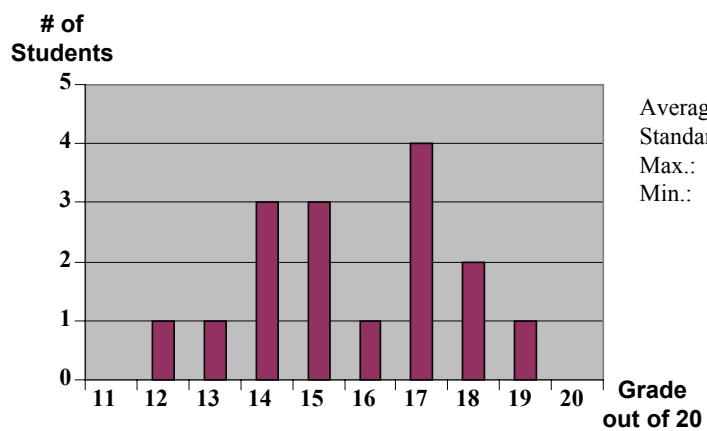
- Pipelined ADCs (continued)
 - Effect gain stage, sub-DAC non-idealities on overall ADC performance
 - Digital calibration (continued)
 - Correction for inter-stage gain nonlinearity
 - Implementation
 - Practical circuits
 - Stage scaling
 - Combining the bits
 - Stage implementation
 - Circuits
 - Noise budgeting
 - How many bits per stage?
 - Algorithmic ADCs utilizing pipeline structure
 - Advanced background calibration techniques
- Time Interleaved Converters
- VCO Based ADCs (guest speaker: Rikky Muller)

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Pipelined ADCs and More

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EE247 Midterm Exam Statistics

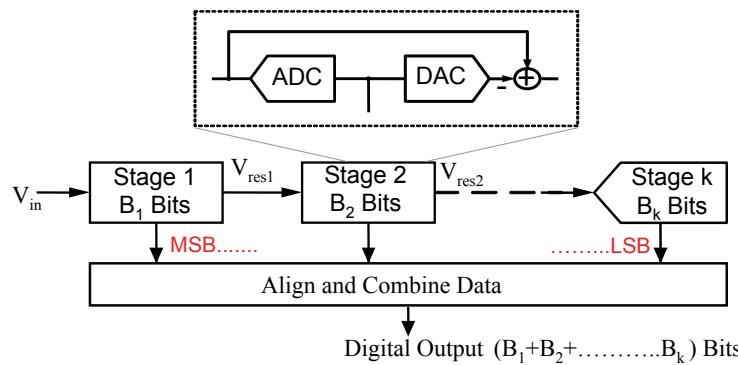


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Pipelined ADCs and More

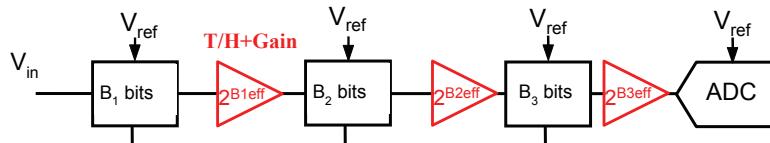
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Pipeline ADC Block Diagram



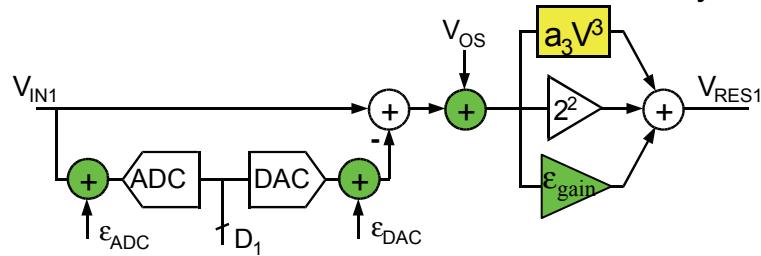
- Idea: Cascade several low resolution stages to obtain high overall resolution (e.g. 10bit ADC can be built with series of 10 ADCs each 1-bit only!)
- Each stage performs coarse A/D conversion and computes its quantization error, or "residue"

Summary So Far Pipelined A/D Converters



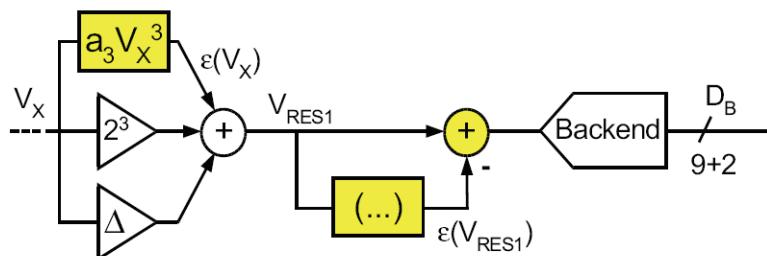
- Cascade of low resolution stages
 - By adding inter-stage gain= $2^{B_{\text{eff}}}$
 - No need to scale down Vref for stages down the pipe
 - Reduced accuracy requirement for stages coming after stage 1
- Addition of Track & Hold function to interstage-gain →
 - Stages can operate concurrently→
 - Throughput increased to as high as one sample per clock cycle
 - Latency function of number of stages & conversion-per-stage
- Correction for circuit non-idealities
 - Built-in redundancy compensates for sub-ADC inaccuracies such as comparator offset (interstage gain: $G=2^{B_{\text{eff}}}$, $B_{\text{eff}} < B_n$)

Pipelined ADC Error Correction/Calibration Summary



Error	Correction/Calibration
ϵ_{ADC}, V_{os}	Redundancy either same stage or next stage
ϵ_{gain}	Digital adjustment
ϵ_{DAC}	Either sufficient component matching or digital calibration
Inter-stage amplifier non-linearity	?

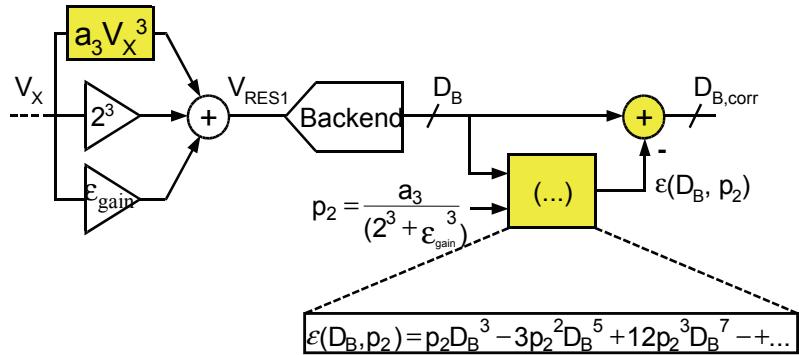
Inter-stage Gain Nonlinearity



- Invert gain stage non-linear polynomial
- Express error as function of V_{RES1}
- Push error into digital domain through backend

Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," ISSCC Dig. Techn. Papers, pp. 328-329, 2003

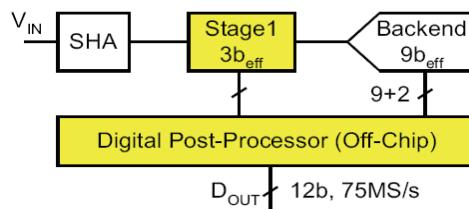
Inter-stage Gain Nonlinearity



- Pre-computed & stored in table look-up form
- p_2 continuously estimated & updated (account for temp. & other variations)

Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," ISSCC Dig. Techn. Papers, pp. 328-329, 2003

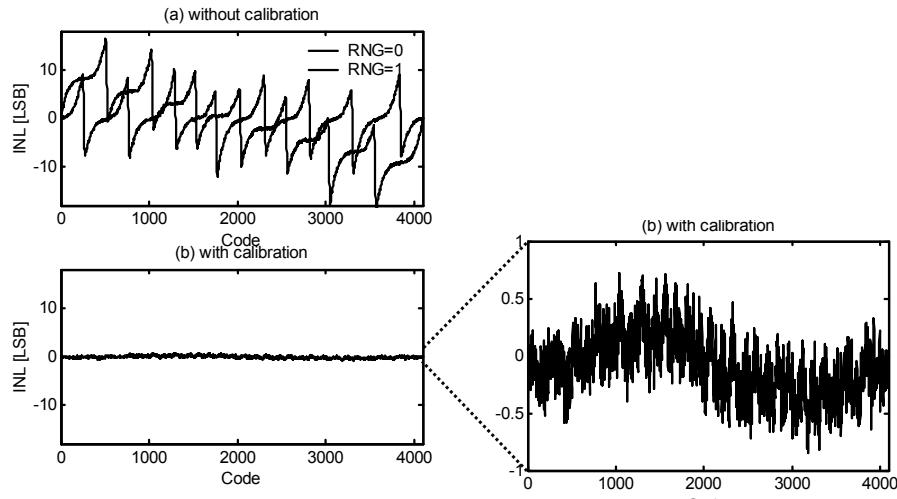
Inter-stage Gain Nonlinearity Compensation Proof of Concept Evaluation Prototype



- Re-used 14-bit ADC in 0.35μm from Analog Devices [Kelly, ISSCC 2001]
- Modified only 1st stage with 3-b_{eff} → open-loop amplifier built with simple diff-pair + resistive load instead of the conventional feedback around high-gain amp
- Conventional 9-b_{eff} backend, 2-bit redundancy in 1st stage
- Real-time post-processor off-chip (FPGA)

Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," ISSCC Dig. Techn. Papers, pp. 328-329, 2003

Measurement Results 12-bit ADC w Extra 2-bits for Calibration



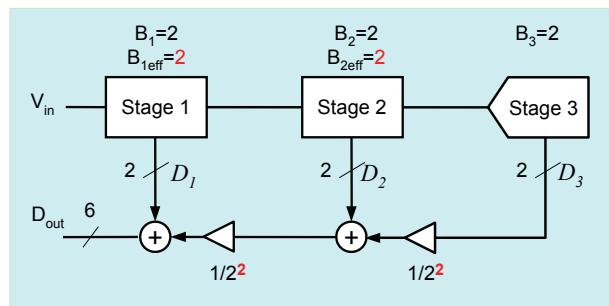
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Pipelined ADCs and More

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Combining the Bits

- Example: Three 2-bit stages, no redundancy



$$D_{out} = D_1 + \frac{1}{2^{B1\text{eff}}} D_2 + \frac{1}{2^{B1\text{eff}} \cdot 2^{B2\text{eff}}} D_3$$

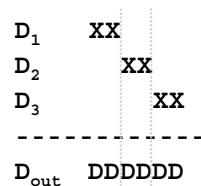
$$D_{out} = D_1 + \frac{1}{4} D_2 + \frac{1}{16} D_3$$

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Pipelined ADCs and More

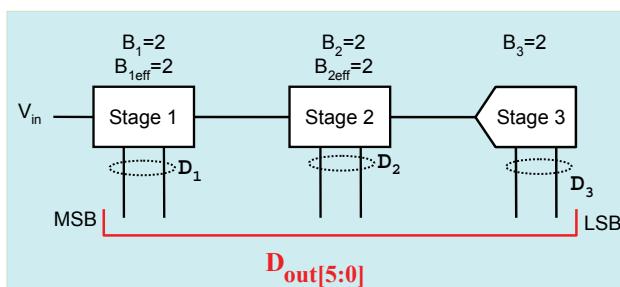
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Combining the Bits



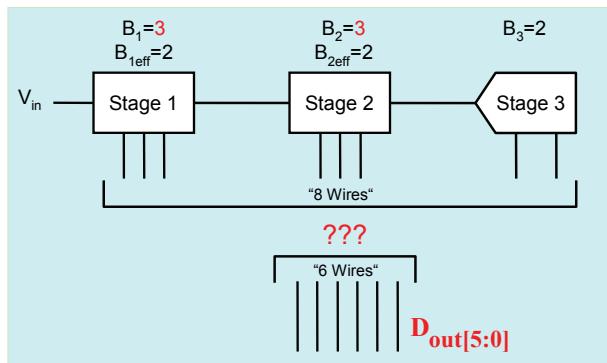
- Only bit shifts

- No arithmetic circuits needed



Combining the Bits Including Redundancy

- Example: Three 2-bit stages, incorporating 1-bit redundancy in stages 1 and 2

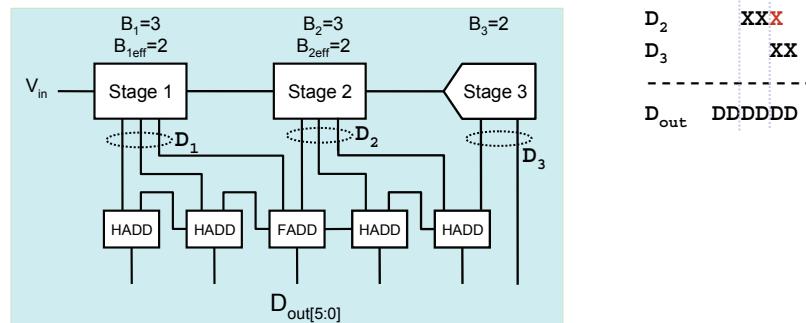


Combining the Bits

$$D_{out} = D_1 + \frac{1}{2^{B1_{eff}}} D_2 + \frac{1}{2^{B1_{eff}} \cdot 2^{B2_{eff}}} D_3$$

$$D_{out} = D_1 + \frac{1}{4} D_2 + \frac{1}{16} D_3$$

- Bits overlap
- Need adders

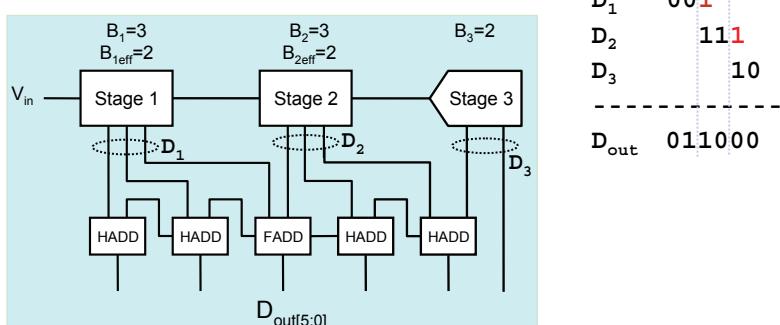


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Pipelined ADCs and More

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Combining the Bits Example

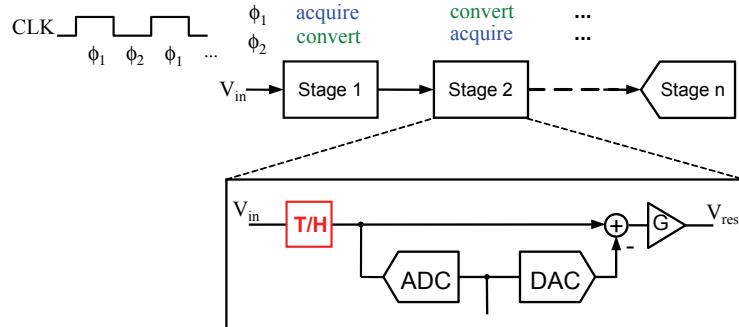


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Pipelined ADCs and More

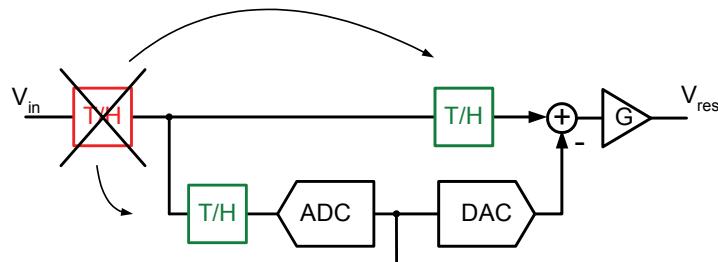
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Pipelined ADC Stage Implementation



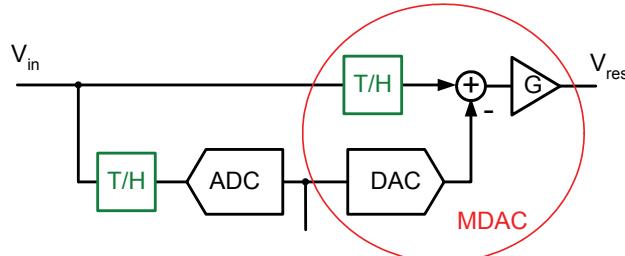
- Each stage needs T/H hold function
- Track phase: Acquire input/residue from previous stage
- Hold phase: sub-ADC decision, compute residue

Stage Implementation



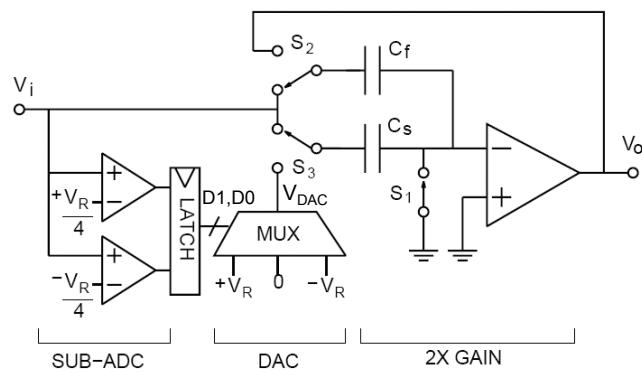
- Usually no dedicated T/H amplifier in each stage
(Except first stage in some cases – why?)
- T/H implicitly contained in stage building blocks

Stage Implementation



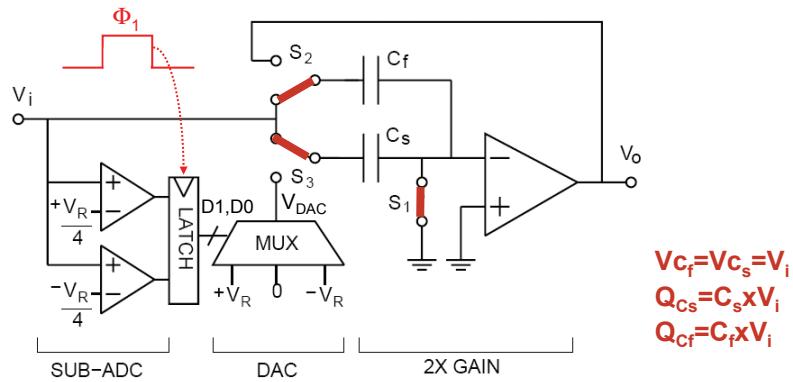
- DAC-subtract-gain function can be lumped into a single switched capacitor circuit
- "MDAC"

1.5-Bit Stage Implementation Example



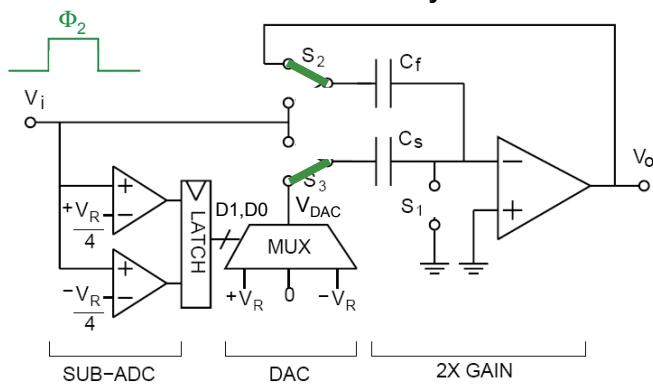
Ref. A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

1.5-Bit Stage Implementation Acquisition Cycle



Ref: A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

1.5-Bit Stage Implementation Conversion Cycle

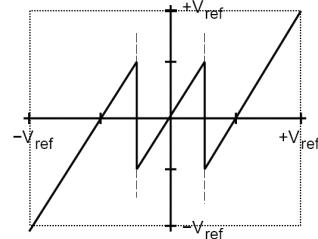


Ref: A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

1.5 Bit Stage Implementation Example

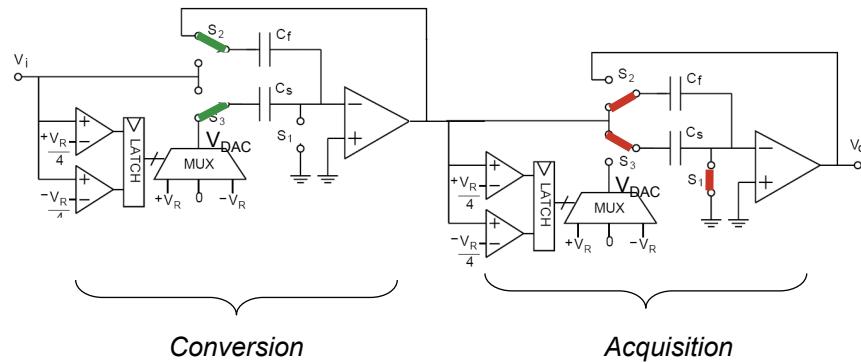
$$V_o = \begin{cases} \left(1 + \frac{C_s}{C_f}\right) V_i - \frac{C_s}{C_f} V_{ref} & \text{if } V_i > V_{ref}/4 \\ \left(1 + \frac{C_s}{C_f}\right) V_i & \text{if } -V_{ref}/4 \leq V_i \leq +V_{ref}/4 \\ \left(1 + \frac{C_s}{C_f}\right) V_i + \frac{C_s}{C_f} V_{ref} & \text{if } V_i < -V_{ref}/4 \end{cases}$$

Note: Interstage gain set by C ratios
 → Accuracy better than 0.1%
 → Up to 10bit level no need for gain calibration



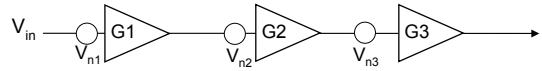
Ref: A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

1.5-Bit Stage Implementation Timing of Stages



Pipelined ADC Stage Power Dissipation & Noise

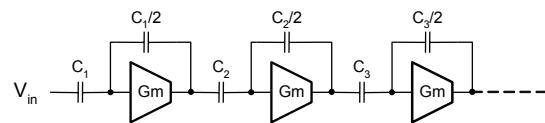
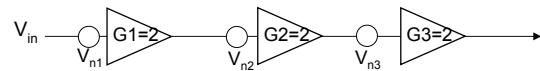
- Typically pipeline ADC noise dominated by inter- stage gain blocks
- Sub-ADC comparator noise translates into comparator threshold uncertainty and is compensated for by redundancy



$$V_{noise}^{in} = \sqrt{V_{n1}^2 + \frac{V_{n2}^2}{GI^2} + \frac{V_{n3}^2}{GI^2G2^2} + \dots}$$

Pipelined ADC Stage Scaling

- Example: Pipeline using 1-bit_{eff} stages

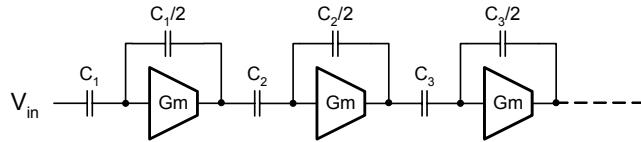


- Total input referred noise power:

$$N_{tot} \propto kT \left[\frac{I}{C_1} + \frac{I}{GI^2C_2} + \frac{I}{GI^2G2^2C_3} + \dots \right]$$

$$N_{tot} \propto kT \left[\frac{I}{C_1} + \frac{I}{4C_2} + \frac{I}{16C_3} + \dots \right]$$

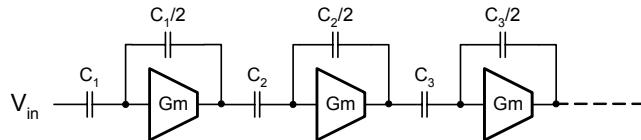
Pipelined ADC Stage Scaling



$$N_{tot} \propto kT \left[\frac{1}{C_1} + \frac{1}{4C_2} + \frac{1}{16C_3} + \dots \right]$$

- If all caps made the same size, backend stages contribute very little noise
- Wasteful power-wise, because:
 - Power $\sim Gm$
 - Speed $\sim Gm/C$
 Fixed speed $\rightarrow Gm/C$ fixed \rightarrow Power $\sim C$

Pipelined ADC Stage Scaling

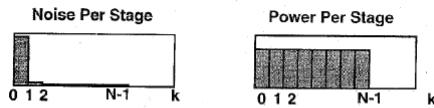


$$N_{tot} \propto kT \left[\frac{1}{C_1} + \frac{1}{4C_2} + \frac{1}{16C_3} + \dots \right]$$

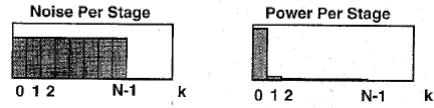
- How about scaling caps down by $G^2=2^2=4x$ per stage?
 - Same amount of noise from every stage
 - All stages contribute significant noise
 - To keep overall noise the same \rightarrow noise/stage must be reduced
 - Power $\sim Gm \sim C$ goes up!

Stage Scaling Example: 2-bit_{eff}/stage

Extreme 1: All Stages the Same Size



Extreme 2: All Stages Contribute the Same Noise

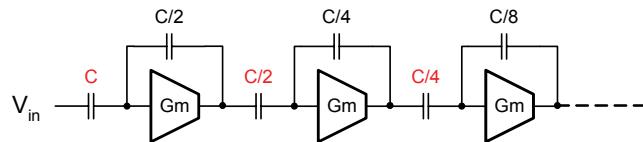


- Optimum capacitor scaling lies approximately midway between these two extremes

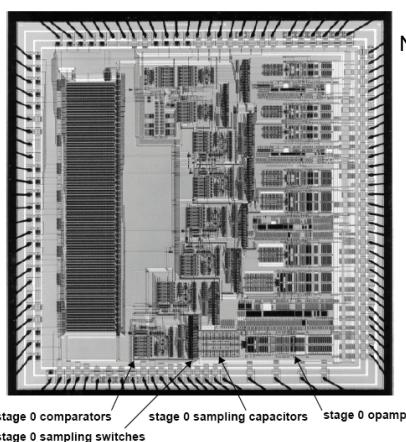
Ref: D. W. Cline, P.R. Gray "A power optimized 13-b 5MSamples/s pipelined analog-to-digital converter in 1.2um CMOS," JSSC 3/1996

Pipeline ADC Stage Scaling

- Power minimum is "shallow"
- Near optimum solution in practice: Scale capacitors by stage gain
- E.g. for effective stage resolution of 1bit (Gain=2):

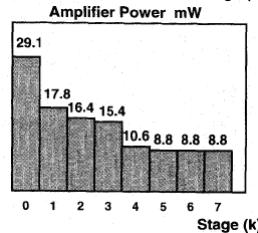
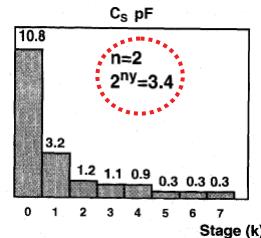


Stage Scaling Example



Note:
Resolution per stage:
→2bits

→G=4



Ref: D. W. Cline, P.R Gray "A power optimized 13-b 5 MSamples/s pipelined analog-to-digital converter in 1.2um CMOS," JSSC 3/1996

How Many Bits Per Stage?

- Many possible architectures
 - E.g. $B_{1\text{eff}}=3, B_{2\text{eff}}=1, \dots$
 - vs. $B_{1\text{eff}}=1, B_{2\text{eff}}=1, B_{3\text{eff}}=1, \dots$
 - Complex optimization problem, fortunately optimum tends to be shallow...
 - Qualitative answer:
 - Maximum speed for given technology
 - Use small resolution-per-stage (large feedback factor)
 - Maximum power efficiency for fixed, "low" speed
 - Try higher resolution stages
 - Can help alleviate matching & noise requirements in stages following the 1st stage
- Ref: Singer VLSI 96, Yang, JSSC 12/01 (14bit ADC w/o calibration)

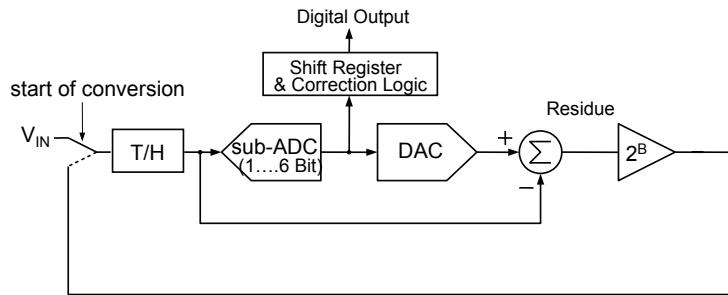
14 & 12-Bit State-of-the-Art Implementations

Reference	Yang (JSSC 12/2001) 0.35μ/3V	Loloee (ESSIRC 2002) 0.18μ/3V
Bits	14	12
Architecture	3-1-1-1-1-1-1-1-3	1-1-1-1-1-1-1-1-1-2
SNR/SFDR	~73dB/88dB	~66dB/75dB
Speed	75MS/s	80MS/s
Power	340mW	260mW

10 & 8-Bit State-of-the-Art Implementations

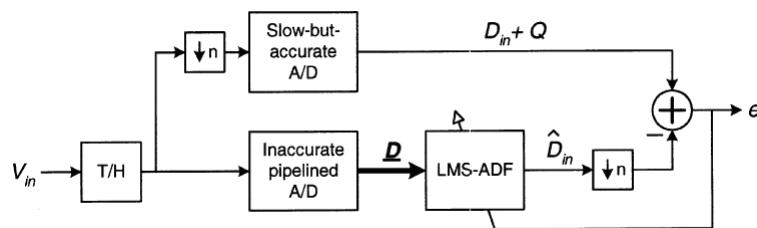
Reference	Yoshioko et al (ISSCC 2005) 0.18μ/1.8V	Kim et al (ISSCC 2005) 0.18μ/1.8V
Bits	10	8
Architecture	1.5bit/stage	2.8 -2.8 - 4
SNR/SFDR	~55dB/66dB	~48dB/56dB
Speed	125MS/s	200MS/s
Power	40mW	30mW

Algorithmic ADC



- Essentially same as pipeline, but a single stage is reused for all partial conversions
- For overall B_{overall} bits \rightarrow need $B_{\text{overall}}/B_{\text{stage}}$ clock cycles per conversion
 - \rightarrow Small area, slow
 - \rightarrow Trades conversion time for area

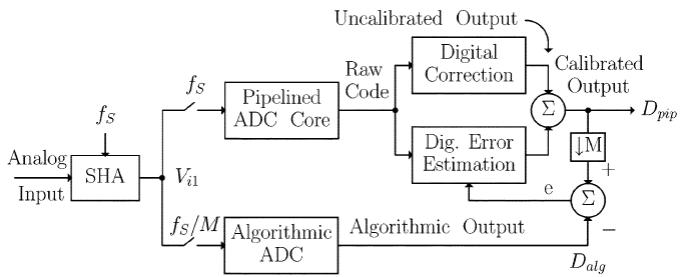
Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters



- Slow, but accurate ADC operates in parallel with pipelined (main) ADC
- Slow ADC samples input signal at a lower sampling rate (f_s/n)
- Difference between corresponding samples for two ADCs (e) used to correct fast ADC digital output via an adaptive digital filter (ADF) based on minimizing the Least-Mean-Squared error

Ref: Y. Chiu, et al, "Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters," IEEE TRANS. CAS, VOL. 51, NO. 1, JANUARY 2004

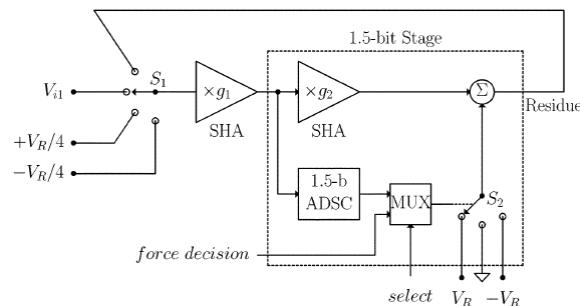
Example: "A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration"



- Pipelined ADC operates at 20Ms/s @ has 1.5bit/stage
- Slow ADC → Algorithmic type operating at 20Ms/32=625ks/s
- Digital correction accounts for bit redundancy
- Digital error estimator → minimizes the mean-squared-error

Ref: X. Wang, P. J. Hurst, S. H. Lewis, "A 12-bit 20-Msample/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

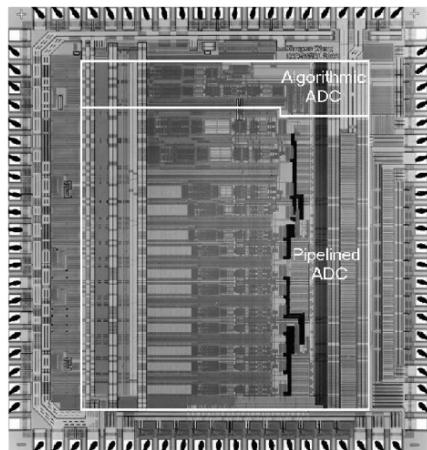
Algorithmic ADC Used for Calibration of Pipelined ADC (continued from previous page)



- Uses replica of pipelined ADC stage
- Requires extra SHA in front to hold residue
- Undergoes a calibration cycle periodically prior to being used to calibrate pipelined ADC

Ref: X. Wang, P. J. Hurst, S. H. Lewis, "A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

12-bit 20-MS/s Pipelined ADC with Digital Background Calibration



Sampling capacitors scaled ($1B_{eff}/stage$):

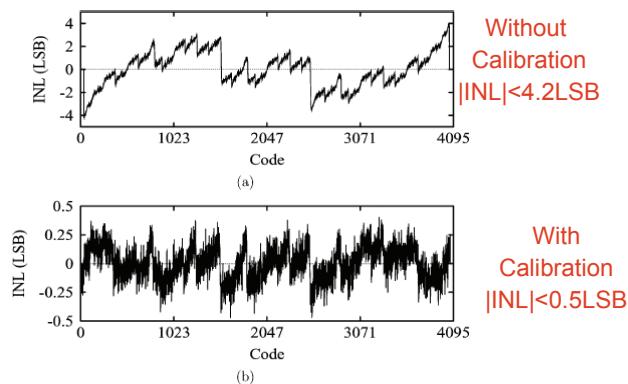
- Input SHA: 6pF
- Pipelined ADC: 2pF, 0.9, 0.4, 0.2, 0.1, 0.1...
- Algorithmic ADC: 0.2pF

Chip area: 13.2mm²

- Does not include digital calibration circuitry estimated ~1.7mm²
- Area of Algorithmic ADC <20%

Ref: X. Wang, P. J. Hurst, S. H. Lewis, "A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

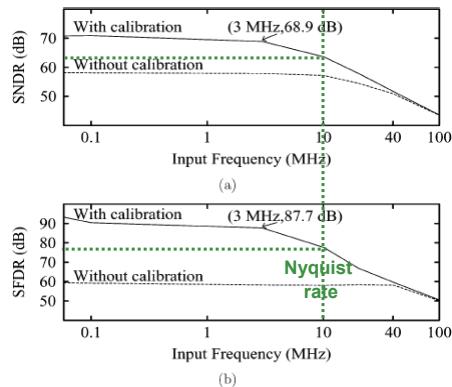
Measurement Results 12-bit 20-MS/s Pipelined ADC with Digital Background Calibration



Ref: X. Wang, P. J. Hurst, S. H. Lewis, "A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Measurement Results

12-bit 20-MS/s Pipelined ADC with Digital Background Calibration



Ref: X. Wang, P. J. Hurst, S. H. Lewis, "A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Measurement Results

12-bit 20-MS/s Pipelined ADC with Digital Background Calibration

PERFORMANCE SUMMARY (3.3 V, 25 °C)

Process	0.35µm 2P4M CMOS	
Sampling rate	20 Msample/s	
Active area	7.5 mm ²	
Full-Scale Input	1.6 Vp-p	
	Without Cal.	With Cal.
Analog Power Diss.	190 mW	226 mW
Total Power Diss.	217 mW	254 mW
Max. INL (Pip. ADC)*	4.21 LSB	0.47 LSB
Max. DNL (Pip. ADC)*	0.60 LSB	0.41 LSB
SNDR (Alg. ADC)*	49.6 dB	59.6 dB
SNDR (Pip. ADC)*	58.2 dB	70.8 dB
SFDR (Pip. ADC)*	59.4 dB	93.3 dB
THD (Pip. ADC) *	-59.4 dB	-92.9 dB
PSRR*	65.0 dB	64.8 dB
CMRR*	73.6 dB	73.4 dB

* $f_{in}=58$ kHz

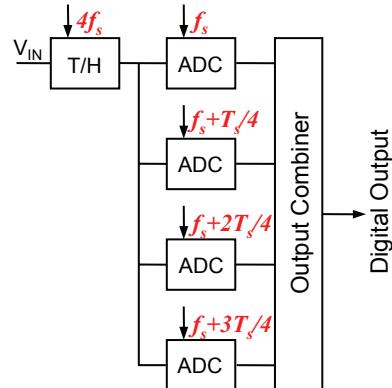
Does not include
digital calibration
circuitry estimated
 $\sim 1.7\text{mm}^2$

Alg. ADC SNDR
dominated by noise

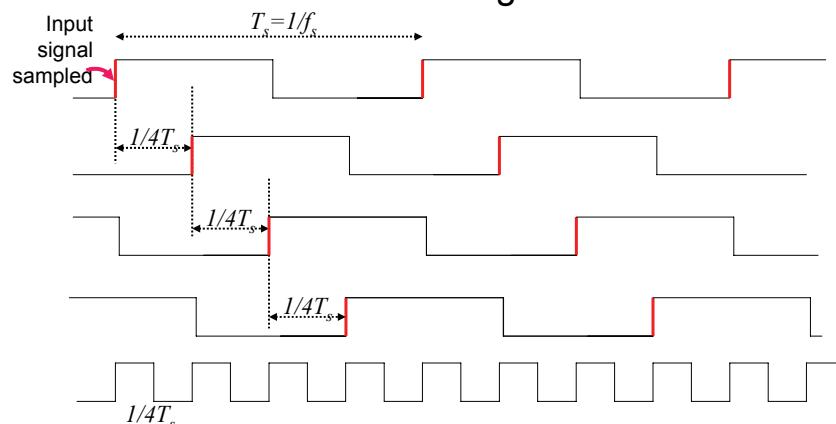
Ref: X. Wang, P. J. Hurst, S. H. Lewis, "A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Time Interleaved Converters

- Example:
 - 4 ADCs operating in parallel at sampling frequency f_s
 - Each ADC converts on one of the 4 possible clock phases
 - Overall sampling frequency = $4f_s$
 - Note T/H has to operate at $4f_s$!
- Extremely fast:
Typically, limited by speed of T/H
- Accuracy limited by mismatch among individual ADCs (timing, offset, gain, ...)



Time Interleaved Converters Timing



- Note: Effective sampling rate $\rightarrow 4f_s$

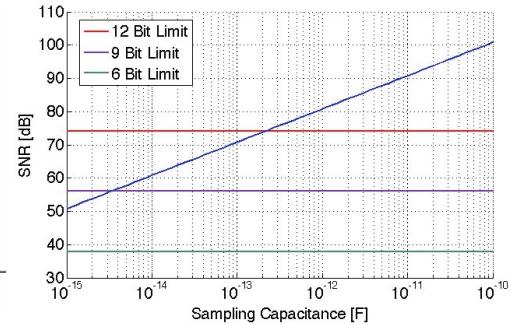
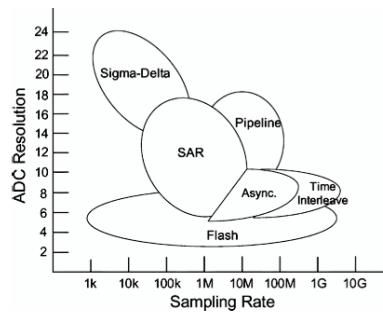
VCO-Based Analog to Digital Conversion

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November 17, 2009

EE247

Picking an ADC

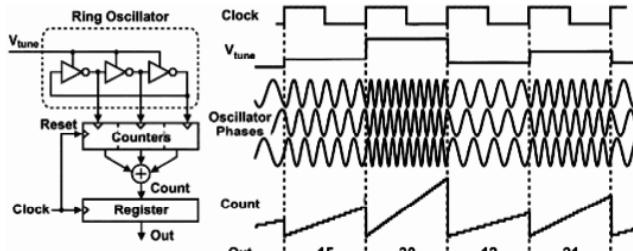
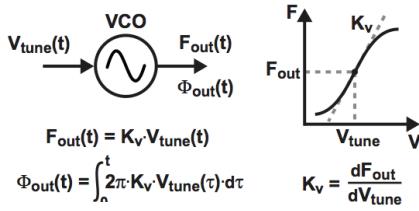


- At 6 bits you are not limited by thermal noise
- Pick an architecture which minimizes other errors
 - Can trade off noise efficiency

[S. Chen, R. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13- μ m CMOS: IEEE J. of Solid-State Circuits, Vol. 41, No. 12, December 2006.]

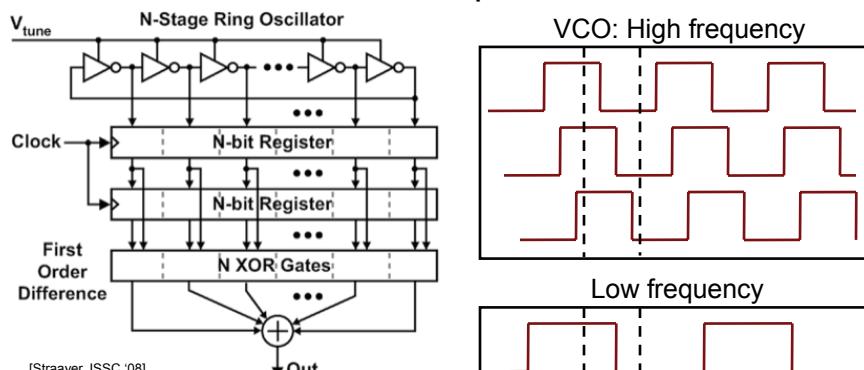
VCO ADC Basics

- Quantizes tuning voltage
 - Performs an integration
 - Two methods
- Method 1: count cycles

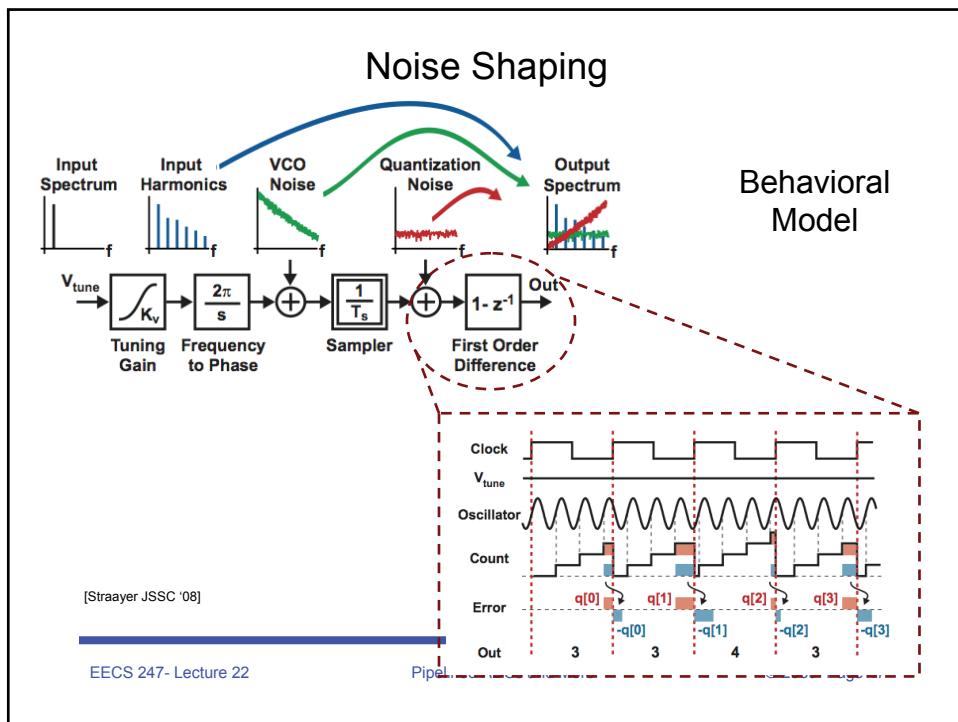


[M. Straayer, Noise Shaping Techniques for Analog and Time to Digital Converters Using Voltage Controlled Oscillator, *Ph.D. Thesis, MIT, 6/ '08.*]
 [M. Straayer, M. Perrott, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time $\Sigma\Delta$ ADC with a 5-bit, 950MS/s VCO-Based Quantizer" IEEE J. of Solid-State Circuits, Vol. 43, No. 4, April 2008.]

Method 2: Sample Phases



- Voltage \rightarrow Frequency
- Frequency \rightarrow Phase
- Phase \rightarrow Frequency



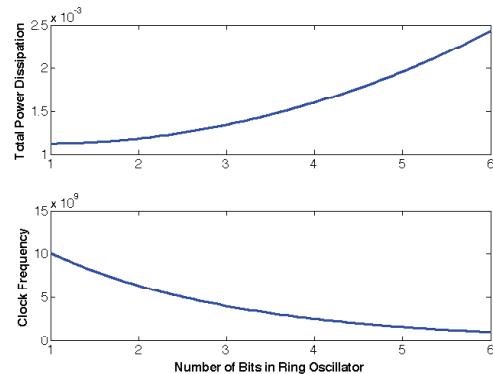
Why Use a VCO ADC?

- ✓ Fully digital
 - Simple
 - Scalable
 - Amplify or integrate
 - Low-energy
 - ✓ Very small area
 - ✓ First-order noise shaping
 - Mismatch whitening and shaping
 - ✓ Oversampling
 - Efficient due to noise shaping
- $\curvearrowleft K_{vco}$ linearity
- Best for lower resolutions

Segmentation

Project: 6-bit, 1GS/s, 90nm process

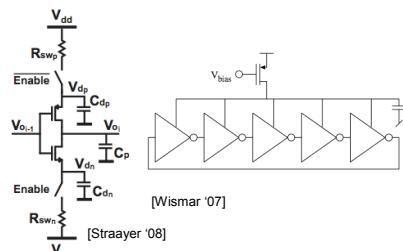
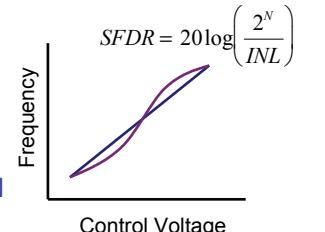
- Number of digital blocks grows as 2^B (B =bits in ring)
- Clock frequency grows as $2^{(N-B)/1.5}$ (N =total resolution)
- Lowest-power solution:
 - Minimize resolution in the ring
 - Maximize oversampling: limited by process



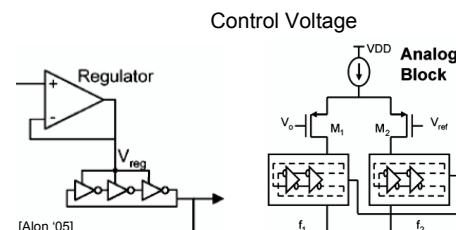
[R. Muller, C. Thakkar]

Tuning the VCO

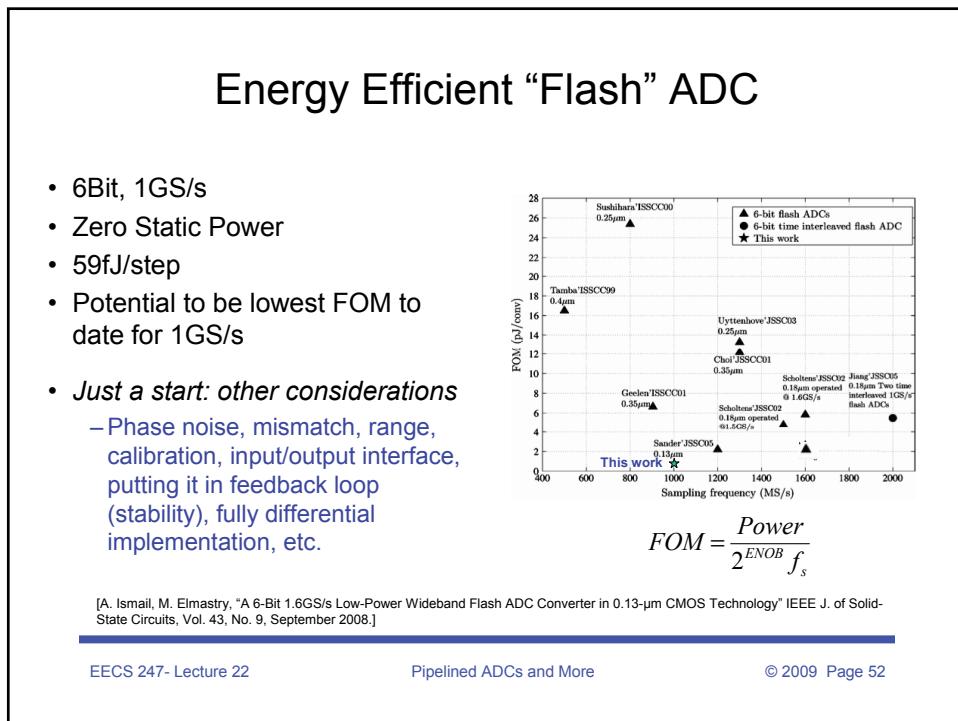
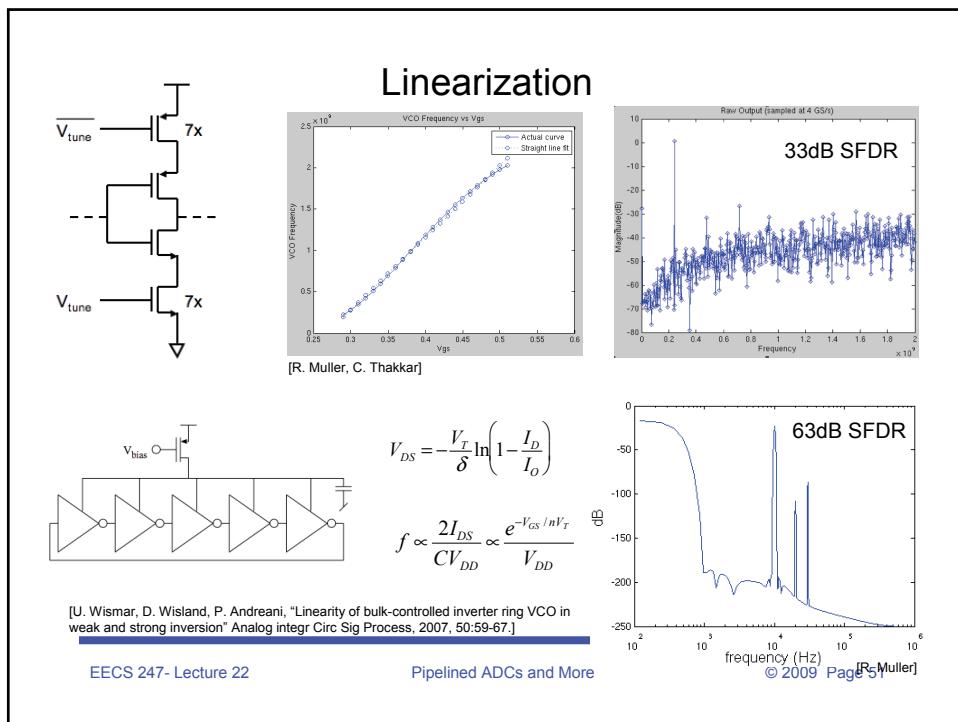
- ADC: INL as voltage deviation
- TDC: INL as frequency deviation
- Multiple ways to tune K_{VCO}
 - ex. Linearization resistance, current control, direct V_{dd} modulation or virtual rail



[E. Alon, V. Stojanovic, M. Horowitz, "Circuits and Techniques for High-Resolution Measurement of On-Chip Power Supply Noise" IEEE J. of Solid-State Circuits, Vol. 40, No. 4, April 2005.]



[J. Xiao, A. Peterchev, J. Zhang, S. Sanders, "A 4-uA Quiescent-Current Dual-Mode Digitally Controlled Buck Converter IC for Cellular Phone Applications" IEEE J. of Solid-State Circuits, Vol. 39, No. 12, December 2004.]



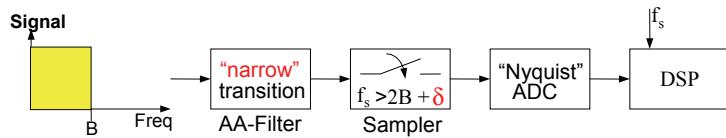
Oversampled ADCs

Analog-to-Digital Converters

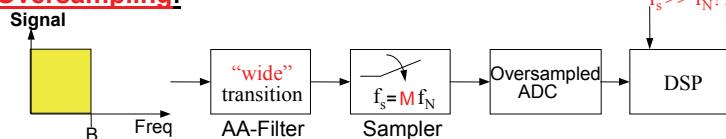
- Two categories:
 - Nyquist rate ADCs $\rightarrow f_{sig}^{max} \sim 0.5xf_{sampling}$
 - Maximum achievable signal bandwidth higher compared to oversampled type
 - Resolution limited to max. ~14bits
 -  Oversampled ADCs $\rightarrow f_{sig}^{max} \ll 0.5xf_{sampling}$
 - Maximum possible signal bandwidth lower compared to nyquist
 - Maximum achievable resolution high (18 to 20bits!)

The Case for Oversampling

Nyquist sampling:

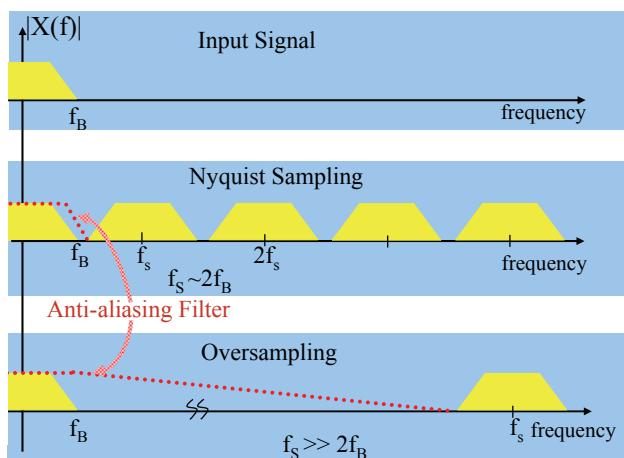


Oversampling:



- Nyquist rate $f_N \sim 2B$
- Oversampling rate $M = f_s/f_N \gg 1$

Nyquist v.s. Oversampled Converters Antialiasing

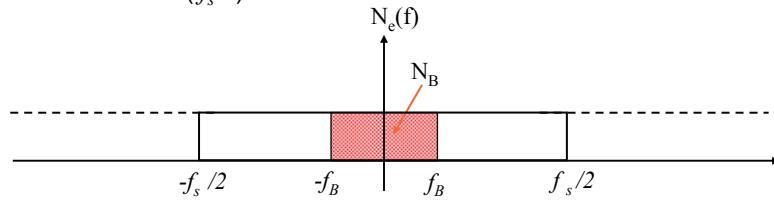


Oversampling Benefits

- No stringent requirements imposed on analog building blocks
- Takes advantage of the availability of low cost, low power digital filtering
- Relaxed transition band requirements for analog anti-aliasing filters
- Reduced baseband quantization noise power
- Allows trading speed for resolution

ADC Converters Baseband Noise

- For a quantizer with quantization step size Δ and sampling rate f_s :
 - Quantization noise power distributed uniformly across Nyquist bandwidth ($f_s/2$)



- Power spectral density:

$$N_e(f) = \frac{\overline{e^2}}{f_s} = \left(\frac{\Delta^2}{12} \right) \frac{1}{f_s}$$

- Noise is distributed over the Nyquist band $-f_s/2$ to $f_s/2$

Oversampled Converters Baseband Noise

$$S_B = \int_{-f_B}^{f_B} N_e(f) df = \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12} \right) \frac{1}{f_s} df$$

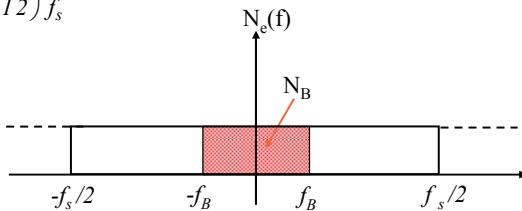
$$= \frac{\Delta^2}{12} \left(\frac{2f_B}{f_s} \right)$$

where for $f_B = f_s / 2$

$$S_{B0} = \frac{\Delta^2}{12}$$

$$S_B = S_{B0} \left(\frac{2f_B}{f_s} \right) = \frac{S_{B0}}{M}$$

where $M = \frac{f_s}{2f_B}$ = oversampling ratio



Oversampled Converters Baseband Noise

$$S_B = S_{B0} \left(\frac{2f_B}{f_s} \right) = \frac{S_{B0}}{M}$$

where $M = \frac{f_s}{2f_B}$ = oversampling ratio

2X increase in M

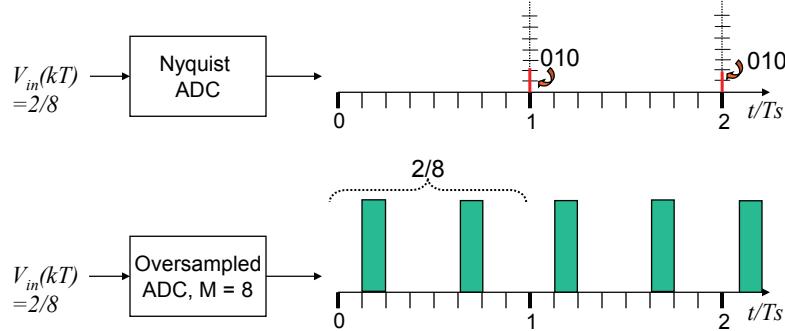
→ 3dB reduction in S_B

→ ½ bit increase in resolution/octave oversampling

To further increase the improvement in resolution:

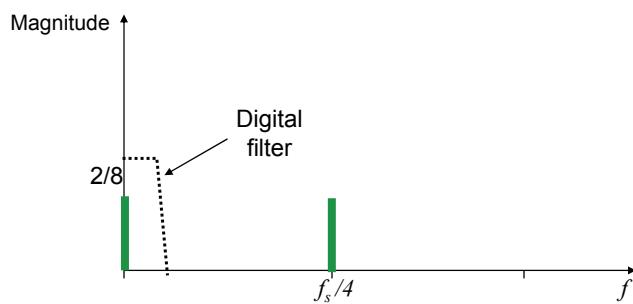
- Embed quantizer in a feedback loop
- Noise shaping (sigma delta modulation)

Pulse-Count Modulation



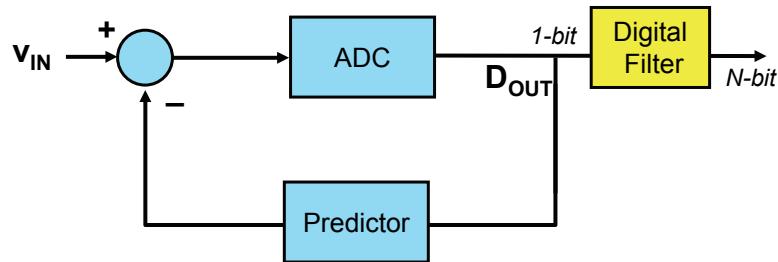
Mean of pulse-count signal approximates analog input!

Pulse-Count Spectrum



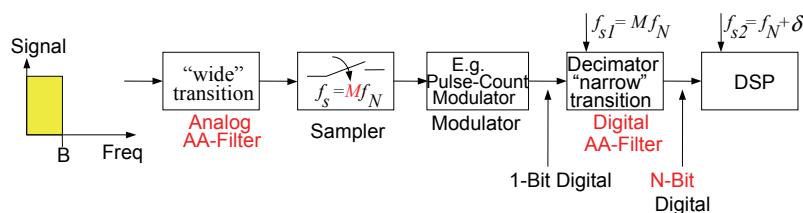
- Signal: low frequencies, $f < B \ll f_s$
- Quantization error: high frequency, $B \dots f_s / 2$
- Separate with low-pass filter!

Oversampled ADC Predictive Coding



- Quantize the difference signal rather than the signal itself
- Smaller input to ADC → Buy dynamic range
- Only works if combined with oversampling
- 1-Bit digital output
- Digital filter computes “average” → N-bit output

Oversampled ADC



Decimator:

- Digital (low-pass) filter
- Removes quantization error for $f > B$
- Provides anti-alias filtering for DSP
- Narrow transition band, high-order
- 1-Bit input, N-Bit output (essentially computes “average”)