

EE247

Lecture 16

- **D/A Converters (continued)**
 - Self calibration techniques
 - Current copiers (last lecture)
 - Dynamic element matching
 - DAC reconstruction filter
- **ADC Converters**
 - Sampling
 - Sampling switch considerations
 - Thermal noise due to switch resistance
 - Clock jitter related non-idealities
 - Sampling switch bandwidth limitations
 - Switch induced distortion
 - Sampling switch conductance dependence on input voltage
 - Clock voltage boosters

A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE,
HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

Called:
Current Copier

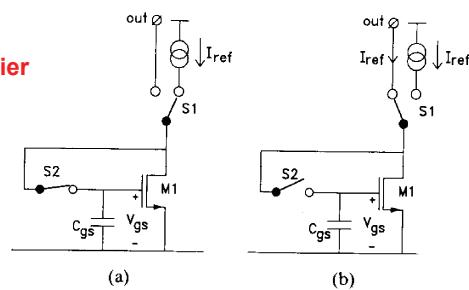
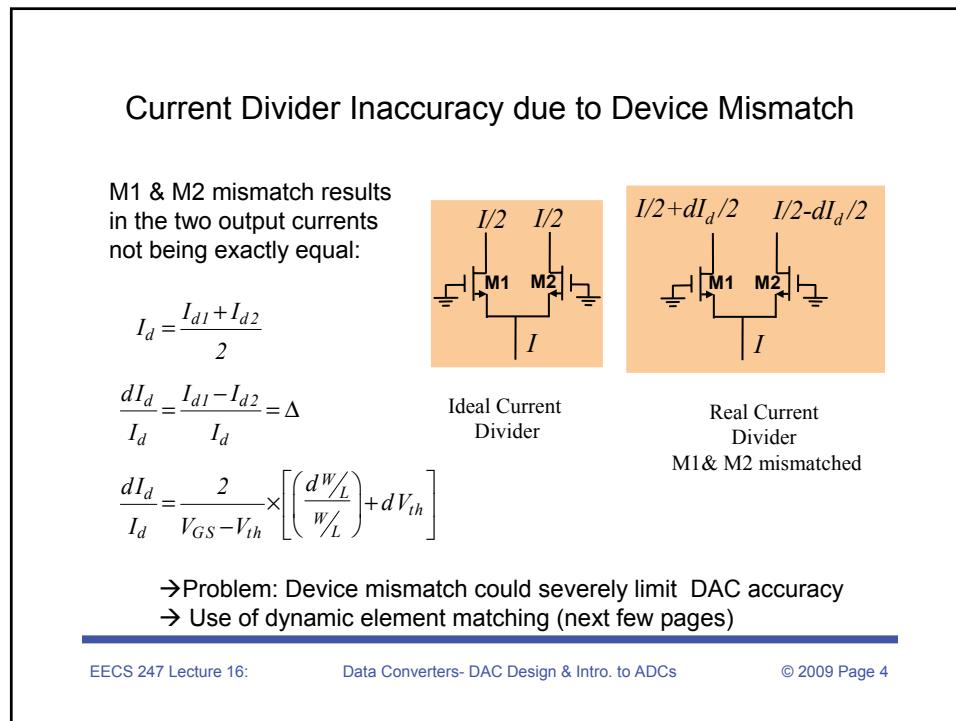
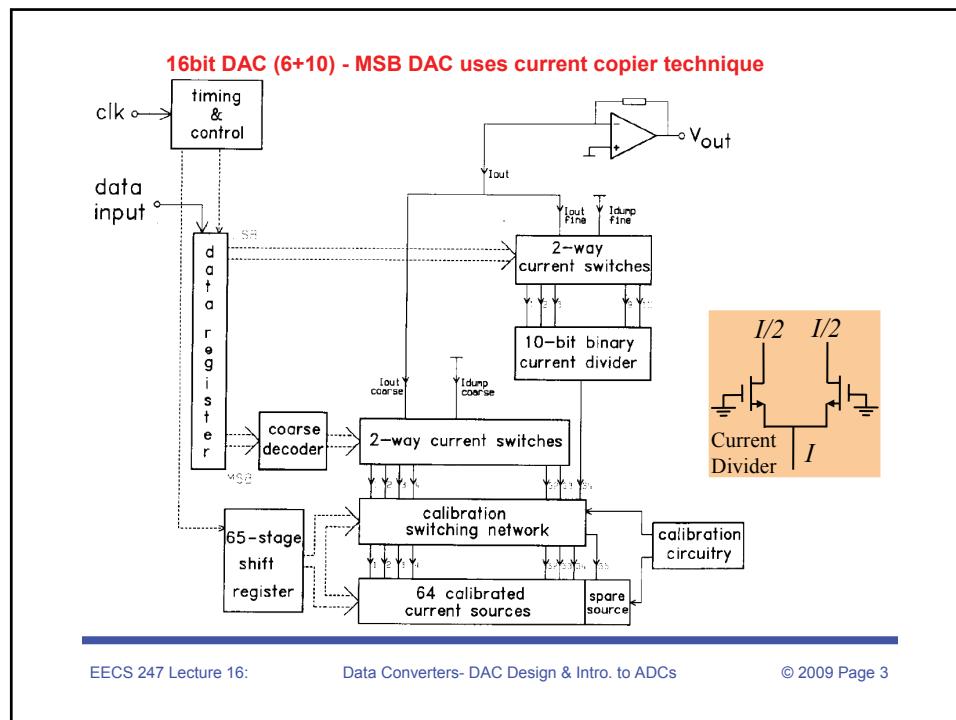
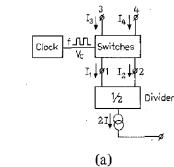


Fig. 2. Calibration principle. (a) Calibration. (b) Operation.

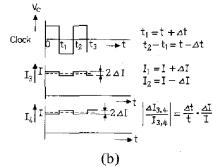


Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE



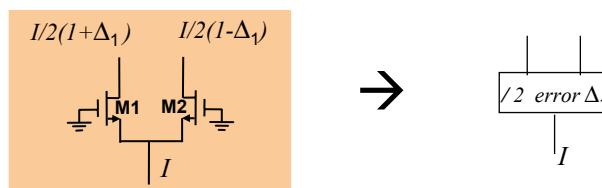
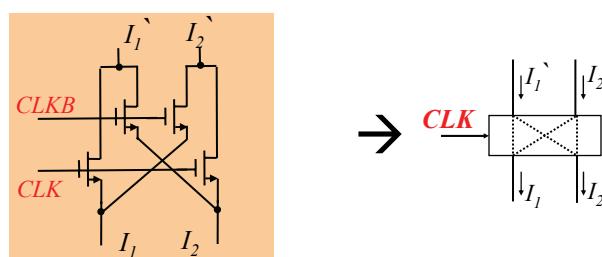
(a)



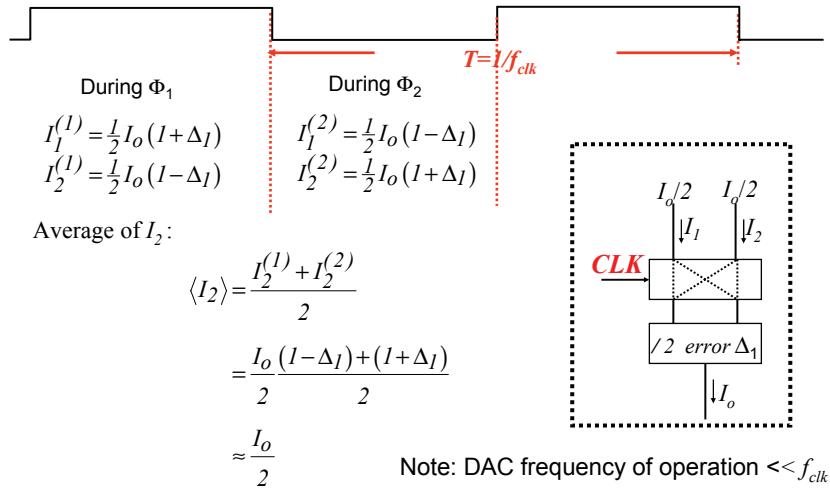
(b)

Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.

Dynamic Element Matching Block Diagram Representation



Dynamic Element Matching



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Note:
For optimum current division accuracy \rightarrow clock frequency is divided by two for each finer division
Problem: DAC frequency of operation drastically reduced

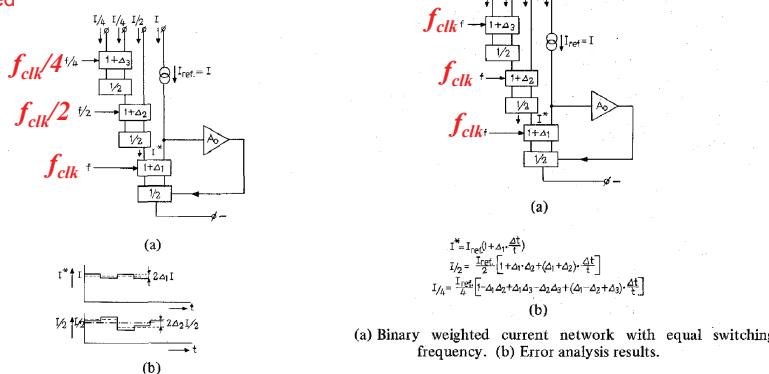


Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Time dependence of currents flowing in the first and second divider stage.

Note: What if the same clock frequency is used?

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Dynamic Element Matching

During Φ_1

$$I_1^{(1)} = \frac{1}{2} I_o (1 + \Delta_1)$$

$$I_2^{(1)} = \frac{1}{2} I_o (1 - \Delta_1)$$

$$I_3^{(1)} = \frac{1}{2} I_1^{(1)} (1 + \Delta_2)$$

$$= \frac{1}{4} I_o (1 + \Delta_1)(1 + \Delta_2)$$

$$\langle I_3 \rangle = \frac{I_3^{(1)} + I_3^{(2)}}{2}$$

$$= \frac{I_o (1 + \Delta_1)(1 + \Delta_2) + (1 - \Delta_1)(1 - \Delta_2)}{4}$$

$$= \frac{I_o}{4} (1 + \Delta_1 \Delta_2)$$

E.g. $\Delta_1 = \Delta_2 = 1\% \rightarrow$ matching error is $(1\%)^2 = 0.01\%$

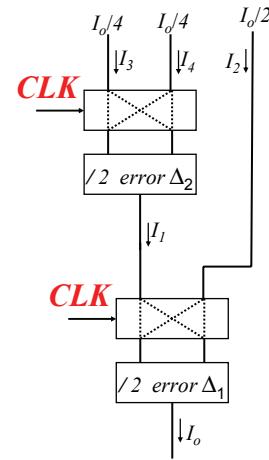
During Φ_2

$$I_1^{(2)} = \frac{1}{2} I_o (1 - \Delta_1)$$

$$I_2^{(2)} = \frac{1}{2} I_o (1 + \Delta_1)$$

$$I_3^{(2)} = \frac{1}{2} I_1^{(2)} (1 - \Delta_2)$$

$$= \frac{1}{4} I_o (1 - \Delta_1)(1 - \Delta_2)$$



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IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 6, DECEMBER 1976

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Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

- Bipolar 12-bit DAC using dynamic element matching built in 1976
- Element matching clock frequency 100kHz
- INL <0.25LSB!

12-BIT D/A TEST CHIP

D/A NETWORK DATA	
Resolution :	12 bit
Accuracy :	$\leq \frac{1}{4}$ L.S.B. or $5 \cdot 10^{-5}$ (linearity)
Output current :	2 mA
Temp. Coeff. of output current :	5 ppm/°C
Voltage Coeff. of output current :	1 ppm/V
Chip size :	2.5 x 2.5 mm
Max. clock freq. for dynamic matching :	100 kHz
Power supply :	-15V

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ISSCC 2004 / SESSION 20 / DIGITAL-TO-ANALOG CONVERTERS / 20.1

20.1 A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications

Bernd Schafferer and Richard Adams

Example: State-of-the-Art current steering DAC

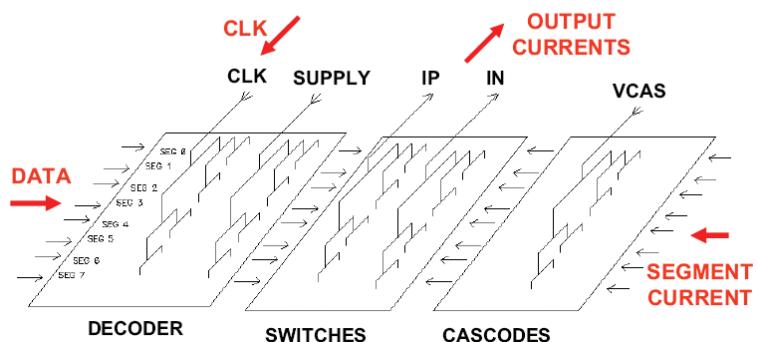
Segmented:
6bit unit-element
8bit binary

Max Sample Frequency	1.4	GSPS
Resolution	14	Bit
DNL	+/- 0.8	LSB
INL	+/- 2.1	LSB
SFDR @ 1.0 GSPS	> 60	dB
IMD @ 1.0 GSPS	> 64	dBc
NSD @ f _{out} = 400MHz	-155	dBm/Hz
Power (Core) @ 1.4GSPS	200	mW
Power(Total) @ 1.4GSPS	400	mW
Area (Core)	0.8	mm ²
Area (Chip)	6.25	mm ²

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20.1 A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications

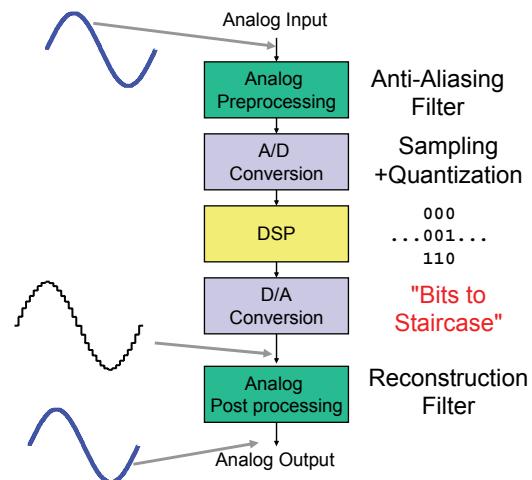
Layout Tree Structures



DAC In the Big Picture

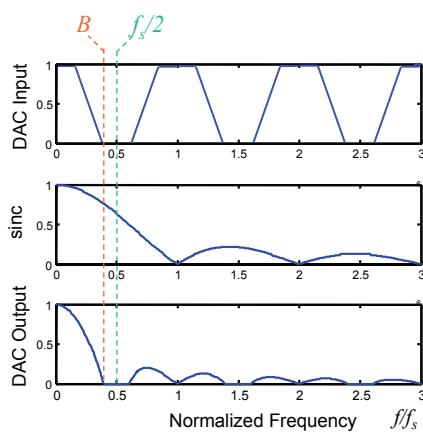
- Learned to build DACs
 - Convert the incoming digital signal to analog
- DAC output \rightarrow staircase form
- Some applications require filtering (smoothing) of DAC output
 \rightarrow reconstruction filter

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DAC Reconstruction Filter

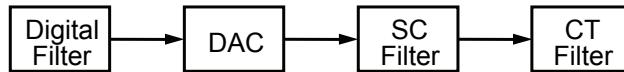
- Need for and requirements depend on application
- Tasks:
 - Correct for sinc droop
 - Remove “aliases” (stair-case approximation)



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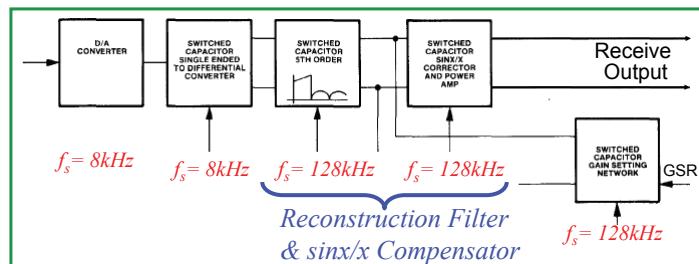
Reconstruction Filter Options

Reconstruction Filters



- Reconstruction filter options:
 - Continuous-time filter only
 - CT + SC filter
- SC filter possible only in combination with oversampling (signal bandwidth B << $f_s/2$)
- Digital filter
 - Band limits the input signal → prevent aliasing
 - Could also provide high-frequency pre-emphasis to compensate in-band $\sin x/x$ amplitude droop associated with the inherent DAC S/H function

DAC Reconstruction Filter Example: Voice-Band CODEC Receive Path



Note: $f_{sig}^{max} = 3.4\text{kHz}$
 $f_s^{DAC} = 8\text{kHz}$
 $\rightarrow \sin(\pi f_{sig}^{max} x T_s) / (\pi f_{sig}^{max} x T_s)$
 $= -2.75 \text{ dB droop due to DAC sinx/x shape}$

Ref: D. Senderowicz et. al, "A Family of Differential NMOS Analog Circuits for PCM Codec Filter Chip," *IEEE Journal of Solid-State Circuits*, Vol.-SC-17, No. 6, pp.1014-1023, Dec. 1982.

Summary D/A Converter

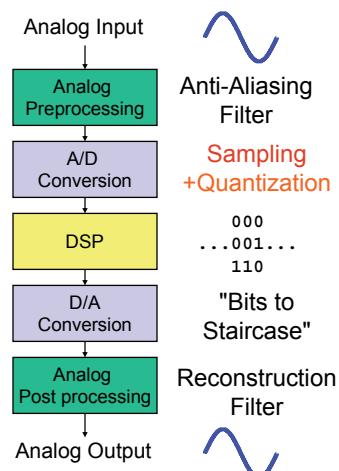
- D/A architecture
 - Unit element – complexity proportional to 2^B - excellent DNL
 - Binary weighted- complexity proportional to B - poor DNL
 - Segmented- unit element MSB(B_1)+ binary weighted LSB(B_2)
→ Complexity proportional $((2^{B_1}-1) + B_2)$ -DNL compromise between the two
- Static performance
 - Component matching
- Dynamic performance
 - Time constants, Glitches
- DAC improvement techniques
 - Symmetrical switching rather than sequential switching
 - Current source self calibration
 - Dynamic element matching
- Depending on the application, reconstruction filter may be needed

What Next?

• ADC Converters:

- Need to build circuits that "sample"

- Need to build circuits for amplitude quantization



Analog-to-Digital Converters

- Two categories:

- Nyquist rate ADCs → $f_{sig}^{max} \sim 0.5xf_{sampling}$
 - Maximum achievable signal bandwidth higher compared to oversampled type
 - Resolution limited to max. 12-14bits
- Oversampled ADCs → $f_{sig}^{max} \ll 0.5xf_{sampling}$
 - Maximum achievable signal bandwidth significantly lower compared to nyquist
 - Maximum achievable resolution high (18 to 20bits!)

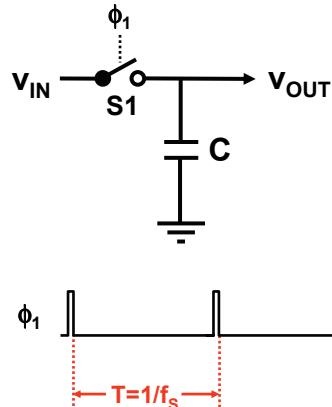
MOS Sampling Circuits

Ideal Sampling

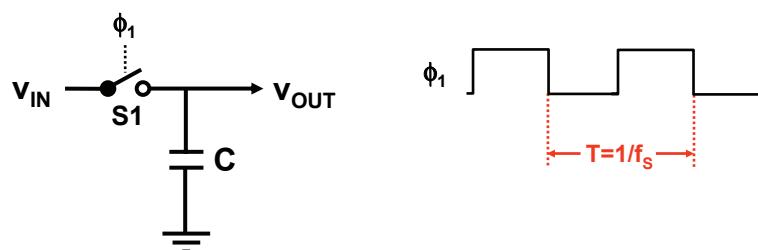
- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage v_{IN} onto the capacitor C

→ Output Dirac-like pulses with amplitude equal to V_{IN} at the time of sampling

- In practice not realizable!

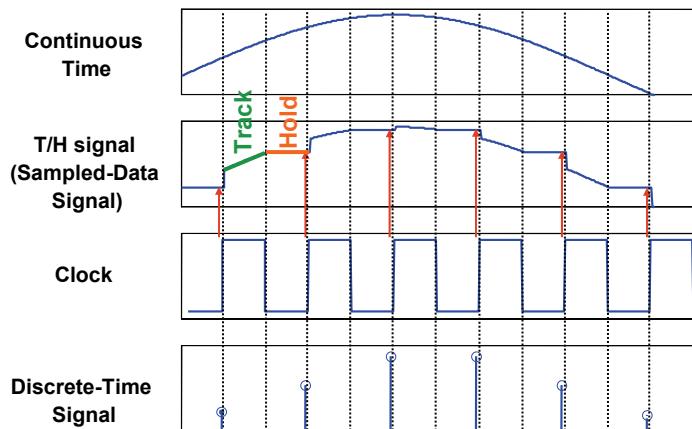


Ideal Track & Hold Sampling

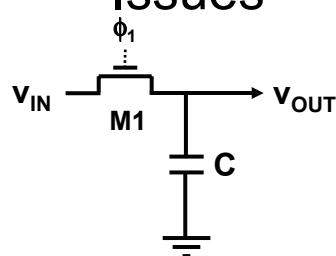


- V_{out} tracks input for $\frac{1}{2}$ clock cycle when switch is closed
- Ideally acquires exact value of V_{in} at the instant the switch opens
- "Track and Hold" (T/H) (often called Sample & Hold!)

Ideal T/H Sampling

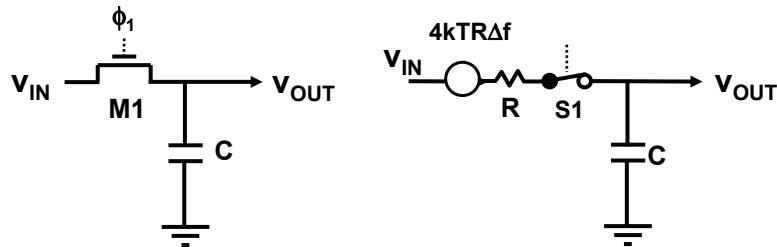


Practical Sampling Issues



- Switch induced noise due to M1 finite channel resistance
- Clock jitter
- Finite R_{sw} → limited bandwidth → finite acquisition time
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection & clock feedthrough

Sampling Circuit kT/C Noise



- Switch resistance & sampling capacitor form a low-pass filter
- Noise associated with the switch resistance results in → Total noise variance = kT/C @ the output (see noise analysis in Lecture 1)
- In high resolution ADCs kT/C noise at times dominates overall minimum signal handling capability (power dissipation considerations).

Sampling Network kT/C Noise

For ADCs sampling capacitor size is usually chosen based on having thermal noise smaller or equal or at times slightly larger compared to quantization noise:
Assumption: → Nyquist rate ADC

For a Nyquist rate ADC : Total quantization noise power $\approx \frac{\Delta^2}{12}$

Choose C such that thermal noise level is less (or equal) than Q noise

$$\frac{k_B T}{C} \leq \frac{\Delta^2}{12}$$

$$\rightarrow C \geq 12k_B T \left(\frac{2^B - 1}{V_{FS}} \right)^2$$

$$\rightarrow C \geq 12k_B T \times \frac{2^{2B}}{V_{FS}^2}$$

Sampling Network kT/C Noise

$$C \geq 12k_B T \frac{2^{2B}}{V_{FS}^2}$$

Required C_{min} as a Function of ADC Resolution		
B	C_{min} ($V_{FS} = 1V$)	C_{min} ($V_{FS} = 0.5V$)
8	0.003 pF	0.012 pF
12	0.8 pF	2.4 pF
14	13 pF	52 pF
16	206 pF	824 pF
20	52,800 pF	211,200 pF

The large area required for C → limit highest achievable resolution for Nyquist rate ADCs

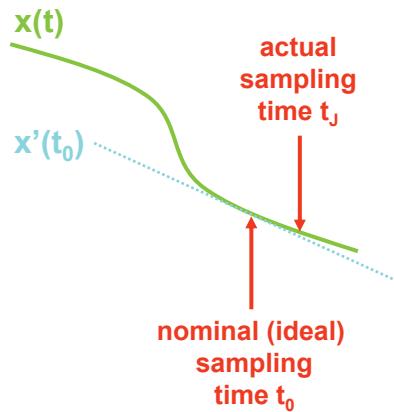
Oversampling results in reduction of required value for C (will be covered in oversampled converter lectures)

Clock Jitter

- So far : clock signal controls sampling instants – which we assumed to be precisely equi-distant in time (period T)
- Real clock generator → some level of variability
- Variability in T causes errors
 - "Aperture Uncertainty" or "Aperture Jitter"
- What is the effect of clock jitter on ADC performance?

Clock Jitter

- Sampling jitter adds an error voltage proportional to the product of $(t_J - t_0)$ and the derivative of the input signal at the sampling instant

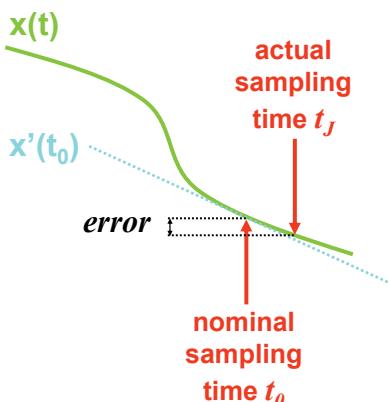


Clock Jitter

- The error voltage is

$$e = x'(t_0)(t_J - t_0)$$

- Does jitter matter when sampling dc signals ($x'(t_0) = 0$)?



Effect of Clock Jitter on Sampling of a Sinusoidal Signal

Sinusoidal input

$$\begin{array}{ll} \text{Amplitude: } & A \\ \text{Frequency: } & f_x \\ \text{Jitter: } & dt \end{array}$$

$$x(t) = A \sin(2\pi f_x t)$$

$$x'(t) = 2\pi f_x A \cos(2\pi f_x t)$$

$$|x'(t)|_{max} \leq 2\pi f_x A$$

Then:

$$|e(t)| \leq |x'(t)|_{max} dt$$

$$|e(t)| \leq 2\pi f_x A dt$$

Worst case

$$A = \frac{A_{FS}}{2} \quad f_x = \frac{f_s}{2}$$

$$|e(t)| \ll \frac{\Delta}{2} \equiv \frac{A_{FS}}{2^{B+1}}$$

$$dt \ll \frac{1}{2^B \pi f_s}$$

# of Bits	f_s	$dt \ll$
12	1 MHz	78 ps
16	20 MHz	0.24 ps
12	1000 MHz	0.07 ps

Statistical Jitter Analysis

- The worst case looks pretty stringent ... what about the “average”?
- Let’s calculate the mean squared jitter error (variance)
- If we’re sampling a sinusoidal signal
 $x(t) = A \sin(2\pi f_x t)$,
 then
 - $x'(t) = 2\pi f_x A \cos(2\pi f_x t)$
 - $E\{[x'(t)]^2\} = 2\pi^2 f_x^2 A^2$
- Assume the jitter has variance $E\{(t_j - t_0)^2\} = \tau^2$

Statistical Jitter Analysis

- If $x'(t)$ and the jitter are independent
 - $E\{[x'(t)(t_j - t_0)]^2\} = E\{[x'(t)]^2\} E\{(t_j - t_0)^2\}$

- Hence, the jitter error power is

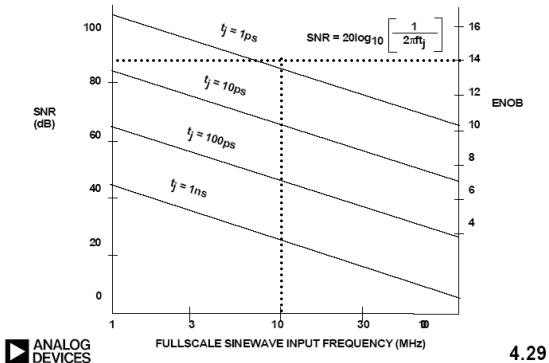
$$E\{e^2\} = 2\pi^2 f_x^2 A^2 \tau^2$$

- If the jitter is uncorrelated from sample to sample, this “jitter noise” is white

Statistical Jitter Analysis

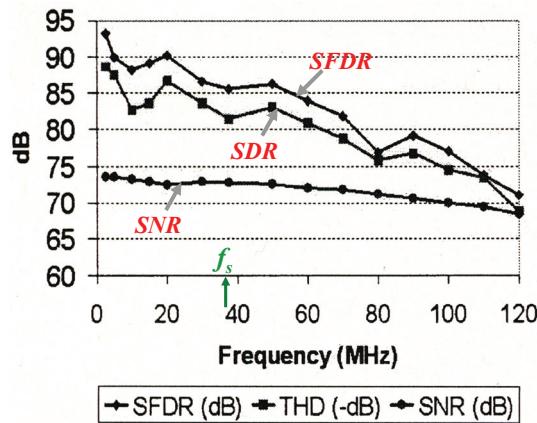
SNR DUE TO APERTURE AND SAMPLING CLOCK JITTER

$$\begin{aligned} DR_{\text{jitter}} &= \frac{A^2 / 2}{2\pi^2 f_x^2 A^2 \tau^2} \\ &= \frac{1}{2\pi^2 f_x^2 \tau^2} \\ &= -20 \log_{10}(2\pi f_x \tau) \end{aligned}$$



4.29

Example: ADC Spectral Tests



Ref: W. Yang et al., "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. of Solid-State Circuits*, Dec. 2001

Summary

Effect of Clock Jitter on ADC Performance

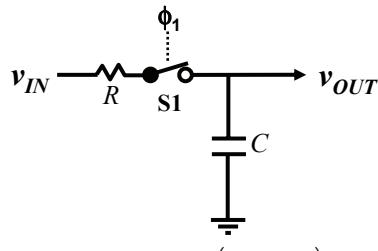
- In cases where clock signal is provided from off-chip → have to choose a source with low enough jitter
- On-chip precautions to keep the clock jitter less than single-digit pico-second :
 - Separate supplies as much as possible
 - Separate analog and digital clocks
 - Short inverter chains between clock source and destination
- Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
 - RMS noise proportional to input signal frequency
 - RMS noise proportional to input signal amplitude
- In cases where clock jitter limits the dynamic range, it's easy to tell, but may be difficult to fix...

Sampling Acquisition Bandwidth

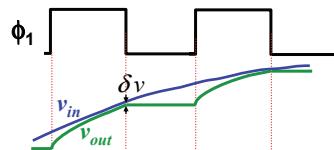
- The resistance R of switch S1 turns the sampling network into a lowpass filter with finite time constant:

$$\tau = RC$$

- Assuming V_{in} is constant or changing slowly during the sampling period and C is initially discharged
- Need to allow enough time for the output to settle to less than 1 ADC LSB \rightarrow determines minimum duration for ϕ_1 or maximum clock frequency



$$v_{out}(t) = v_{in} \left(1 - e^{-t/\tau}\right)$$



Sampling: Effect of Switch On-Resistance

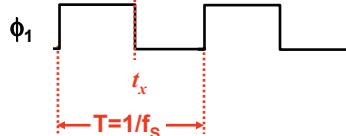
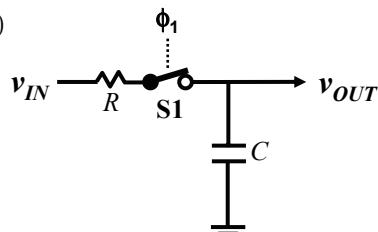
$$V_{in}^{tx} - V_{out}^{tx} \ll \Delta \text{ since } V_{out} = V_{in} \left(1 - e^{-t/\tau}\right)$$

$$\rightarrow V_{in} e^{-T_s/2\tau} \ll \Delta \text{ or } \tau \ll \frac{T_s}{2} \ln\left(\frac{V_{in}}{\Delta}\right)$$

Worst Case: $V_{in} = V_{FS}$

$$\tau \ll \frac{T_s}{2} \frac{1}{\ln(2^B - 1)} \approx \frac{0.72 \times T_s}{B}$$

$$R \ll \frac{1}{2f_s C} \frac{1}{\ln(2^B - 1)} \approx \frac{0.72}{B f_s C}$$



Example:

$$B = 14, \quad C = 13pF, \quad f_s = 100MHz$$

$$T_s/\tau \gg 19.4, \text{ or } 10\tau \ll T_s/2 \rightarrow R \ll 40 \Omega$$

Switch On-Resistance

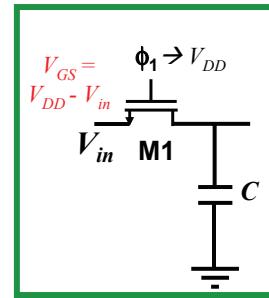
Switch → MOS operating in triode mode:

$$I_{D(\text{triode})} = \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS}, \quad \frac{1}{R_{ON}} \equiv \left. \frac{dI_{D(\text{triode})}}{dV_{DS}} \right|_{V_{DS} \rightarrow 0}$$

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{DD} - V_{th} - V_{in})}$$

Let us call $R @ V_{in}=0$ R_o then $R_o = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{DD} - V_{th})}$

$$R_{ON} = \frac{R_o}{1 - \frac{V_{in}}{V_{DD} - V_{th}}}$$



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Sampling Distortion

Simulated 10-Bit ADC &

$$T_s/2 = 5\tau$$

$$V_{DD} - V_{th} = 2V$$

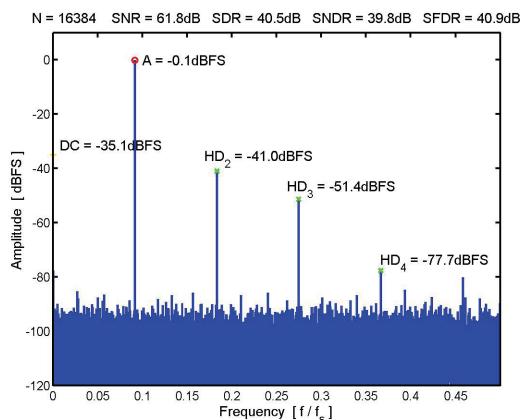
$$V_{FS} = 1V$$

Sampling Switch modeled:

$$v_{out} = v_{in} \left(I - e^{-\frac{T}{2\tau} \left(1 - \frac{V_{in}}{V_{DD} - V_{th}} \right)} \right)$$

→ Results in

$$HD2 = -41\text{dBFS} \text{ &} HD3 = -51.4\text{dBFS}$$



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Sampling Distortion

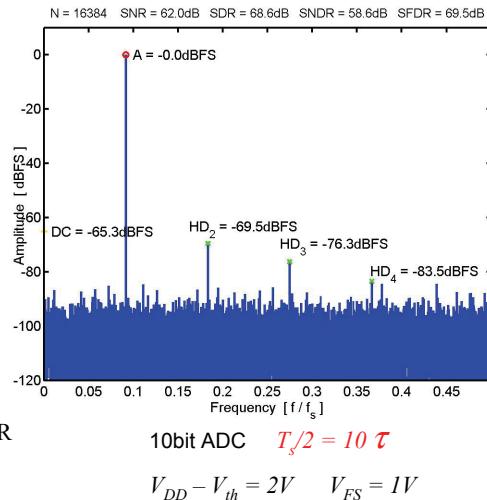
Doubling sampling time (or $\frac{1}{2}$ time constant)

Results in:

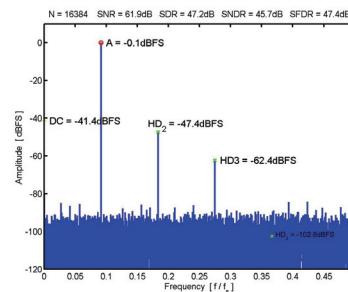
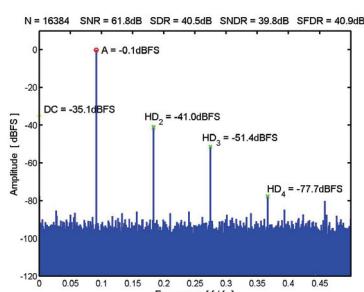
HD2 improved from -41dBFS to -70dBFS ~ 30 dB

HD3 improved from -51.4dBFS to -76.3dBFS ~ 25 dB

Allowing enough time for the sampling network settling \rightarrow
Reduces distortion due to switch R non-linear behavior to a tolerable level



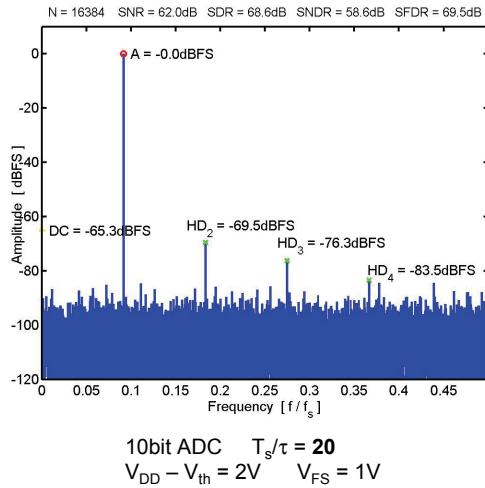
Sampling Distortion Effect of Supply Voltage



- Effect of higher supply voltage on sampling distortion
 - HD3 decreased by $(V_{DD1}/V_{DD2})^2$
 - HD2 decreased by (V_{DD1}/V_{DD2})

Sampling Distortion

- SFDR → sensitive to sampling distortion - improve linearity by:
 - Larger V_{DD}/V_{FS}
 - Higher sampling bandwidth
- Solutions:
 - Overdesign → Larger switches
 - Issue:
 - Increased switch charge injection
 - Increased nonlinear S & D junction cap.
 - Maximize V_{DD}/V_{FS}
 - Decreased dynamic range if V_{DD} const.
 - Complementary switch
 - Constant & max. $V_{GS} \neq f(V_{in})$



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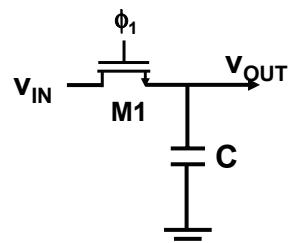
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Practical Sampling Summary So Far!

- kT/C noise

$$C \geq 12k_B T \frac{2^{2B}}{V_{FS}^2}$$
- Finite R_{sw} → limited bandwidth

$$R \ll \frac{0.72}{B f_s C}$$



- $g_{sw} = f(V_{in})$ → distortion

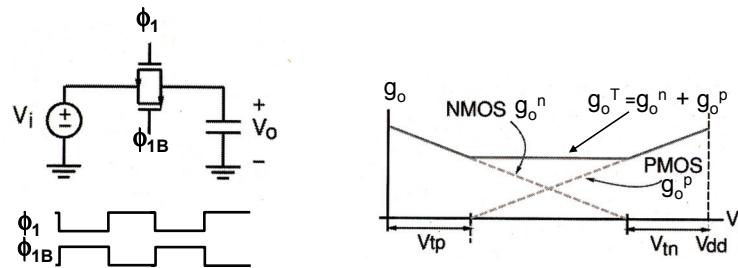
$$g_{ON} = g_o \left(1 - \frac{V_{in}}{V_{DD} - V_{th}} \right) \quad \text{for} \quad g_o = \mu C_{ox} \frac{W}{L} (V_{DD} - V_{th})$$

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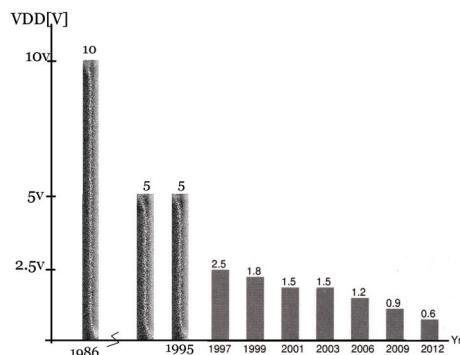
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Sampling: Use of Complementary Switches



- Complementary n & p switch advantages:
 - ✓ Increase in the overall conductance
 - ✓ Linearize the switch conductance for the range $|V_{th}^p| < V_{in} < V_{dd} - |V_{th}^n|$

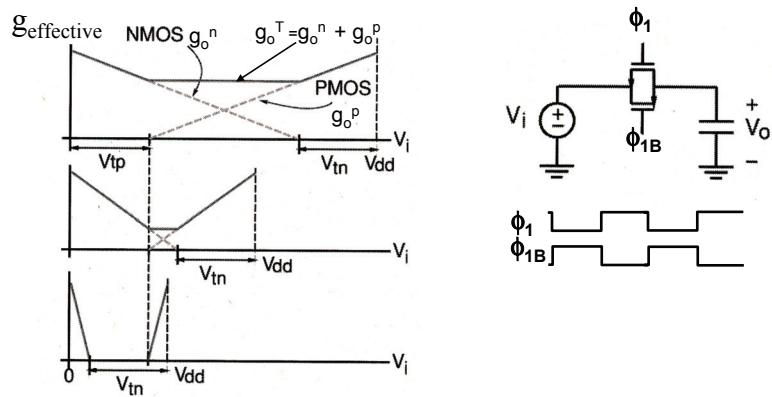
Complementary Switch Issues Supply Voltage Evolution



- Supply voltage has scaled down with technology scaling
- Threshold voltages do not scale accordingly

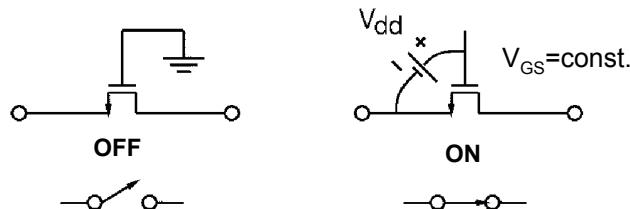
Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

Complementary Switch Effect of Supply Voltage Scaling



- As supply voltage scales down input voltage range for constant g_o shrinks
→ Complementary switch not effective when V_{DD} becomes comparable to $2xV_{th}$

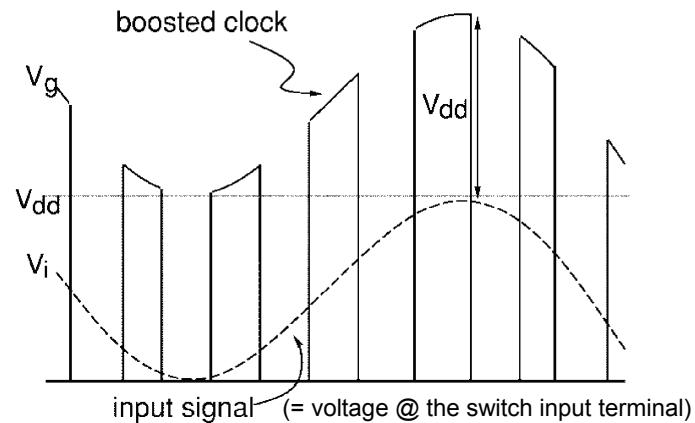
Boosted & Constant V_{GS} Sampling



- Gate voltage V_{GS} =low
 - Device off
 - Beware of signal feedthrough due to parasitic capacitors

- Increase gate overdrive voltage as much as possible + keep V_{GS} constant
 - Switch overdrive voltage independent of signal level
 - Error due to finite R_{ON} linear (to 1st order)
 - Lower R_{on} → lower time constant

Constant V_{GS} Sampling

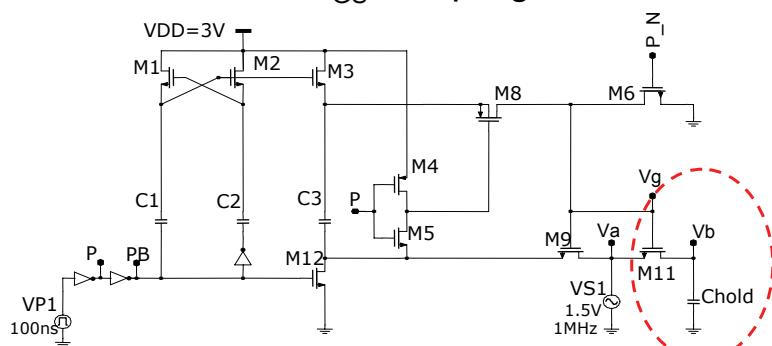


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Constant V_{GS} Sampling Circuit



This Example: All device sizes: $W/L = 10\mu/0.35\mu$

All capacitor size: 1pF (except for Chold)

Note: Each critical switch requires a separate clock booster

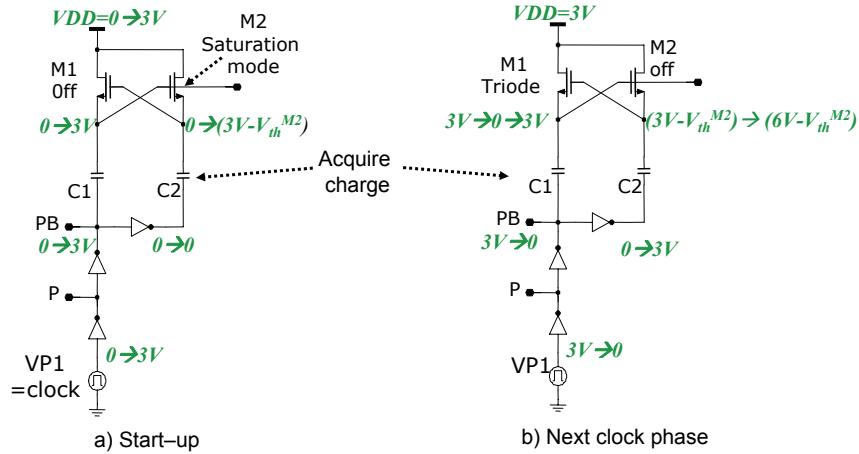
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Clock Voltage Doubler

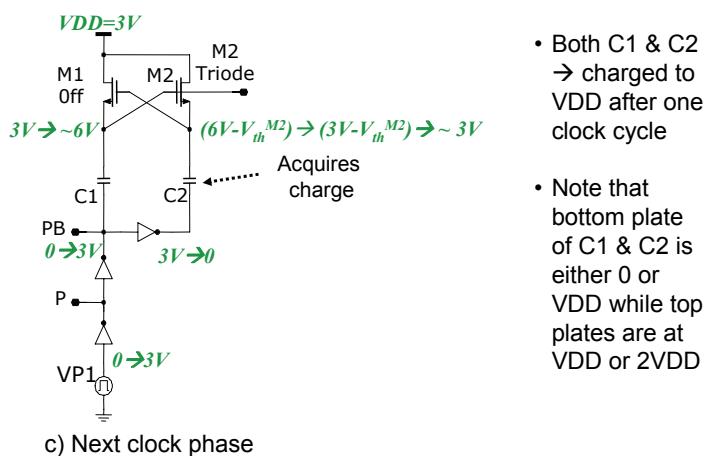


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Clock Voltage Doubler

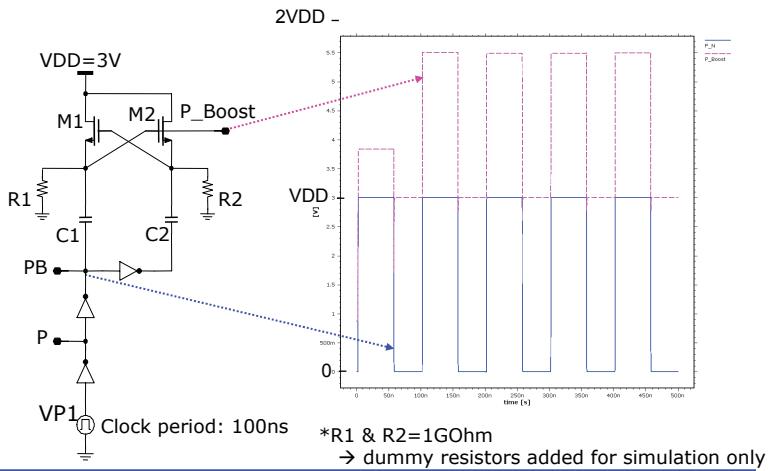


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Clock Voltage Doubler

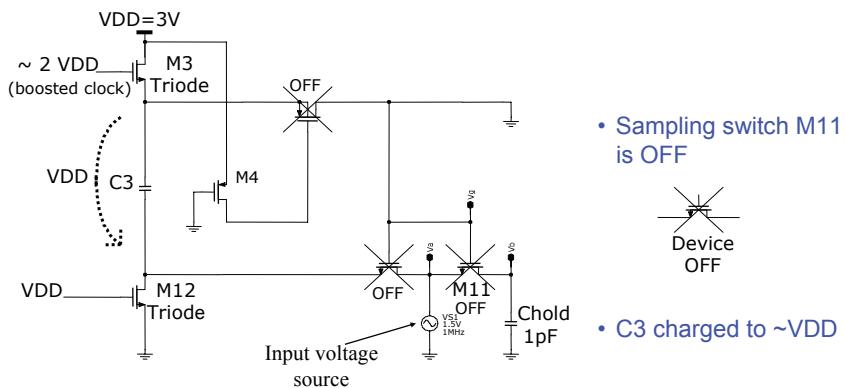


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Constant V_{GS} Sampler: Φ Low

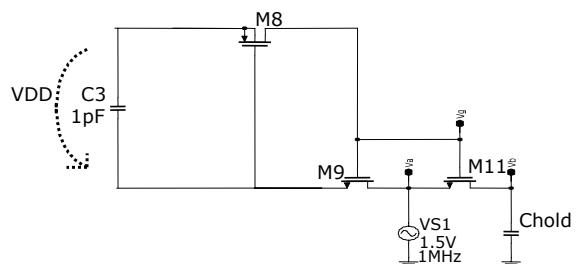


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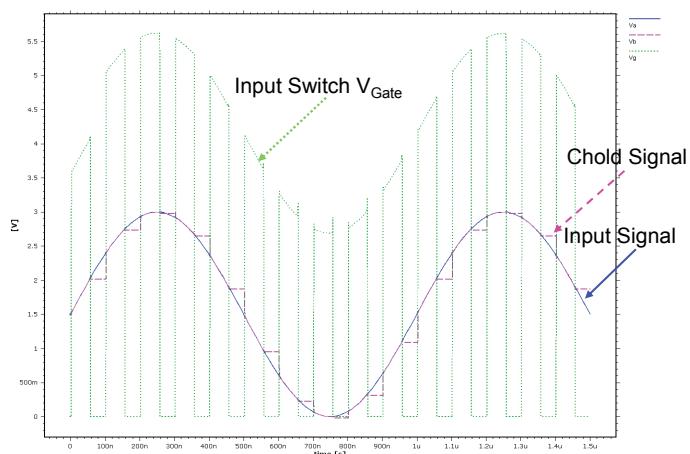
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Constant V_{GS} Sampler: Φ High

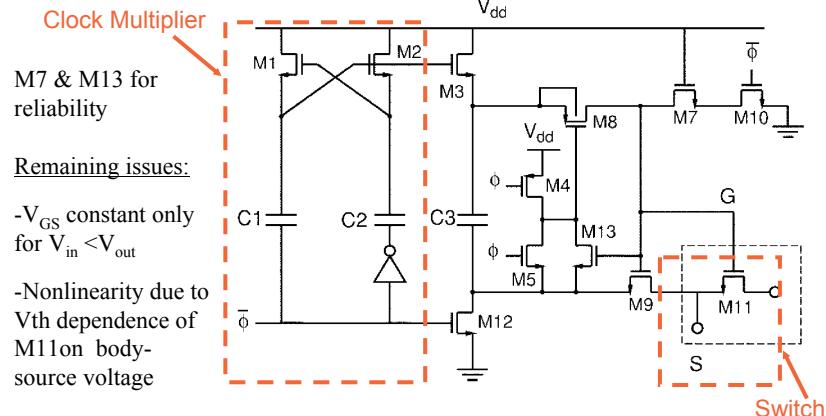


- C_3 previously charged to V_{DD}
- M_8 & M_9 are on: C_3 across G-S of M_{11}
- M_{11} on with constant $V_{GS} = V_{DD}$

Constant V_{GS} Sampling



Boosted Clock Sampling Complete Circuit

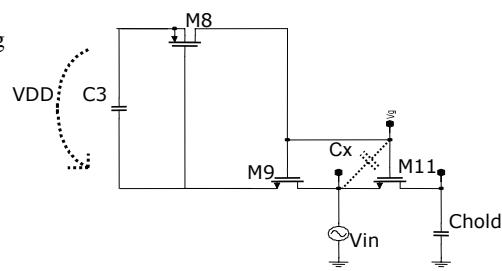


Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

Boosted Clock Sampling Design Consideration

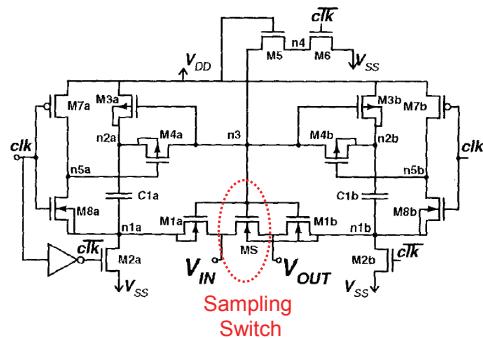
Choice of value for C_3 :

- C_3 too large \rightarrow large charging current \rightarrow large dynamic power dissipation
- C_3 too small \rightarrow $V_{gate-V_s} = \frac{V_{DD} \cdot C_3}{(C_3 + C_x)}$ \rightarrow Loss of V_{GS} due to low ratio of C_x/C_3
 C_x includes M11 CGS and all other parasitics caps....



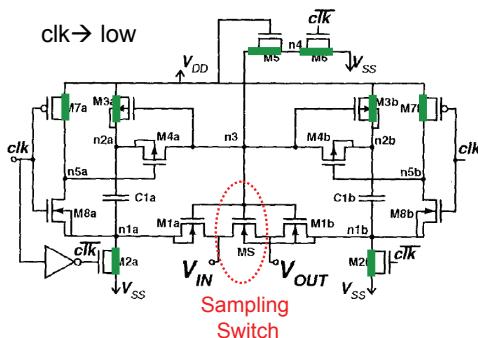
Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

Advanced Clock Boosting Technique



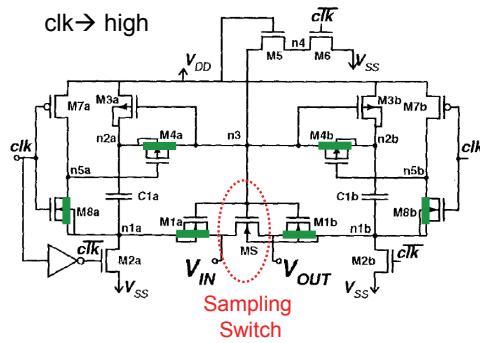
Ref: M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Tech. Papers, pp. 314

Advanced Clock Boosting Technique



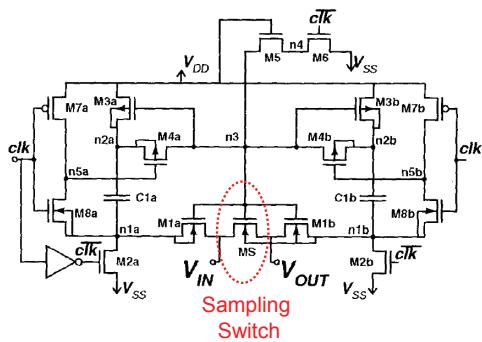
- **clk → low**
 - Capacitors C1a & C1b → charged to VDD
 - MS → off
 - Hold mode

Advanced Clock Boosting Technique



- clk → high
 - Top plate of C1a & C1b connected to gate of sampling switch
 - Bottom plate of C1a connected to V_{IN}
 - Bottom plate of C1b connected to V_{OUT}
 - VGS & VGD of MS both @ VDD & ac signal on G of MS → average of V_{IN} & V_{OUT}

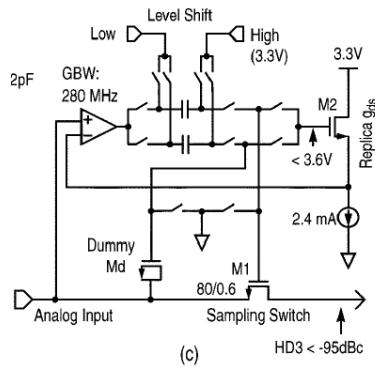
Advanced Clock Boosting Technique



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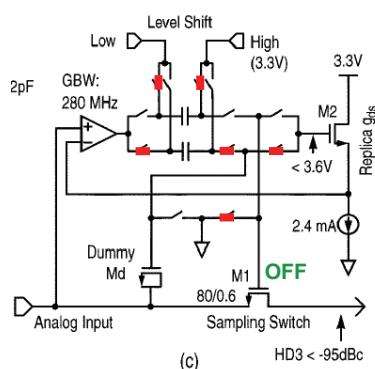
- Gate tracks average of input and output, reduces effect of I-R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to S)
- Reported measured SFDR = 76.5dB at $f_{in}=200MHz$

Constant Conductance Switch



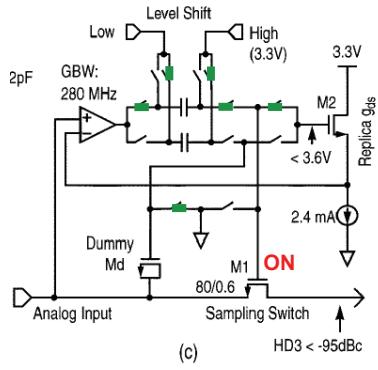
Ref: H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6μm CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, pp. 1769-1780, Dec. 2000

Constant Conductance Switch



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Constant Conductance Switch



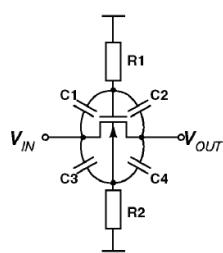
$M_2 \rightarrow$ Constant current
 \rightarrow constant g_{ds}

$M_1 \rightarrow$ replica of M_2
& same VGS
as M_2
 $\rightarrow M_1$ also
constant g_{ds}

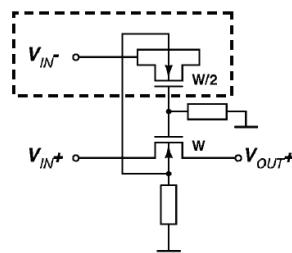
- Note: Authors report requirement of 280MHz GBW for the opamp for 12bit 50Ms/s ADC
- Also, opamp common-mode compliance for full input range required

Ref: H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6μm CMOS with over 80-dB SFDR," IEEE J. Solid-State Circuits, pp. 1769-1780, Dec. 2000

Switch Off-Mode Feedthrough Cancellation



High-pass feedthrough
paths past an open
switch



Feedthrough
cancellation with a
dummy switch

Ref: M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Techn. Papers, pp. 314