EE247
Lecture 15

• D/A converters
  – Practical aspects of current-switched DACs (continued)
  – Segmented current-switched DACs
  – DAC dynamic non-idealities
  – DAC design considerations
  – Self calibration techniques
    • Current copiers
    • Dynamic element matching
  – DAC reconstruction filter
• A/D converter introduction

Summary Last Lecture

D/A converter architectures:
  – Resistor string DAC
  – Serial charge redistribution DAC
  – Parallel charge scaling DAC
  – Combination of resistor string (MSB) & binary weighted charge scaling (LSB)
  – Current source DAC
    • Unit element
    • Binary weighted
• Static performance
  – Component matching-systematic & random errors
    • Component random variations → Gaussian pdf
    • INL for both unit-element & binary weight DAC: \( \sigma_{INL} = \sigma_e 2^{B/2-1} \)
    • DNL for unit-element: \( \sigma_{DNL} = \sigma_e \)
    • DNL for binary-weighted \( \sigma_{DNL} = \sigma_e 2^{B/2} \)
INL & DNL for Binary Weighted DAC

- INL same as for unit element DAC
- DNL depends on transition
  - Example:
    0 to 1 → $\sigma_{DNL}^2 = \sigma_{(dI/dV)}^2$
    1 to 2 → $\sigma_{DNL}^2 = 3\sigma_{(dI/dV)}^2$

- Consider MSB transition:
  0111 → 1000 ...

DAC DNL
Example: 4bit DAC

- DNL depends on transition
  - Example:
    0 to 1 → $\sigma_{DNL}^2 = \sigma_{(dI_{ref}/dV_{ref})}^2$
    1 to 2 → $\sigma_{DNL}^2 = 3\sigma_{(dI_{ref}/dV_{ref})}^2$
### Binary Weighted DAC DNL

- Worst-case transition occurs at mid-scale:
  \[
  \sigma_{DNL} = \frac{2^{B-1} - 1}{2} \sigma_\varepsilon + \frac{2^{B-1}}{2} \sigma_\varepsilon^2 \\
  \approx 2^B \sigma_\varepsilon^2 \\
  \sigma_{DNL_{max}} = 2^{B/2} \sigma_\varepsilon \\
  \sigma_{INL_{max}} \approx \frac{1}{2} \left( \sigma_\varepsilon^2 - 1 \right) \sigma_\varepsilon \approx \frac{1}{2} \sigma_{DNL_{max}}
  \]

- Example:
  \( B = 12, \ \sigma_\varepsilon = 1\% \)  
  \( \sigma_{DNL} = 0.64 \text{ LSB} \)  
  \( \sigma_{INL} = 0.32 \text{ LSB} \)

### Unit Element versus Binary Weighted DAC

**Example: B=10**

**Unit Element DAC**

- \( \sigma_{DNL} = \sigma_\varepsilon \)
- \( \sigma_{INL} \approx 2^{B/2-1} \sigma_\varepsilon = 16 \sigma_\varepsilon \)

**Binary Weighted DAC**

- \( \sigma_{DNL} \approx 2^{B/2} \sigma_\varepsilon = 32 \sigma_\varepsilon \)
- \( \sigma_{INL} \approx 2^{B/2-1} \sigma_\varepsilon = 16 \sigma_\varepsilon \)

Number of switched elements:

- Unit Element: \( S = 2^B = 1024 \)
- Binary Weighted: \( S = B = 10 \)

**Requires B to (2^B-1) decoder to address switches**  
**B-bit digital input can be used directly**

*Significant difference in performance and complexity!*
"Another" Random Run …

Now (by chance) worst DNL is mid-scale.

Close to statistical result!

$\sigma_e = 1\%$

$B = 12$

Random # generator used in MatLab

Computed INL:

$\sigma_{INL}^{\text{max}} = 0.32 \text{ LSB (midscale)}$

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10Bit DAC DNL/INL Comparison

Plots: 100 Simulation Runs Overlaid


Note: $\sigma_e = 2\%$
10Bit DAC DNL/INL Comparison
Plots: RMS for 100 Simulation Runs


Note: $\sigma = 2\%$

DAC INL/DNL Summary

- DAC choice of architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
- Results assume uncorrelated random element variations
- Systematic errors and correlations are usually also important and may affect final DAC performance

Segmented DAC

Combination of Unit-Element & Binary-Weighted

• **Objective:**
  Compromise between unit-element and binary-weighted DAC

• **Approach:**
  \[ B_1 \text{ MSB bits} \rightarrow \text{unit elements} \]
  \[ B_2 \text{ LSB bits} \rightarrow \text{binary weighted} \]
  \[ B_{\text{Total}} = B_1 + B_2 \]

• **INL:** unaffected same as either architecture
• **DNL:** Worst case occurs when LSB DAC turns off and one more MSB DAC element turns on → Same as binary weighted DAC with \((B_2+1) \text{ # of bits}\)
• **Number of switched elements:** \((2^{B_1}-1) + B_2\)

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**Comparison**

**Example:**

\[ B = 12, \quad B_1 = 5, \quad B_2 = 7 \]
\[ B_1 = 6, \quad B_2 = 6 \]

Assuming: \(\sigma_E = 1\%\)

\[ \sigma_{\text{DNL}} \approx 2^{(B_2+1)/2} \sigma_E = 2 \sigma_{\text{INL}} \]
\[ \sigma_{\text{INL}} \approx 2^{B_2-1} \sigma_E \]

\[ S = 2^{B_1} - 1 + B_2 \]

<table>
<thead>
<tr>
<th>DAC Architecture (B1+B2)</th>
<th>(\sigma_{\text{INL,LSB}})</th>
<th>(\sigma_{\text{DNL,LSB}})</th>
<th># of switched elements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit element (12+0)</td>
<td>0.32</td>
<td>0.01</td>
<td>4095</td>
</tr>
<tr>
<td>Segmented (6+6)</td>
<td>0.32</td>
<td>0.113</td>
<td>63+6=69</td>
</tr>
<tr>
<td>Segmented (5+7)</td>
<td>0.32</td>
<td>0.16</td>
<td>31+7=38</td>
</tr>
<tr>
<td>Binary weighted (0+12)</td>
<td>0.32</td>
<td>0.64</td>
<td>12</td>
</tr>
</tbody>
</table>
Practical Aspects
Current-Switched DACs

- Unit element DACs ensure monotonicity by turning on equal-weighted current sources in succession
- Typically current switching performed by differential pairs
- For each diff pair, only one of the devices are on→ switch device mismatch not an issue
- Issue: While binary weighted DAC can use the incoming binary digital word directly, unit element requires a decoder

<table>
<thead>
<tr>
<th>Binary</th>
<th>Thermometer</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>00000000</td>
</tr>
<tr>
<td>001</td>
<td>00000001</td>
</tr>
<tr>
<td>010</td>
<td>00000011</td>
</tr>
<tr>
<td>011</td>
<td>00001111</td>
</tr>
<tr>
<td>100</td>
<td>00111111</td>
</tr>
<tr>
<td>101</td>
<td>01111111</td>
</tr>
<tr>
<td>110</td>
<td>11111111</td>
</tr>
<tr>
<td>111</td>
<td>11111111</td>
</tr>
</tbody>
</table>

Segmented Current-Switched DAC
Example: 8bit→4MSB+4LSB

- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register
Segmented Current-Switched DAC

Cont’d

• 4-bit MSB Unit
element DAC + 4-bit binary weighted DAC

• Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder

• Digital code for both DACs stored in a register

Segmented Current-Switched DAC

Cont’d

• MSB Decoder
  ➔ Domino logic
  ➔ Example: D4,5,6,7=1 OUT=1

• Register
  ➔ Latched NAND gate:
  ➔ CTRL=1 OUT=INB
Segmented Current-Switched DAC
Reference Current Considerations

• $I_{\text{ref}}$ is referenced to $V_{\text{DD}}$

→ Problem: Reference current varies with supply voltage

$$I_{\text{ref}} = \frac{(V_{\text{DD}} - V_{\text{ref}})}{R}$$

Segmented Current-Switched DAC
Reference Current Considerations

• $I_{\text{ref}}$ is referenced to $V_{\text{ss}} \to \text{GND}$

$$I_{\text{ref}} = \frac{(V_{\text{ref}} - V_{\text{ss}})}{R}$$
Segmented Current-Switched DAC Considerations

- Example:
  - 2-bit MSB Unit element DAC & 3-bit binary weighted DAC

- To ensure monotonicity at the MSB→LSB transition: First OFF MSB current source is routed to LSB current generator

DAC Dynamic Non-Idealities

- Finite settling time
  - Linear settling issues: (e.g. RC time constants)
  - Slew limited settling

- Spurious signal coupling
  - Coupling of clock/control signals to the output via switches & switch charge injection

- Timing error related glitches
  - Control signal timing skew
Dynamic DAC Error: Timing Glitch

- Consider binary weighted DAC transition 011 $\rightarrow$ 100
- DAC output depends on timing
- Plot shows situation where the control signals for LSB & MSB
  - LSB/MSBs on time
  - LSB early, MSB late
  - LSB late, MSB early

Glitch Energy

- Glitch energy (worst case) proportional to: $dt \times 2^{B-1}$
- $dt \rightarrow$ error in timing & $2^{B-1}$ associated with half of the switches changing state
- LSB energy proportional to: $T = \frac{1}{f_s}$
- Need $dt \times 2^{B-1} \ll T$ or $dt \ll 2^{B-1} T$

Examples:

<table>
<thead>
<tr>
<th>$f_s$ [MHz]</th>
<th>B</th>
<th>$dt$ [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12</td>
<td>$&lt;&lt; 488$</td>
</tr>
<tr>
<td>20</td>
<td>16</td>
<td>$&lt;&lt; 1.5$</td>
</tr>
<tr>
<td>1000</td>
<td>12</td>
<td>$&lt;&lt; 0.5$</td>
</tr>
</tbody>
</table>

$\rightarrow$ Timing accuracy for logic circuitry associated with data converters much more critical compared to digital circuitry e.g. DSP
DAC Dynamic Errors

- To suppress effect of non-idealities:
  - Retiming of current source control signals
    - Each current source has its own clocked latch incorporated in the current cell
    - Minimization of latch clock skew by careful layout ensuring simultaneous change of bits
  - To minimize control and clock feed through to the output via G-D & G-S of the switches
    - Use of low-swing digital circuitry

DAC Implementation Examples

- Untrimmed segmented

- Current copiers:

- Dynamic element matching:
An 80-MHz 8-bit CMOS D/A Converter

TAKAHIRO MIKI, YASUYUKI NAKAMURA, MASAKI NAKAYA, SOTOJU ASAHI,
YOICHI AKASAKA, AND YASUTAKA HIRIBA

Two sources of systematic error:
- Finite current source output resistance
- Voltage drop due to finite ground bus resistance

Fig. 1. Basic architecture of the DAC.

Fig. 2. Two-step decoding.

Fig. 9. Symmetrical switching.
Current-Switched DACs in CMOS

Assumptions:
- $R_x$ small compared to transistor gate-overdrive
- To simplify analysis: Initially, all device currents assumed to be equal to $I$

$$V_{GS_{M2}} = V_{GS_{M1}} - 4RI$$
$$V_{GS_{M3}} = V_{GS_{M1}} - 7RI$$
$$V_{GS_{M4}} = V_{GS_{M1}} - 9RI$$
$$V_{GS_{M5}} = V_{GS_{M1}} - 10RI$$

$$I_2 = k(V_{GS_{M2}} - V_{th})^2$$

$$I_2 = I_1 \left(1 - \frac{4RI}{V_{GS_{M1}} - V_{th}}\right)^2$$

Example: 5 unit element current sources

Desirable to have $g_m$ small
Two sources of systematic error:
- Finite current source output resistance
- Voltage drop due to finite ground bus resistance

Current-Switched DACs in CMOS

Example: INL of 3-Bit unit element DAC

Example: 7 unit element current source DAC- assume $g_{m}R = 1/100$
- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  $\rightarrow \text{INL} = +0.15\text{LSB}$
- If switching of current sources symmetrical (4-3-5-2-6-1-7)
  $\rightarrow \text{INL} = +0.09\text{, }-0.058\text{LSB} \rightarrow \text{INL reduced by a factor of 2.6}$

This technique is also effective in compensating for systematic errors associated with process gradients.
Current-Switched DACs in CMOS

Example: DNL of 7 unit element DAC

<table>
<thead>
<tr>
<th>Input</th>
<th>DNL [LSB]</th>
</tr>
</thead>
</table>

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  \[ \text{DNL}_{\text{max}} = +0.15\text{LSB} \]
- If switching of current sources symmetrical (4-3-5-2-6-1-7)
  \[ \text{DNL}_{\text{max}} = +0.15\text{LSB} \]

More recent published DAC using symmetrical switching built in 0.35\(\mu\)3V analog/1.9V digital, area x10 smaller compared to previous example
• Layout of Current sources - each current source made of 4 devices in parallel each located in one of the 4 quadrants
• Thermometer decoder used to convert incoming binary digital control for the 5 MSB bits
• Dummy decoder used on the LSB side to match the latency due to the MSB decoder

• Current source layout
  – MSB current sources layout in the mid sections of the four quad
  – LSB current sources mostly in the periphery
  – Two rows of dummy current sources added @ the periphery to create identical environment for devices in the center versus the ones on the outer sections
• Note that each current cell has its clocked latch and clock signal laid out to be close to its switch to ensure simultaneous switching of current sources
• Special attention paid to the final latch to have the cross point of the complementary switch control signal such that the two switches are not both turned off during transition

• Measured DNL/INL with current associated with the current cells as variable
A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

Called:
Current Copier

Fig. 2. Calibration principle. (a) Calibration. (b) Operation.
Current Divider Inaccuracy due to Device Mismatch

M1 & M2 mismatch results in the two output currents not being exactly equal:

\[
I_d = \frac{I_{d1} + I_{d2}}{2}
\]

\[
\frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d}
\]

\[
\frac{dI_d}{I_d} = \frac{2}{V_{GS} - V_{th}} \left( \frac{dW_{L}}{W_L} + dV_{th} \right)
\]

Problem: Device mismatch could severely limit DAC accuracy
Use of dynamic element matching (next few pages)
Dynamic Element Matching

During $\Phi_1$
\[ I_1^{(1)} = \frac{1}{4} I_o (1 + \Delta I) \]
\[ I_2^{(1)} = \frac{1}{4} I_o (1 - \Delta I) \]

Average of $I_2$:
\[ \langle I_2 \rangle = \frac{I_2^{(1)} + I_2^{(2)}}{2} \]
\[ = \frac{I_o (1 - \Delta I) + (1 + \Delta I)}{2} \]
\[ = \frac{I_o}{2} \]

Note: DAC frequency of operation $< f_{clk}$

Note:
For optimum current division accuracy $\rightarrow$ clock frequency is divided by two for each finer division
Problem: DAC frequency of operation drastically reduced

Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Time dependence of currents flowing in the first and second divider stage.

Note: What if the same clock frequency is used?
Dynamic Element Matching

\[
\begin{align*}
\text{During } \Phi_1: & \\
I_1^{(1)} &= \frac{1}{2} I_1 (1 + \Delta_1) \\
I_1^{(2)} &= \frac{1}{2} I_1 (1 - \Delta_1) \\
I_1^{(1)} &= \frac{1}{2} I_0 (1 + \Delta_1) \\
I_1^{(2)} &= \frac{1}{2} I_0 (1 - \Delta_1)
\end{align*}
\]

\[
\begin{align*}
\langle I_1 \rangle &= \frac{I_1^{(1)} + I_1^{(2)}}{2} \\
&= \frac{I_1 (1 + \Delta_1) (1 + \Delta_1) + (1 - \Delta_1) (1 - \Delta_1)}{4} \\
&= \frac{I_1 (1 + \Delta_1, \Delta_1)}{4}
\end{align*}
\]

E.g. \( \Delta_1 = \Delta_2 = 1\% \rightarrow \) matching error is \((1\%)^2 = 0.01\%

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Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASCHTE

- Bipolar 12-bit DAC using dynamic element matching built in 1976
- Element matching clock frequency 100kHz
- INL <0.25LSB!
Example: State-of-the-Art current steering DAC

- **Segmented:**
  - 6bit unit-element
  - 8bit binary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max Sample Frequency</th>
<th>GSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>14</td>
<td>Bit</td>
</tr>
<tr>
<td>DNL</td>
<td>+/- 0.8</td>
<td>LSB</td>
</tr>
<tr>
<td>INL</td>
<td>+/- 2.1</td>
<td>LSB</td>
</tr>
<tr>
<td>SFDR @ 1.0 GSPS</td>
<td>&gt; 60</td>
<td>dB</td>
</tr>
<tr>
<td>IMD @ 1.0 GSPS</td>
<td>&gt; 64</td>
<td>dBC</td>
</tr>
<tr>
<td>NSD @ f_{out} = 400MHz</td>
<td>-155</td>
<td>dBm/Hz</td>
</tr>
<tr>
<td>Power (Core) @ 1.4GSPS</td>
<td>200</td>
<td>mW</td>
</tr>
<tr>
<td>Power (Total) @ 1.4GSPS</td>
<td>400</td>
<td>mW</td>
</tr>
<tr>
<td>Area (Core)</td>
<td>0.8</td>
<td>mm^2</td>
</tr>
<tr>
<td>Area (Chip)</td>
<td>6.25</td>
<td>mm^2</td>
</tr>
</tbody>
</table>

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**Layout Tree Structures**

- **CLK**
- **DATA**
- **OUTPUT CURRENTS**
- **VCAS**
- **DECODER**
- **SWITCHES**
- **CASCODES**
- **SEGMENT CURRENT**
DAC In the Big Picture

- Learned to build DACs
  - Convert the incoming digital signal to analog
- DAC output → staircase form
- Some applications require filtering (smoothing) of DAC output
  → reconstruction filter

DAC Reconstruction Filter

- Need for and requirements depend on application
- Tasks:
  - Correct for sinc droop
  - Remove “aliases” (stair-case approximation)
Reconstruction Filter Options

- Reconstruction filter options:
  - Continuous-time filter only
  - CT + SC filter
- SC filter possible only in combination with oversampling (signal bandwidth \( B \ll f_s/2 \))
- Digital filter
  - Band limits the input signal \( \rightarrow \) prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band \( \sin(x)/x \) amplitude droop associated with the inherent DAC S/H function

---

 DAC Reconstruction Filter Example: Voice-Band CODEC Receive Path

\[
\text{Note: } f_{\text{DAC}} = 8\text{kHz} \quad f_{\text{max}} = 3.4\text{kHz} \\
\Rightarrow \sin(\pi f_{\text{max}} x T_s)/(\pi f_{\text{max}} x T_s) = -2.75 \text{ dB droop due to DAC } \sin(x)/x \text{ shape}
\]

Summary

D/A Converter

• D/A architecture
  – Unit element – complexity proportional to $2^B$, excellent DNL
  – Binary weighted - complexity proportional to $B$; poor DNL
  – Segmented- unit element $MSB(B_1)+$ binary weighted $LSB(B_2)$
  $\rightarrow$ Complexity proportional $(2^{B_1}-1) + B_2$; DNL compromise between the two

• Static performance
  – Component matching

• Dynamic performance
  – Time constants, Glitches

• DAC improvement techniques
  – Symmetrical switching rather than sequential switching
  – Current source self calibration
  – Dynamic element matching

• Depending on the application, reconstruction filter may be needed

What Next?

• ADC Converters:
  – Need to build circuits that "sample"
  – Need to build circuits for amplitude quantization
Analog-to-Digital Converters

• Two categories:
  – Nyquist rate ADCs $\rightarrow f_{\text{sig max}} \sim 0.5 f_{\text{sampling}}$
    • Maximum achievable signal bandwidth higher compared to oversampled type
    • Resolution limited to max. 12-14 bits
  – Oversampled ADCs $\rightarrow f_{\text{sig max}} \ll 0.5 f_{\text{sampling}}$
    • Maximum achievable signal bandwidth significantly lower compared to nyquist
    • Maximum achievable resolution high (18 to 20 bits!)

MOS Sampling Circuits
Ideal Sampling

- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage $v_{IN}$ onto the capacitor $C$.

  → Output Dirac-like pulses with amplitude equal to $V_{IN}$ at the time of sampling.

- In practice not realizable!

$$v_{IN} \rightarrow v_{OUT}$$

$$C$$

$$S_1$$

$\phi_1$

$T = \frac{1}{f_S}$

Ideal Track & Hold Sampling

- $V_{out}$ tracks input for $\frac{1}{2}$ clock cycle when switch is closed.
- Ideally acquires *exact* value of $V_{in}$ at the instant the switch opens.
- "Track and Hold" (T/H) (often called Sample & Hold!)

$$v_{IN} \rightarrow v_{OUT}$$

$$C$$

$$S_1$$

$\phi_1$

$T = \frac{1}{f_S}$
Ideal T/H Sampling

Continuous Time

T/H signal (Sampled-Data Signal)

Clock

Discrete-Time Signal

Practical Sampling Issues

- Switch induced noise due to M1 finite channel resistance
- Clock jitter
- Finite $R_{SW} \rightarrow$ limited bandwidth $\rightarrow$ finite acquisition time
- $R_{SW} = f(V_{IN}) \rightarrow$ distortion
- Switch charge injection & clock feedthrough
Sampling Circuit kT/C Noise

- Switch resistance & sampling capacitor form a low-pass filter
- Noise associated with the switch resistance results in Total noise variance = kT/C @ the output (see noise analysis in Lecture 1)
- In high resolution ADCs kT/C noise at times dominates overall minimum signal handling capability (power dissipation considerations).

Sampling Network kT/C Noise

For ADCs sampling capacitor size is usually chosen based on having thermal noise smaller or equal or at times larger compared to quantization noise:
Assumption: Nyquist rate ADC

For a Nyquist rate ADC: Total quantization noise power = \( \Delta^2 \)

Choose C such that thermal noise level is less (or equal) than Q noise

\[
\frac{k_B T}{C} \leq \frac{\Delta^2}{12}
\]

\[\Rightarrow C \geq 12k_B T \left( \frac{2^B - 1}{V_{FS}} \right)^2\]

\[\Rightarrow C \geq 12k_B T \times \frac{2^{2B}}{V_{FS}^2}\]
Sampling Network $kT/C$ Noise

\[ C \geq 12k_BT \frac{2^B}{V_{FS}^2} \]

<table>
<thead>
<tr>
<th>B</th>
<th>$C_{\text{min}}$ ($V_{FS} = 1V$)</th>
<th>$C_{\text{min}}$ ($V_{FS} = 0.5V$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>0.003 pF</td>
<td>0.012 pF</td>
</tr>
<tr>
<td>12</td>
<td>0.8 pF</td>
<td>2.4 pF</td>
</tr>
<tr>
<td>14</td>
<td>13 pF</td>
<td>52 pF</td>
</tr>
<tr>
<td>16</td>
<td>206 pF</td>
<td>824 pF</td>
</tr>
<tr>
<td>20</td>
<td>52,800 pF</td>
<td>211,200 pF</td>
</tr>
</tbody>
</table>

The large area required for $C \rightarrow$ limit highest achievable resolution for Nyquist rate ADCs

Oversampling results in reduction of required value for $C$ (will be covered in oversampled converter lectures)

Clock Jitter

- So far: clock signal controls sampling instants – which we assumed to be precisely equi-distant in time (period $T$)

- Real clock generator $\rightarrow$ some level of variability

- Variability in $T$ causes errors
  - "Aperture Uncertainty" or "Aperture Jitter"

- What is the effect of clock jitter on ADC performance?
Clock Jitter

• Sampling jitter adds an error voltage proportional to the product of \((t_J - t_0)\) and the derivative of the input signal at the sampling instant.

\[
e = x'(t_0)(t_J - t_0)
\]

• Does jitter matter when sampling dc signals \((x'(t_0) = 0)\)?
Effect of Clock Jitter on Sampling of a Sinusoidal Signal

Sinusoidal input

- **Amplitude:** $A$
- **Frequency:** $f_s$
- **Jitter:** $\frac{d}{t}$

$$x(t) = A \sin(2\pi f_s t)$$

$$x'(t) = 2\pi f_s A \cos(2\pi f_s t)$$

$$\left| x'(t) \right|_{\text{max}} \leq 2\pi f_s A$$

**Worst case**

- $A = \frac{A_{FS}}{2}$
- $f_s = \frac{f_s}{2}$

$$|e(t)| << \frac{A}{2} \approx \frac{A_{FS}}{2^{B+1}}$$

$$dt << \frac{1}{2^B \pi f_s}$$

<table>
<thead>
<tr>
<th># of Bits</th>
<th>$f_s$</th>
<th>$dt &lt;&lt;$</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>1 MHz</td>
<td>78 ps</td>
</tr>
<tr>
<td>16</td>
<td>20 MHz</td>
<td>0.24 ps</td>
</tr>
<tr>
<td>12</td>
<td>1000 MHz</td>
<td>0.07 ps</td>
</tr>
</tbody>
</table>

Statistical Jitter Analysis

- The worst case looks pretty stringent … what about the “average”?
- Let’s calculate the mean squared jitter error (variance)
- If we’re sampling a sinusoidal signal
  $$x(t) = A \sin(2\pi f_s t),$$
  then
  - $x'(t) = 2\pi f_s A \cos(2\pi f_s t)$
  - $E\{[x'(t)]^2\} = 2\pi^2 f_s^2 A^2$

- Assume the jitter has variance $E\{(t_j-t_0)^2\} = \tau^2$
Statistical Jitter Analysis

- If $x'(t)$ and the jitter are independent
  - $E\{[x'(t)(t_J-t_0)]^2\} = E\{[x'(t)]^2\} E\{(t_J-t_0)^2\}$

- Hence, the jitter error power is
  - $E\{e^2\} = 2\pi^2 f_x^2 A^2 \tau^2$

- If the jitter is uncorrelated from sample to sample, this “jitter noise” is white
Example: ADC Spectral Tests


More on Jitter

- In cases where clock signal is provided from off-chip → have to choose a source with low enough jitter
- On-chip precautions to keep the clock jitter less than single-digit pico-second:
  - Separate supplies as much as possible
  - Separate analog and digital clocks
  - Short inverter chains between clock source and destination
- Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
  - RMS noise proportional to input signal frequency
  - RMS noise proportional to input signal amplitude
- In cases where clock jitter limits the dynamic range, it’s easy to tell, but may be difficult to fix...