EE247
Lecture 10

- Switched-capacitor filters
  - Effect of non-idealities (continued)
  - Switched-capacitor filters utilizing double sampling technique
- Data converters
  - Areas of application
  - Data converter transfer characteristics
  - Sampling, aliasing, reconstruction
  - Amplitude quantization

Effect of Opamp Nonidealities on Switched Capacitor Filter Behaviour

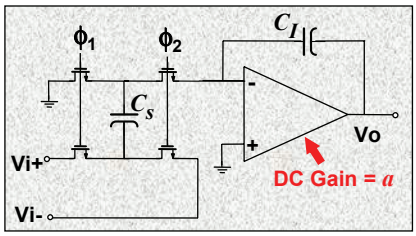
- Opamp finite gain
- Opamp finite bandwidth
- Sources of distortion
  - Finite slew rate of the opamp
  - Non-linearity associated with opamp output/input characteristics
  - Capacitor non-linearity- usually insignificant, similar to cont. time filters
  - Charge injection & clock feedthrough (will be covered in the oversampling data converter section)

Effect of Opamp Non-Idealities
Finite DC Gain

$$H(s) \approx -f_s \frac{C_s}{C_I} \frac{1}{s + f_s \frac{C_s}{C_I} \times \frac{1}{a}}$$

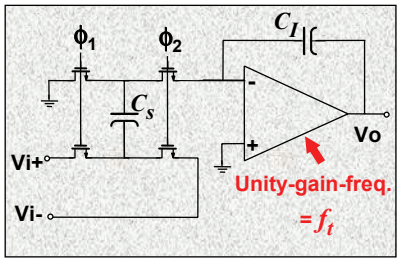
$$H(s) \approx \frac{-\omega_o}{s + \omega_o \times \frac{1}{a}}$$

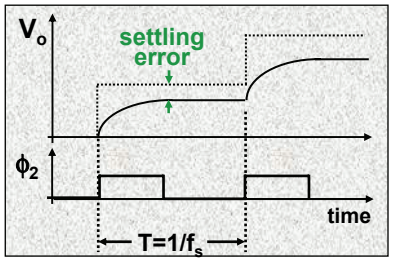
$$\Rightarrow \boxed{Q_{intg} \approx a}$$



- **Finite DC gain same effect in S.C. filters as for C.T. filters**
- **If DC gain not high enough → lowing of overall Q & droop in passband**

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth





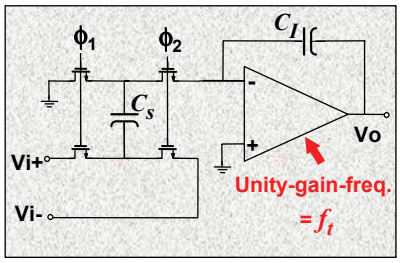
Assumption-

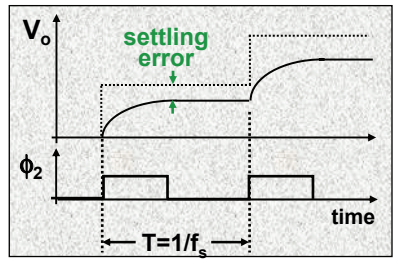
Opamp → does not slew (will be revisited)

Opamp has only one pole only → exponential settling

Ref: K.Martin, A. Sedra, "Effect of the Opamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth





$$H_{actual}(Z) \approx H_{ideal}(Z)\left[1-e^{-k}+e^{-k}\times\frac{C_I}{C_I+C_s}Z^{-1}\right]$$

$$where \quad k=\pi\times\frac{C_I}{C_I+C_s}\times\frac{f_t}{f_s}$$

$$f_t \rightarrow \ Opamp\ unity-gain-frequency \quad , \quad f_s \rightarrow \ Clock\ frequency$$

Ref: K.Martin, A. Sedra, "Effect of the Opamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

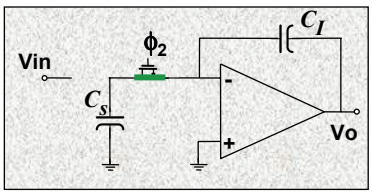
Opamp Bandwidth Requirements for Switched-Capacitor Filters Compared to Continuous-Time Filters

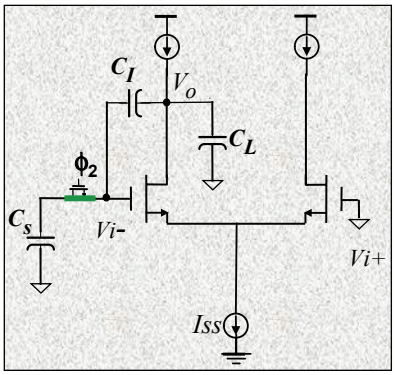
- Finite opamp bandwidth causes phase lag at the unity-gain frequency of the integrator for both type filters
  → Results in negative intg. Q & thus increases overall Q and gain @ results in peaking in the passband of interest
- For given filter requirements, opamp bandwidth requirements much less stringent for S.C. filters compared to cont. time filters
  → Lower power dissipation for S.C. filters (at low freq.s only due to other effects)
- Finite opamp bandwidth causes down shifting of critical frequencies in both type filters
  – Since cont. time filters are usually tuned→ tuning accounts for frequency deviation
  – S.C. filters are untuned and thus frequency shift could cause problems specially for narrow-band filters

Effect of Opamp Nonidealities on Switched Capacitor Filter Behaviour

- Opamp finite gain
- Opamp finite bandwidth
- Sources of distortion
  - Finite slew rate of the opamp
  - Non-linearity associated with opamp output/input characteristics
  - Capacitor non-linearity- usually insignificant, similar to cont. time filters
  - Charge injection & clock feedthrough (will be covered in the oversampling data converter section)

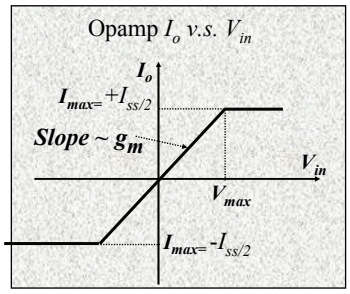
What is Slewing?

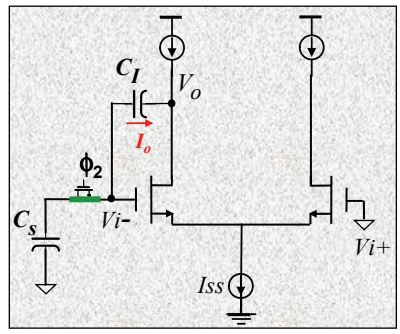




Assumption:
Integrator opamp is a simple class A transconductance type differential pair with fixed tail current, *Iss=const.*

What is Slewing?





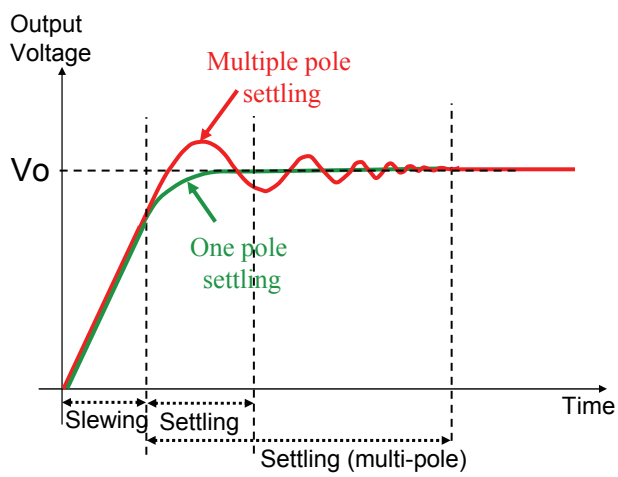
$|V_{Cs}| > V_{max}$ → Output current constant I_o=*Iss/2 or –Iss/2*

→ Constant current charging/discharging C_I: V_o ramps down/up → Slewing

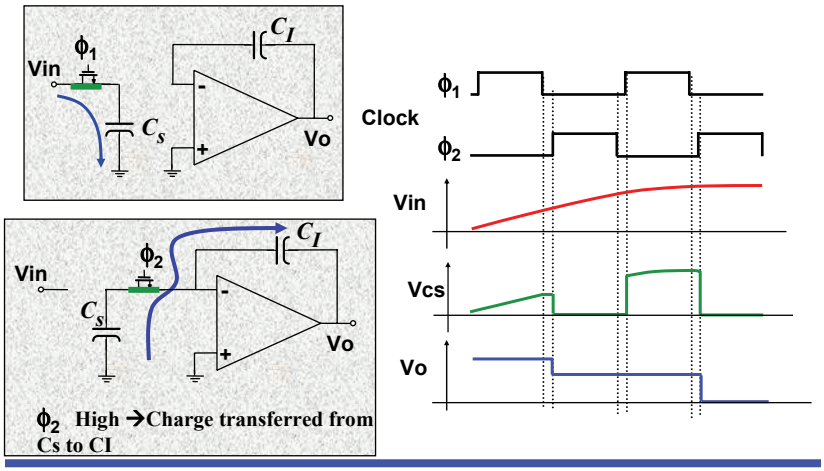
After V_{Cs} is discharged enough to have:

$|V_{Cs}|<V_{max}$ → I_o=*gm* V_{Cs} → Output→ Exponential or over-shoot settling

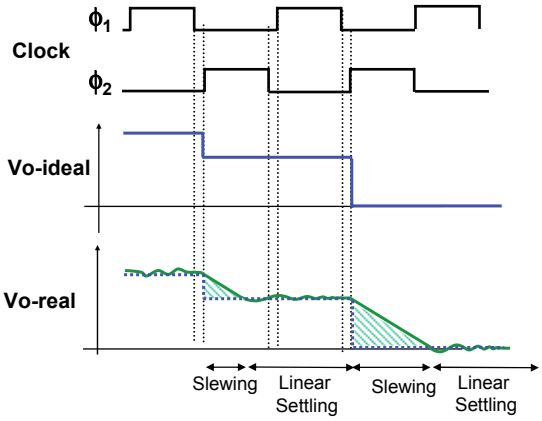
Distortion Induced by Opamp Finite Slew Rate



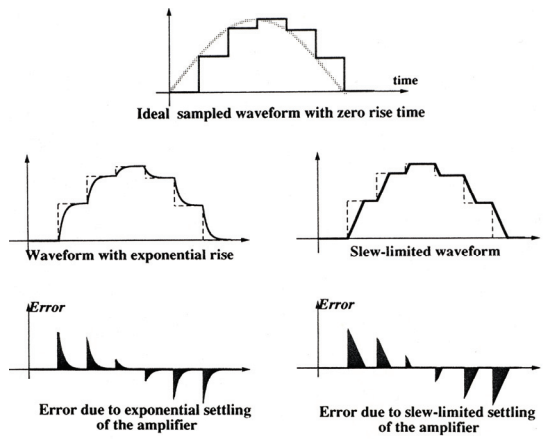
Ideal Switched-Capacitor Output Waveform



Slew Limited Switched-Capacitor Integrator Output Slewing & Settling



Distortion Induced by Finite Slew Rate of the Opamp



Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

Distortion Induced by Opamp Finite Slew Rate

- Error due to exponential settling changes linearly with signal amplitude
- Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error)
  - → For high-linearity need to have either high slew rate or non-slewing opamp

$$HD_k = \frac{V_o}{S_r T_s} \frac{8\left(\sin \omega_o T_s/2\right)^2}{\pi k\left(k^2-4\right)}$$

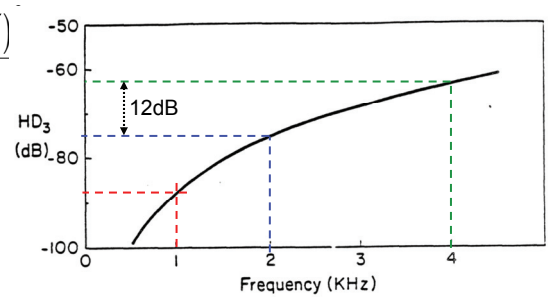
$$\rightarrow HD_3 = \frac{V_o}{S_r T_s} \frac{8\left(\sin \omega_o T_s/2\right)^2}{15\pi} \quad for \quad f_o << f_s \rightarrow \quad HD_3 \approx \frac{8\pi V_o}{15 S_r} \frac{f_o^2}{f_s}$$

Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

Example:
Slew Related Harmonic Distortion

$$HD_3 = \frac{V_o}{S_r T_s} \frac{8\left(\sin \omega_o T_s/2\right)}{15\pi}$$

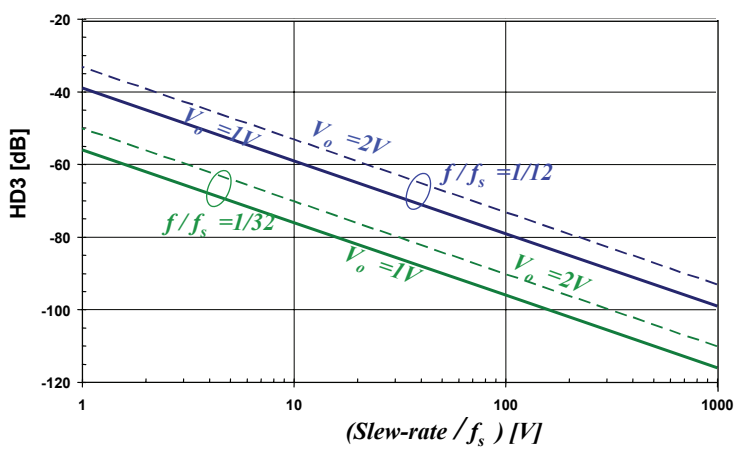
$$HD_3 \approx \frac{8\pi V_o}{15 S_r} \frac{f_o^2}{f_s}$$



Switched-capacitor filter with *4kHz* bandwidth, f_s=*128kHz*, S_r=*1V/μsec*, V_o=*3V*

Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

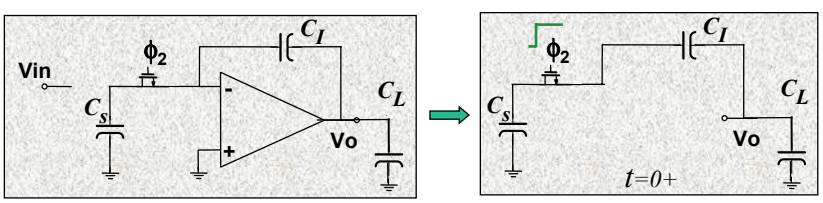
Distortion Induced by Opamp Finite Slew Rate Example



Distortion Induced by Finite Slew Rate of the Opamp

- Note that for a high order switched capacitor filter → only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  - → Can reduce slew limited non-linearities by using an amplifier with a higher slew rate *only* for the last stage
  - → Can reduce slew limited non-linearities by using class A/B amplifiers
    - Even though the output/input characteristics is non-linear as long as the DC open-loop gain is high, the significantly higher slew rate compared to class A amplifiers helps improve slew rate induced distortion in S.C. filters
- In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) → no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time

More Realistic Switched-Capacitor Circuit Slew Scenario



At the instant C_s connects to input of opamp (t=0+)

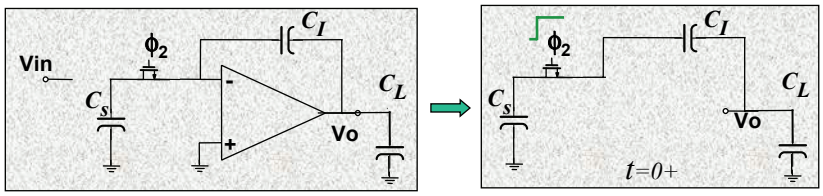
→ Opamp not yet active at t=0+ due to finite opamp bandwidth → delay

→ Feedforward path from input to output generates a voltage spike at the output with polarity opposite to final Vo step- spike magnitude function of C_I, C_L, C_s

→ Spike increases slewing period

→ Eventually, opamp becomes active - starts slewing followed by subsequent settling

Switched-Capacitor Circuit
Opamp not Active @ $t=0+$



$$Charge\ sharing:\ C_s V_{Cs}^{t0-} = V_{Cs}^{t0+}\left(C_s + C_{eq}\right) \quad where\ C_{eq} = \frac{C_I C_L}{C_I + C_L}$$

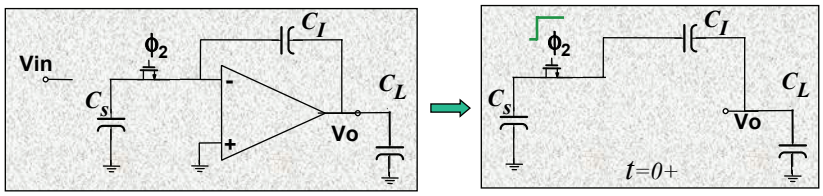
$$\Delta V_{out}^{t0+} = V_{Cs}^{t0+}\frac{C_I}{C_I + C_L} = V_{Cs}^{t0-}\frac{C_s}{C_s + C_{eq}} \times \frac{C_I}{C_I + C_L}$$

$$Assuming\ C_L << C_s << C_I \rightarrow C_{eq} \approx C_L \rightarrow C_s V_{Cs}^{t0-} \approx V_{Cs}^{t0+}\left(C_s + C_L\right) \rightarrow V_{Cs}^{t0-} \approx V_{Cs}^{t0+}$$

$$\rightarrow \Delta V_{out}^{t0+} \approx V_{Cs}^{t0-}\frac{C_s}{C_s + C_L} \times \frac{C_I}{C_I + C_L} \approx V_{Cs}^{t0-}$$

$$Note\ that\ \ \Delta V_{out}^{final} \approx -\frac{C_s}{C_I} V_{Cs}^{t0+} \approx -\frac{C_s}{C_I} V_{Cs}^{t0-}$$

More Realistic Switched-Capacitor Circuit Slew Scenario



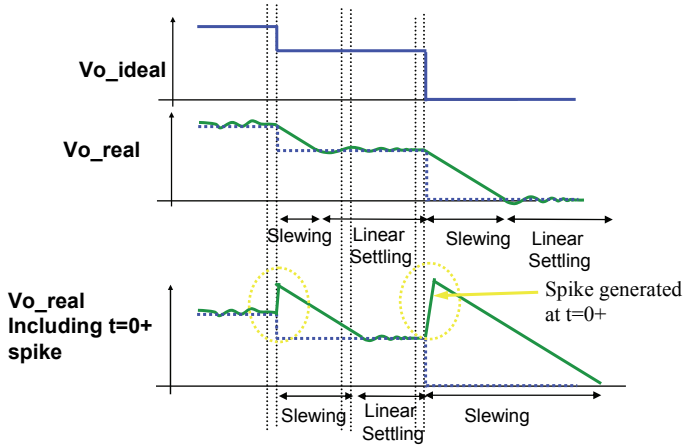
Notice that if C_L is large → some of the charge stored on Cs is lost prior to opamp becoming effective → operation looses accuracy

$$Charge\ sharing:\ C_s V_{Cs}^{t0-} = V_{Cs}^{t0+}\left(C_s + C_{eq}\right) \quad where\ C_{eq} = \frac{C_I C_L}{C_I + C_L}$$

$$V_{Cs}^{t0+} = V_{Cs}^{t0-}\frac{C_s}{C_s + C_{eq}} = V_{Cs}^{t0-}\frac{C_s}{C_s + \frac{C_I C_L}{C_I + C_L}}$$

→ Partly responsible for S.C. filters only good for low-frequency applications

More Realistic S.C. Slew Scenario



Ref: R. Castello, "Low Voltage, Low Power Switched-Capacitor Signal Processing Techniques," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Aug. '84 (ERL Memorandum No. UCB/ERL M84/67).

Sources of Noise in Switched-Capacitor Filters

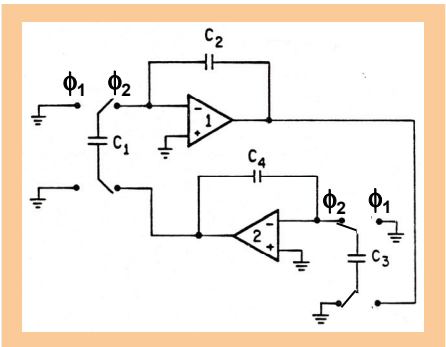
- Opamp Noise
  - Thermal noise
  - 1/f (flicker) noise
- Thermal noise associated with the switching process (kT/C)
  - Same as continuous-time filters
- Precaution regarding aliasing of noise required

Extending the Maximum Achievable Critical Frequency of Switched-Capacitor Filters

Consider a switched-capacitor resonator:

Regular sampling:
Each opamp is busy settling only during one of the two clock phases

→ Idle during the other clock phase

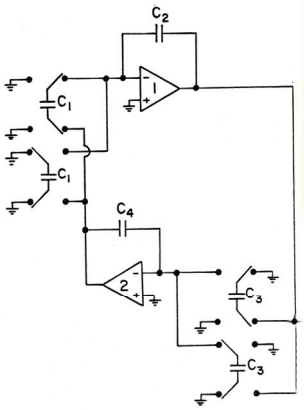


Note: During ϕ_1 both opamps are idle

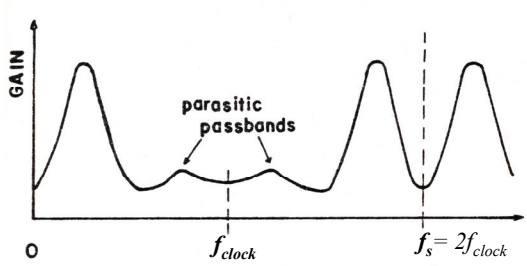
Switched-Capacitor Resonator Using Double-Sampling

Double-sampling:

- 2nd set of switches & sampling caps added to all integrators
- While one set of switches/caps sampling the other set transfers charge into the intg. cap
- Opamps busy during both clock phases
- **Effective sampling freq. twice the clock freq. while opamp bandwidth requirement remains the same**



Double-Sampling Issues

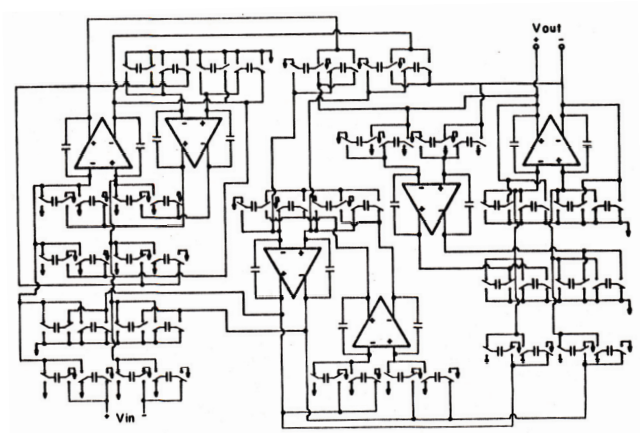


Issues to be aware of:
- Jitter in the clock
- Unequal clock phases
- Mismatch in sampling caps.

→ Results in parasitic passbands

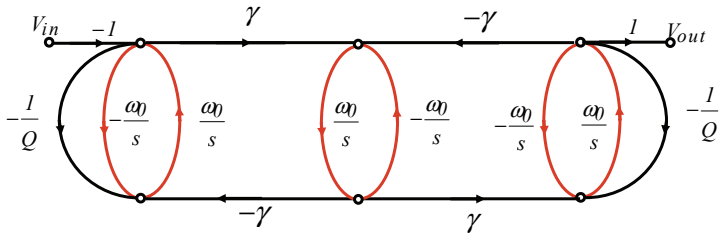
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Double-Sampled Fully Differential S.C. 6th Order All-Pole Bandpass Filter

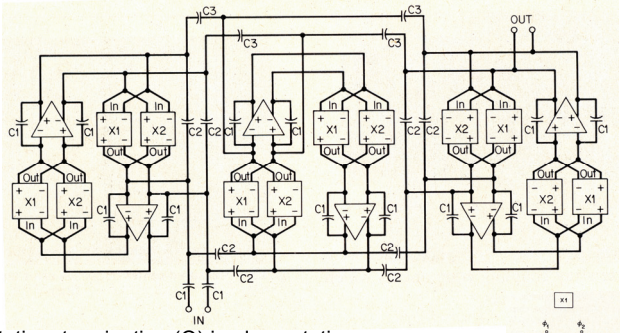


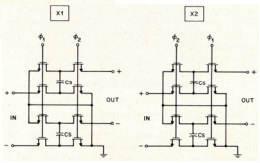
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Sixth Order Bandpass Filter Signal Flowgraph



Double-Sampled Fully Differential 6th Order S.C. All-Pole Bandpass Filter

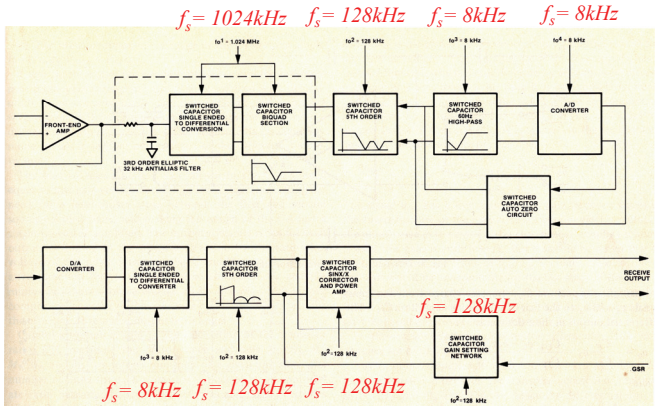




- Cont. time termination (Q) implementation
- Folded-Cascode opamp with $f_u = 100MHz$ used
- Center freq. $3.1MHz$ (Measured error $>1\%$), filter $Q=55$
- Clock freq. $12.83MHz$ → effective oversampling ratio 8.27
- Measured dynamic range $46dB$ ($IM3=1\%$)

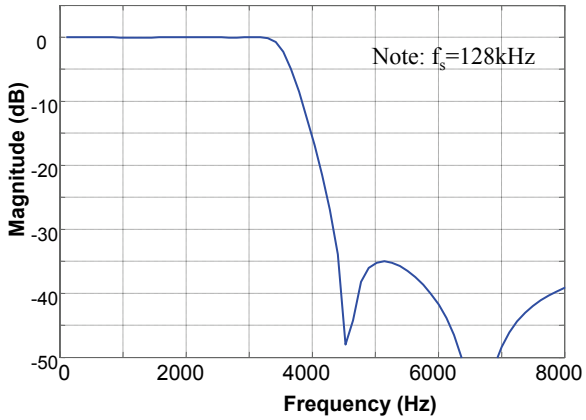
Ref: B.S. Song, P.R. Gray "Switched-Capacitor High-Q Bandpass Filters for IF Applications," *IEEE Journal of Solid State Circuits*, Vol. 21, No. 6, pp. 924-933, Dec. 1986.

Switched-Capacitor Filter Application
Example: Voice-Band CODEC (Coder-Decoder) Chip

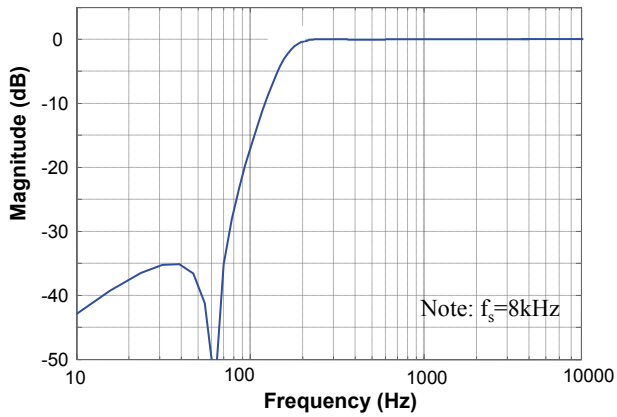


Ref: D. Senderowicz et. al, "A Family of Differential NMOS Analog Circuits for PCM Codec Filter Chip," *IEEE Journal of Solid-State Circuits,* Vol.-SC-17, No. 6, pp.1014-1023, Dec. 1982.

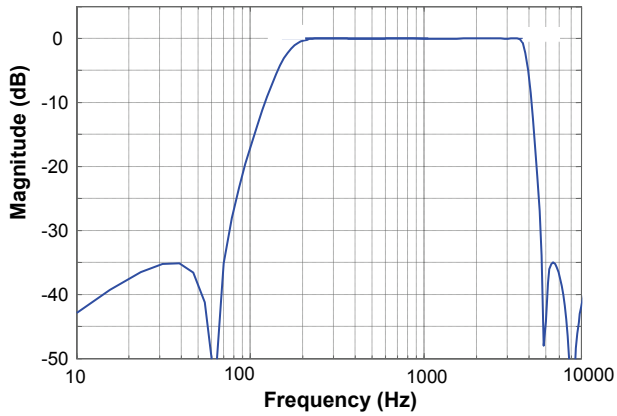
CODEC Transmit Path
Lowpass Filter Frequency Response



CODEC Transmit Path Highpass Filter



CODEC Transmit Path Filter Overall Frequency Response



Low Q bandpass (Q<1) filter shape→ Implemented with lowpass followed by highpass

CODEC Transmit Path Clocking Scheme

First filter (1st order RC type) performs anti-aliasing for the next S.C. biquad

The first 2 stage filters form 3rd order elliptic with corner frequency @ 32kHz → Anti-aliasing for the next S.C. lowpass filter with 3.4kHz corner freq.

The stages prior to the high-pass perform anti-aliasing for high-pass

Notice gradual lowering of clock frequency → Ease of anti-aliasing

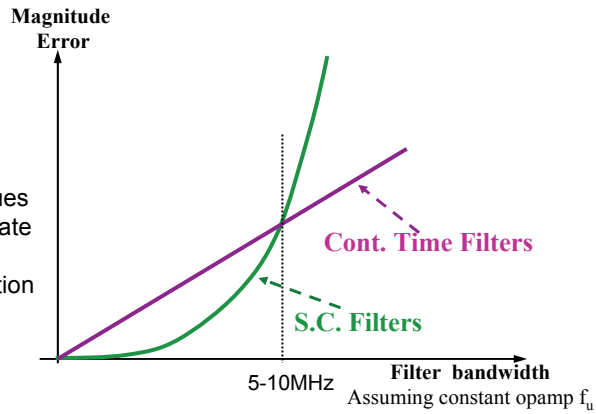
SC Filter Summary

- ✓ Pole and zero frequencies proportional to
  - Sampling frequency f_s
  - Capacitor ratios
  - ➢ High accuracy and stability in response
  - ➢ Long time constants realizable without large R, C
- ✓ Compatible with transconductance amplifiers
  - Reduced circuit complexity, power dissipation
- ✓ Amplifier bandwidth requirements less stringent compared to CT filters (low frequencies only)
- ☹ Issue: Sampled-data filters → require anti-aliasing prefiltering

Switched-Capacitor Filters versus Continuous-Time Filter Limitations

Considering overall effects:

- Opamp finite unity-gain-bandwidth
- Opamp settling issues
- Opamp finite slew rate
- Clock feedthru & switch charge injection
- Switch+ sampling cap. finite time-constant



→ Limited switched-capacitor filter performance frequency range

Summary
Filter Performance versus Filter Topology

	Max. Usable Bandwidth	SNDR	Freq. Tolerance w/o Tuning	Freq. Tolerance + Tuning
Opamp-RC	~10MHz	60-90dB	+-30-50%	1-5%
Opamp-MOSFET-C	~ 5MHz	40-60dB	+-30-50%	1-5%
Opamp-MOSFET-RC	~ 5MHz	50-90dB	+-30-50%	1-5%
Gm-C	~ 100MHz	40-70dB	+-40-60%	1-5%
Switched Capacitor	~ 10MHz	40-90dB	<1%	_

Frequency Warping

- Frequency response
  - Continuous time (s-plane): imaginary axis
  - Sampled time (z-plane): unit circle
- Continuous to sampled time transformation
  - Should map imaginary axis onto unit circle
  - How do S.C. integrators map frequencies?

$$H_{\text{S.C.}}(z) = \frac{C_s}{C_{int}} \frac{z^{-1/2}}{1 - z^{-1}}$$

$$= -\frac{C_s}{C_{int}} \frac{1}{2j \sin \pi f T}$$

CT – SC Integrator Comparison

CT Integrator

$$H_{\text{RC}}(s) = -\frac{1}{s\tau}$$

$$= -\frac{1}{2\pi j f_{RC} \tau}$$

SC Integrator

$$H_{\text{SC}}(z) = \frac{C_s}{C_{int}} \frac{z^{-1/2}}{1 - z^{-1}}$$

$$= -\frac{C_s}{C_{int}} \frac{1}{2j \sin \pi f_{SC} T_s}$$

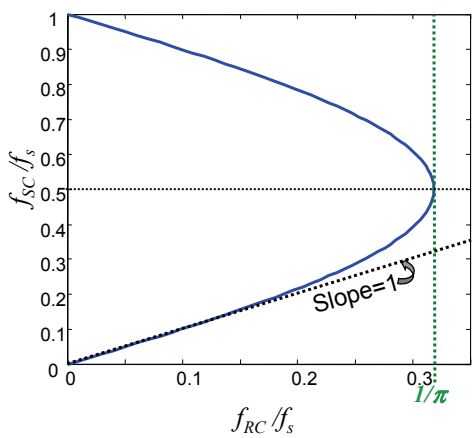
Identical time constants:

$$\tau = RC = \frac{C_{int}}{f_s C_s}$$

Set: $H_{RC}(f_{RC}) = H_{SC}(f_{SC})$ →

$$f_{RC} = \frac{f_s}{\pi} \sin\left(\pi \frac{f_{SC}}{f_s}\right)$$

LDI Integration



$$f_{RC} = \frac{f_s}{\pi}\sin\left(\pi\frac{f_{SC}}{f_s}\right)$$

- "RC" frequencies up to f_s/π map to physical (real) "SC" frequencies
- Frequencies above f_s/π do not map to physical frequencies
- Mapping is symmetric about $f_s/2$ (aliasing)
- "Accurate" only for $f_{RC} << f_s$

Material Covered in EE247 Where are We?

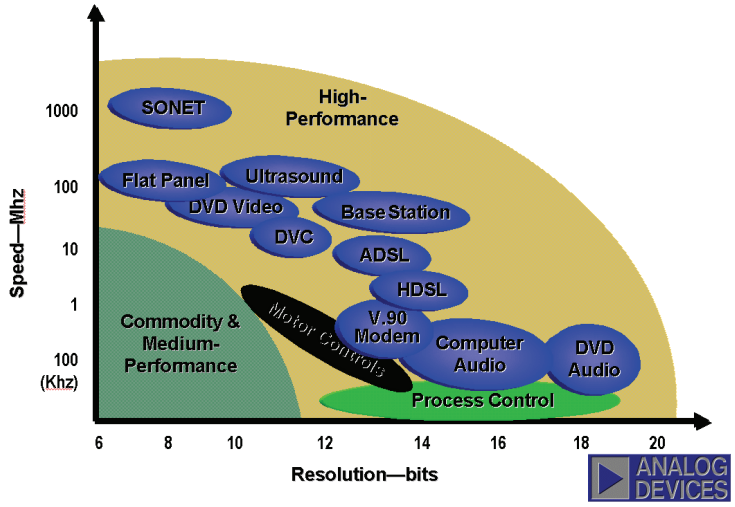
✓ Filters
- Continuous-time filters
  - Biquads & ladder type filters
  - Opamp-RC, Opamp-MOSFET-C, gm-C filters
  - Automatic frequency tuning
- Switched capacitor (SC) filters

- Data Converters
  - D/A converter architectures
  - A/D converter
    - Nyquist rate ADC- Flash, Pipeline ADCs,….
    - Oversampled converters
    - Self-calibration techniques
- Systems utilizing analog/digital interfaces

Data Converters

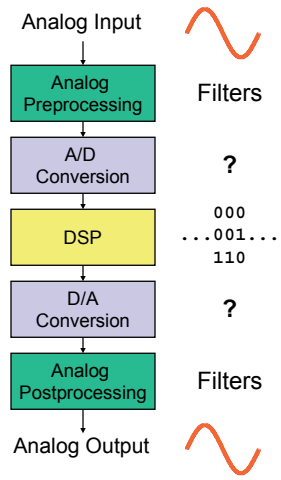
- Data converters
  - Areas of application
  - Data converter transfer characteristics
  - Sampling, aliasing, reconstruction
  - Amplitude quantization
  - Static converter error sources
    - Offset
    - Full-scale error
    - Differential non-linearity (DNL)
    - Integral non-linearity (INL)

Data Converter Applications

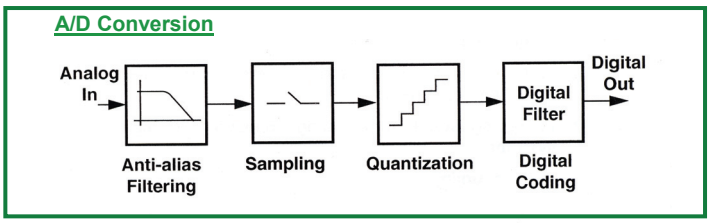


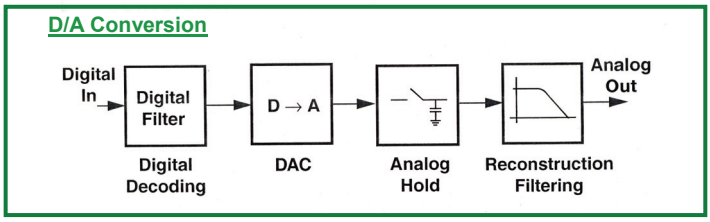
Data Converter Basics

- DSPs benefited from device scaling
- However, real world signals are still analog:
  - Continuous time
  - Continuous amplitude
- DSP can only process:
  - Discrete time
  - Discrete amplitude
    - → Need for data conversion from analog to digital and digital to analog



A/D & D/A Conversion





Data Converters

- Stand alone data converters
  - Used in variety of systems
  - Example: Analog Devices AD9235 12bit/ 65Ms/s ADC- Applications:
    - Ultrasound equipment
    - IF sampling in wireless receivers
    - Various hand-held measurement equipment
    - Low cost digital oscilloscopes

Data Converters

- Embedded data converters
  - Integration of data conversion interfaces along with DSPs and/or RF circuits → Cost, reliability, and performance
  - Main issues
    - Feasibility of integrating sensitive analog functions in a technology typically optimized for digital performance
    - Down scaling of supply voltage as a result of downscaling of feature sizes
    - Interference & spurious signal pick-up from on-chip digital circuitry and/or high frequency RF circuits
    - Portable applications dictate low power consumption

Embedded Converters
Example: Typical Cell Phone

Contains in integrated form:

- 4 Rx filters
- 4 Tx filters
- 4 Rx ADCs
- 4 Tx DACs

} Dual Standard, I/Q

- 3 Auxiliary ADCs
- 8 Auxiliary DACs

} Audio, Tx/Rx power control, Battery charge control, display, ...

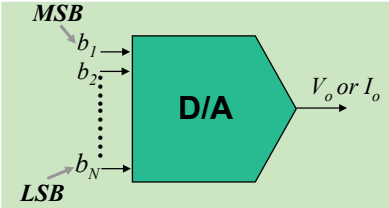
Total: Filters → 8

ADCs → 7

DACs → 12

D/A Converter Transfer Characteristics

- An ideal digital-to-analog converter:
  - Accepts digital inputs b_1-b_n
  - Produces either an analog output voltage or current
  - Assumption (will be revisited)
    - Uniform, binary digital encoding
    - Unipolar output ranging from 0 to V_{FS}



Nomenclature:

$N = \#\ of\ bits$

$V_{FS} = full\ scale\ output$

$\Delta = min.\ step\ size \rightarrow 1LSB$

$$\Delta = \frac{V_{FS}}{2^N}$$

$$or\ N = log_2 \frac{V_{FS}}{\Delta} \rightarrow resolution$$

D/A Converter Transfer Characteristics

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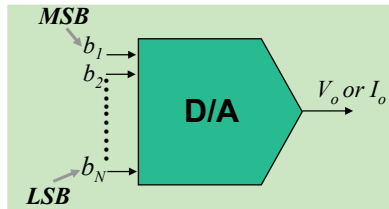


$$V_0 = V_{FS} \sum_{i=1}^{N} \frac{bi}{2^i}$$

$$= \Delta \times \underbrace{\sum_{i=1}^{N} bi \times 2^{N-i}}_{\text{binary-weighted}} \quad , \quad bi = 0 \ \ or \ \ 1$$

$Note: D(b_i = 1, all\ i)$

$\rightarrow V_o^{max} = V_{FS} - \Delta$

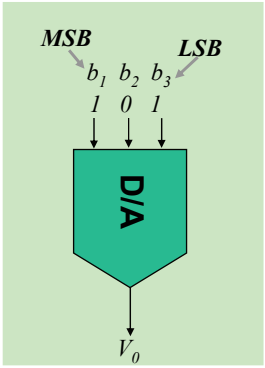
$\rightarrow V_o^{max} = V_{FS}\left(1 - \frac{1}{2^N}\right)$

D/A Converter
Exampe: D/A with 3-bit Resolution

Example: for $N=3$ and $V_{FS}=0.8V$

input code→ 101

Find the output value V_0



$V_0 = \Delta\left(b_1 \times 2^2 + b_2 \times 2^1 + b_3 \times 2^0\right)$

$Then: \Delta = V_{FS}/2^3 = 0.1V$

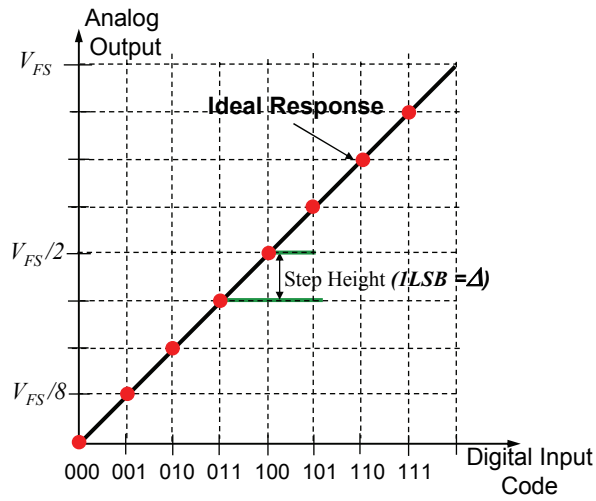
$\rightarrow V_0 = 0.1V\ (1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0) =$

$\rightarrow V_0 = 0.5V$

$Note: MSB \rightarrow V_{FS}/2 \quad \& \quad LSB \rightarrow V_{FS}/2^N$

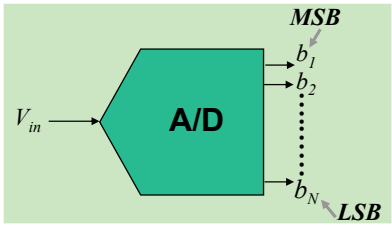
Ideal 3-Bit D/A Transfer Characteristic

- Ideal DAC introduces no error!
- One-to-one mapping from input to output



A/D Converter Transfer Characteristics

- An ideal analog-to-digital converter:
  - Accepts analog input in the form of either voltage or current
  - Produces digital output either in serial or parallel form
  - Assumption (will be revisited)
    - Unipolar input ranging from 0 to V_{FS}
    - Uniform, binary digital encoding



$$N = \#\ of\ bits$$

$$V_{FS} = full\ scale\ output$$

$$\Delta = min.\ resolvable\ input \rightarrow 1LSB$$

$$\Delta = \frac{V_{FS}}{2^N}$$

$$or\ N = log_2 \frac{V_{FS}}{\Delta} \rightarrow resolution$$

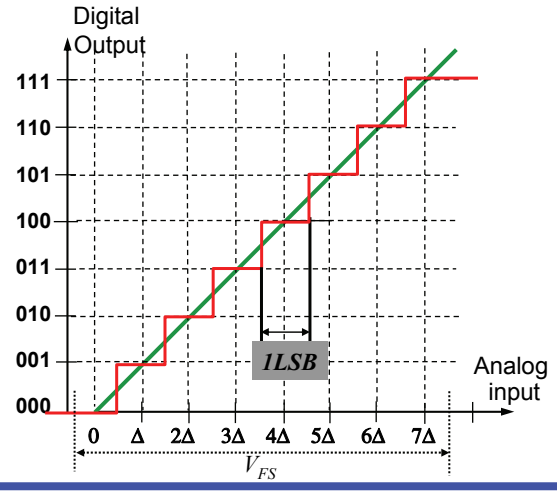
Ideal A/D Transfer Characteristic
Example: 3Bit A/D Converter

- Ideal ADC introduces error with max peak-to-peak:
  → $(+-1/2\ \Delta)$
  $\Delta = V_{FS}/2^N$

  $N = \#\ of\ bits$

- This error is called ``quantization error``

- For a given VFS as N increases quantization error decreases → resolution increases



Non-Linear Data Converters

- So far data converter characterisitics studied are with uniform, binary digital encoding

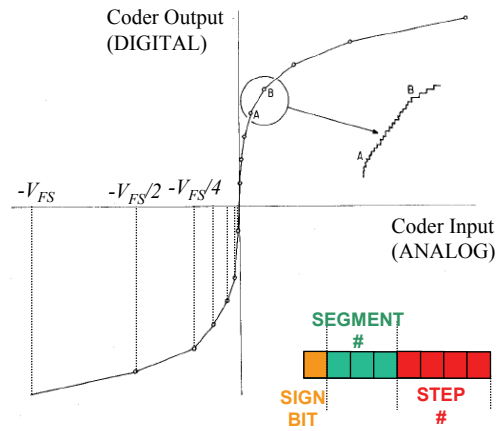
- For some applications to maximize dynamic range non-linear coding is used e.g. Voice-band telephony,
  - Small signals → larger # of codes
  - Large signals → smaller # of codes

Example: Non-Linear A/D Converter For Voice-Band Telephony Applications

Non-linear ADC and DAC used in voice-band CODECs

- To maximize dynamic range without need for large # of bits
- Non-linear Coding scheme called A-law & μ-law is used
- Also called companding

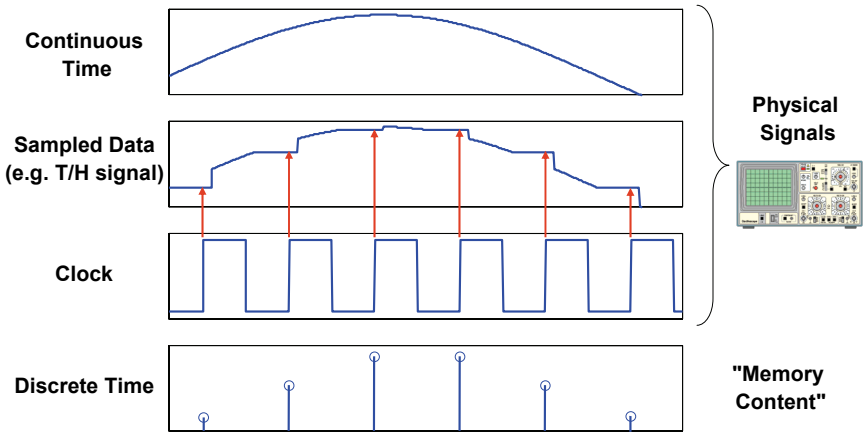
Ref: P. R. Gray, et al. "Companded pulse-code modulation voice codec using monolithic weighted capacitor arrays," *IEEE Journal of Solid-State Circuits,* vol. 10, pp. 497 - 499, December 1975.



Data Converter Performance Metrics

- Data Converters are typically characterized by static, time-domain, & frequency domain performance metrics :
  - Static
    - Offset
    - Full-scale error
    - Differential nonlinearity (DNL)
    - Integral nonlinearity (INL)
    - Monotonicity
  - Dynamic
    - Delay & settling time
    - Aperture uncertainty
    - Distortion- harmonic content
    - Signal-to-noise ratio (SNR), Signal-to-(noise+distortion) ratio (SNDR)
    - Idle channel noise
    - Dynamic range & spurious-free dynamic range (SFDR)

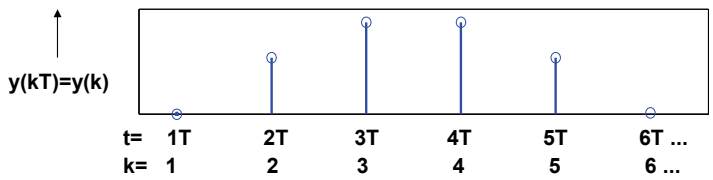
Typical Sampling Process
C.T. ⇒ S.D. ⇒ D.T.



Discrete Time Signals

- A sequence of numbers (or vector) with discrete index time instants
- Intermediate signal values <u>not defined</u> (not the same as equal to zero!)
- Mathematically convenient, non-physical
- We will use the term "*sampled data*" for related signals that occur in real, physical interface circuits

Uniform Sampling



- Samples spaced T seconds in time
- Sampling Period T ⇔ Sampling Frequency f_s=1/T
- Problem: Multiple continuous time signals can yield exactly the same discrete time signal (aliasing)

Data Converters

- ADC/DACs need to *sample/reconstruct* to convert from continuous-time to discrete-time signals and back
- Purely mathematical discrete-time signals are different from "sampled-data signals" that carry information in actual circuits
- Question: How do we ensure that sampling/reconstruction fully preserve information?

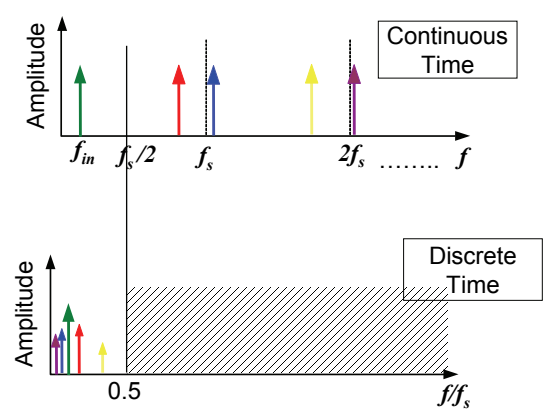
Aliasing

- The frequencies f_x and $nf_s \pm f_x$, n integer, are indistinguishable in the discrete time domain
- Undesired frequency interaction and translation due to sampling is called aliasing
- If aliasing occurs, no signal processing operation downstream of the sampling process can recover the original continuous time signal!

Frequency Domain Interpretation

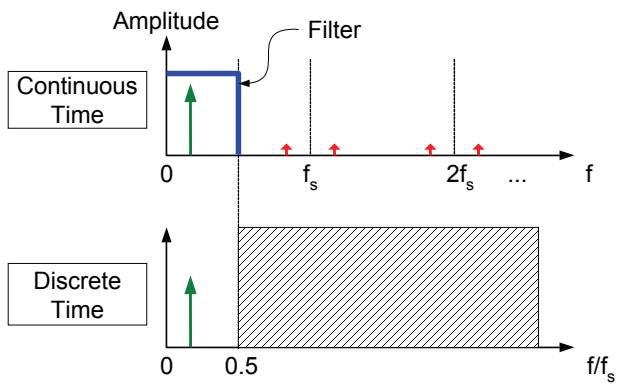
Signal scenario before sampling

Signal scenario after sampling → DT



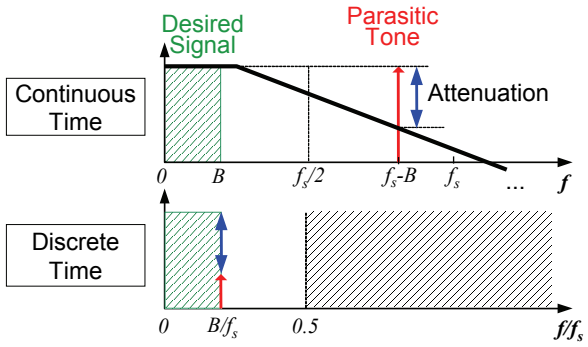
→Signals @ $nf_S \pm f_{max\_signal}$ fold back into band of interest → Aliasing

Brick Wall Anti-Aliasing Filter



Sampling at Nyquist rate (f_s=2f_{signal}) → required brick-wall anti-aliasing filters

Practical Anti-Aliasing Filter

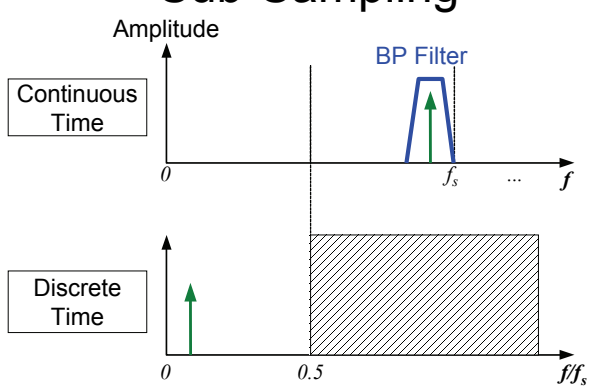


- Practical filter: Nonzero "transition band"
- In order to make this work, we need to sample faster than 2x the signal bandwidth
- "Oversampling"

Data Converter Classification

- $f_s > 2f_{max}$ Nyquist Sampling
  - "Nyquist Converters"
  - Actually always slightly oversampled (e.g. CODEC $f_{sig}^{max} = 3.4kHz$ & ADC sampling $8kHz \rightarrow f_s/f_{max} = 2.35$)
  - Requires anti-aliasing filtering prior to A-to-D conversion
- $f_s >> 2f_{max}$ Oversampling
  - "Oversampled Converters"
  - Anti-alias filtering is often trivial
  - Oversampling is also used to reduce quantization noise, see later in the course...
- $f_s < 2f_{max}$ Undersampling (sub-sampling)

Sub-Sampling



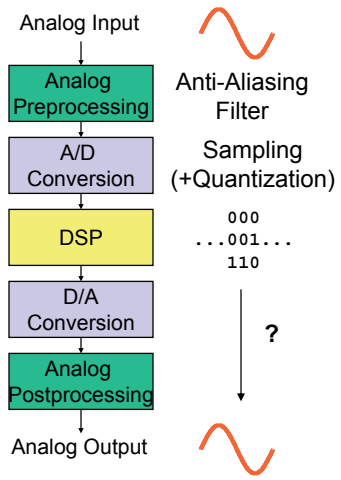
- Sub-sampling → sampling at a rate less than Nyquist rate → aliasing
- For signals centered @ an intermediate frequency → Not destructive!
- Sub-sampling can be exploited to mix a narrowband RF or IF signal down to lower frequencies

Nyquist Data Converter Topics

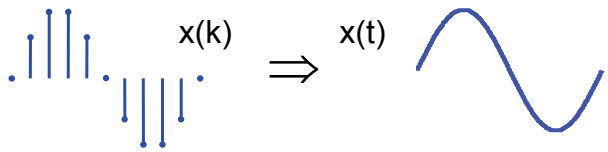
- Basic operation of data converters
  - Uniform sampling and reconstruction
  - Uniform amplitude quantization
- Characterization and testing
- Common ADC/DAC architectures
- Selected topics in converter design
  - Practical implementations
  - Compensation & calibration for analog circuit non-idealities
- Figures of merit and performance trends

Where Are We Now?

- We now know how to preserve signal information in CT→DT transition
- How do we go back from DT→ CT?



Ideal Reconstruction

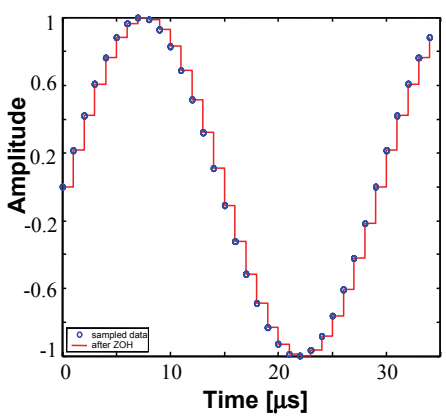


- The DSP books tell us:

$$x(t) = \sum_{k=-\infty}^{\infty} x(k) \cdot g(t - kT) \qquad g(t) = \frac{\sin(2\pi Bt)}{2\pi Bt}$$

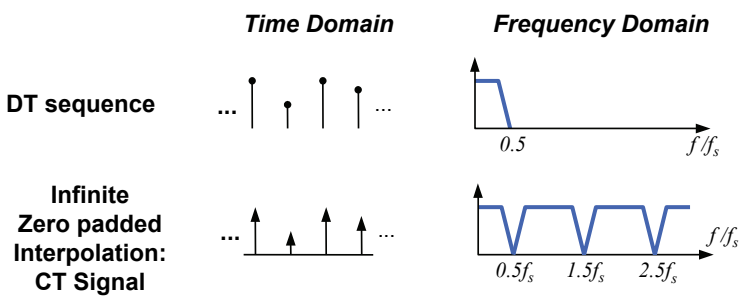
- Unfortunately not all that practical...

Zero-Order Hold Reconstruction



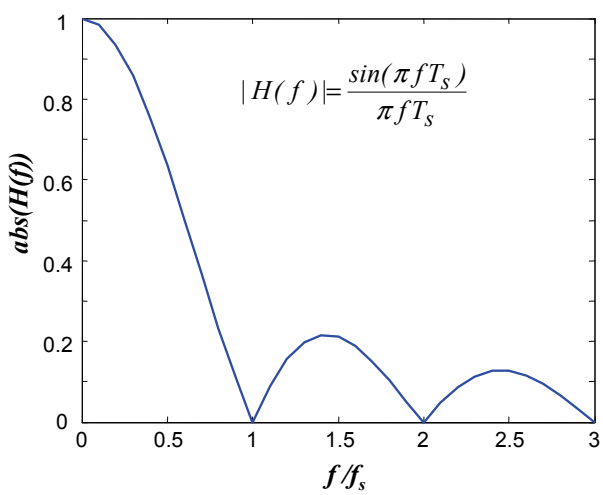
- How about just creating a staircase, i.e. hold each discrete time value until new information becomes available?
- What does this do to the frequency content of the signal?
- Let's analyze this in two steps...

DT→ CT: Infinite Zero Padding

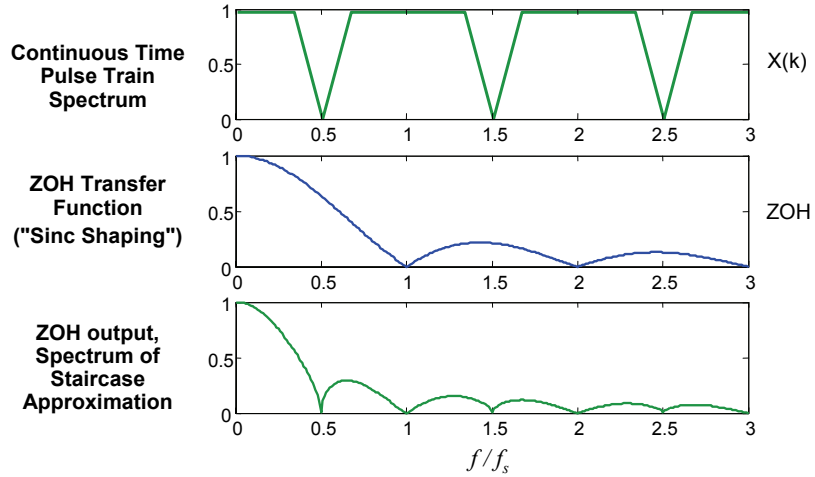


Next step: pass the samples through a sample & hold stage (ZOH)

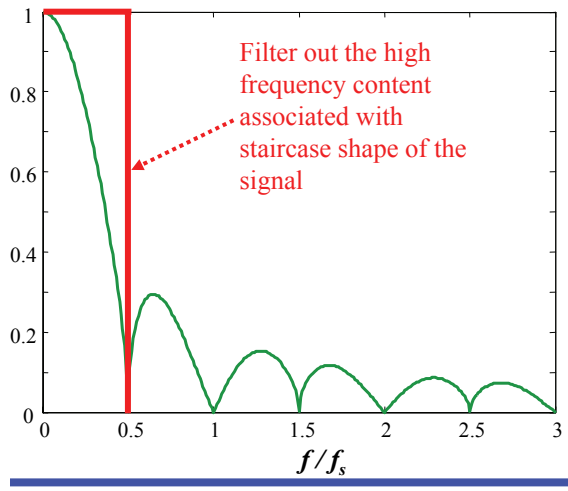
Hold Pulse $T_p = T_s$ Transfer Function



ZOH Spectral Shaping



Smoothing Filter



- Order of the filter required is a function of oversampling ratio
- High oversampling helps reduce filter order requirement

Summary

- Sampling theorem $f_s > 2f_{max}$, usually dictates anti-aliasing filter
- If theorem is met, CT signal can be recovered from DT without loss of information
- ZOH and smoothing filter reconstruct CT signal from DT vector
- Oversampling helps reduce order & complexity of anti-aliasing & smoothing filters