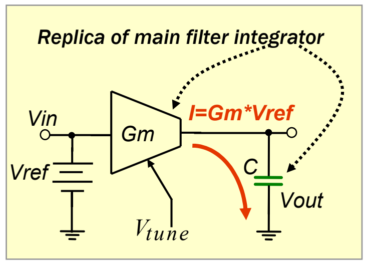
EE247
Lecture 7

- Automatic on-chip filter tuning (continued from last lecture)
  - Continuous tuning (continued)
    - Reference integrator locked to reference frequency
    - DC tuning of resistive timing element
  - Periodic digitally assisted filter tuning
    - Systems where filter is followed by ADC & DSP, existing hardware can be used to periodically update filter freq. response
- Continuous-time filters
  - Highpass filters
  - Bandpass filters
    - Lowpass to bandpass transformation
    - Example: 6^{th} order bandpass filter
    - Gm-C BP filter using simple diff. pair

Summary last lecture

- Continuous-time filters
  - Opamp MOSFET-RC filters
  - Gm-C filters
- Frequency tuning for continuous-time filters
  - Trimming via fuses or laser
  - Automatic on-chip filter tuning
    - Continuous tuning
      - Utilizing VCF built with replica integrators
      - Use of VCO built with replica integrators
      - To be continued………..

Master-Slave Frequency Tuning
3-Reference Integrator Locked to Reference Frequency

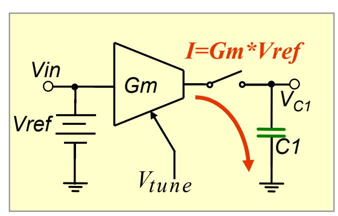


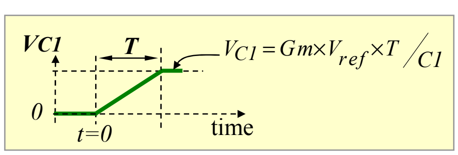
- Replica of main filter building block e.g. *Gm-C* integrator used
- Utilizes the fact that a DC voltage source connected to the input of the Gm cell generates a constant current at the output proportional to the transconductance and the voltage reference

$$I = Gm.Vref$$

Reference Integrator Locked to Reference Frequency

- Consider the following sequence:
  - Integrating capacitor is fully discharged @ $t=0$
  - At $t=0$ the capacitor is connected to the output of the Gm cell for T amount of time then:



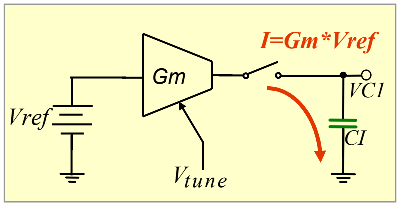


$$Q_{C1} = V_{C1} \times C1 = Gm \times V_{ref} \times T$$
$$\rightarrow V_{C1} = Gm \times V_{ref} \times T / C1$$

Reference Integrator Locked to Reference Frequency

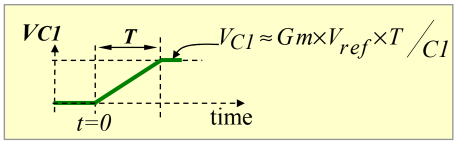
Since at the end of the period T:

$$V_{C1} \approx Gm \times V_{ref} \times T \big/ C1$$



If V_{CI} is forced to be equal to V_{ref} then:

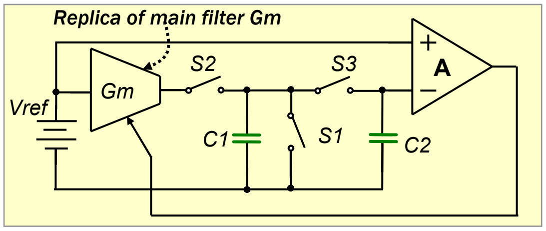
$$\frac{C}{Gm} = T = \frac{N}{f_{clk}}$$



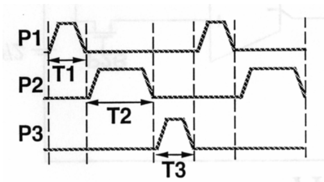
How do we manage to force $V_{CI}=V_{ref}$?

→ **Use feedback!!**

Reference Integrator Locked to Reference Frequency

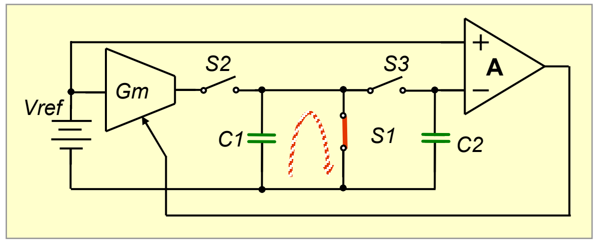


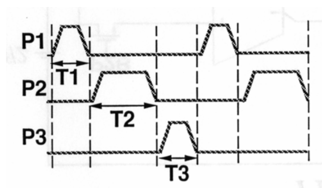
- Three clock phase operation
- To analyze → study one phase at a time



Ref: A. Durham, J. Hughes, and W. Redman- White, "Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering," *IEEE Transactions on Circuits and Systems,* pp. 651-657, Sept. 1992.

Reference Integrator Locked to Reference Frequency
P1 high→ S1 closed

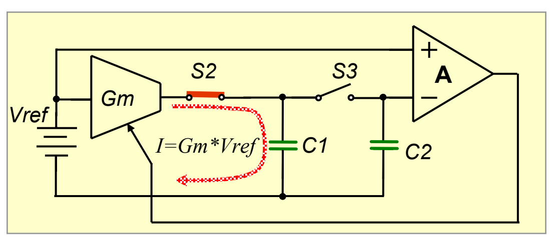




C1 → discharged → $V_{C1}=0$

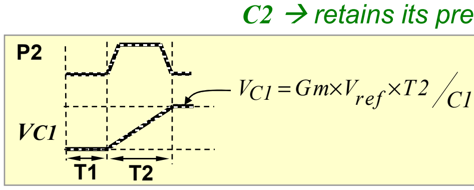
C2 → *retains its previous charge*

Reference Integrator Locked to Reference Frequency
P2 high → S2 closed

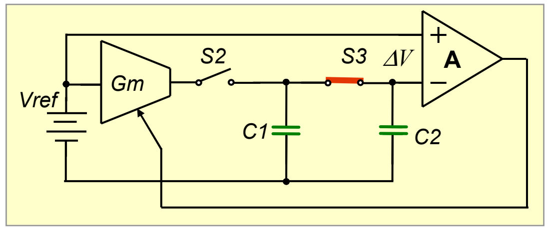


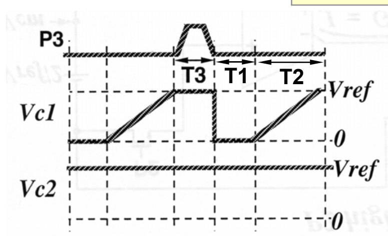
C1 → charged with constant current: $I=Gm*Vref$

C2 → *retains its previous charge*



Reference Integrator Locked to Reference Frequency
P3 high → S3 closed



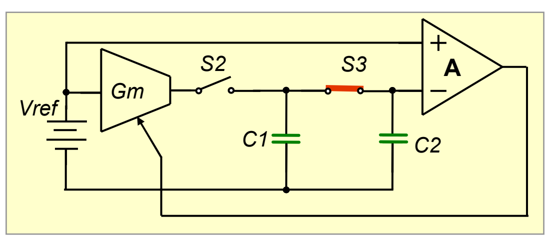


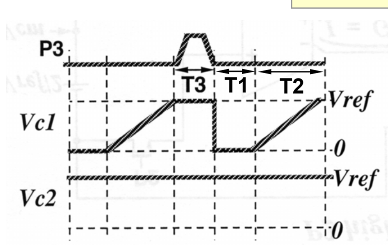
C1 charge shares with C2
Few cycles following startup
Assuming A is large, feedback forces:

$\Delta V \rightarrow 0$

$\rightarrow V_{C2} = V_{ref}$

Reference Integrator Locked to Reference Frequency
P3 high → S3 closed





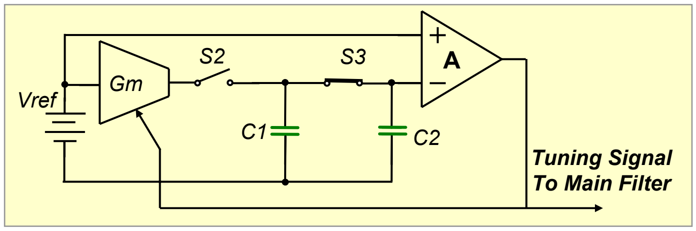
$V_{C1} = V_{C2} = Vref$

$since: V_{C1} = Gm \times V_{ref} \times T2 / C1$

$then: V_{ref} = Gm \times V_{ref} \times T2 / C1$

$or: \quad C1 / Gm = T2 = N / fclk$

Summary
Replica Integrator Locked to Reference Frequency

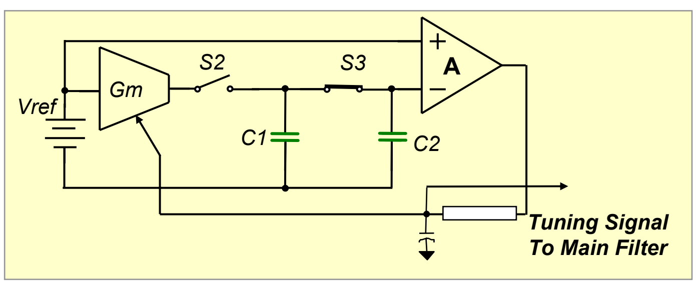


Feedback forces Gm to assume a value so that :

- Integrator time constant locked to an accurate frequency
- Tuning signal used to adjust the time constant of the main filter integrators

$$\tau_{intg} = C1/Gm = N/fclk$$
or
$$\omega_0^{intg} = Gm/C1 = fclk/N$$

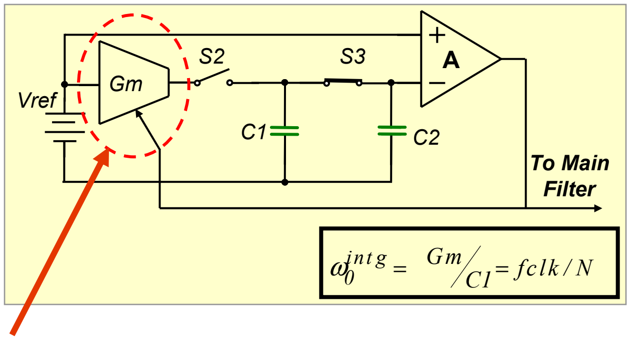
Issues
1- Loop Stability



- Note: Need to pay attention to loop stability
  - ✓C1 chosen to be smaller than C2 – tradeoff between stability and speed of lock acquisition
  - ✓Lowpass filter at the output of amplifier (A) helps stabilize the loop

Issues
2- GM-Cell DC Offset Induced Error

Problems to be aware of:



$$\omega_0^{intg} = \frac{Gm}{C1} = fclk/N$$

→ **Tuning error due to master integrator DC offset**

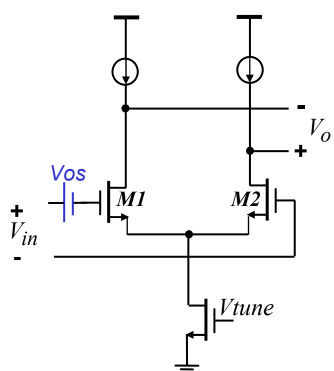
Issues
Gm Cell DC Offset

What is DC offset?

Simple example:

For the differential pair shown here, mismatch in input device or load characteristics would cause DC offset:
→ $Vo = 0$ requires a non-zero input voltage

Offset could be modeled as a small DC voltage source at the input for which with shorted inputs→ $Vo = 0$



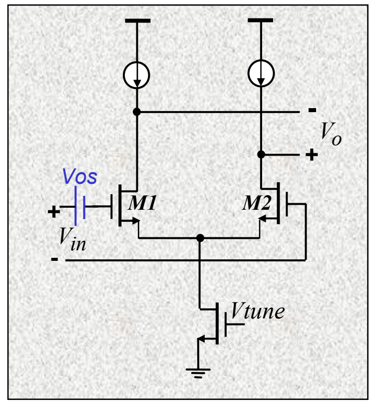
Example: Differential Pair

Simple Gm-Cell DC Offset

Mismatch associated with M1 & M2
→ DC offset

$$V_{os} = (V_{th1} - V_{th2}) - \frac{1}{2} V_{ov1,2} \frac{\Delta (W/L)_{M1,2}}{(W/L)_{M1,2}}$$

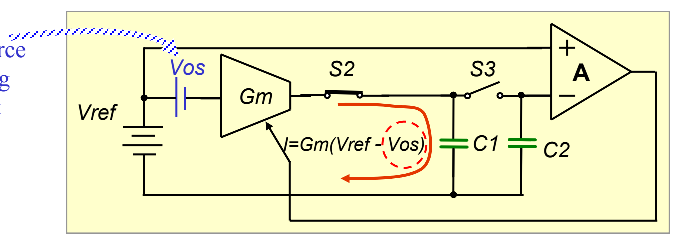
Assuming offset due to load device mismatch is negligible



Ref: Gray, Hurst, Lewis, Meyer, *Analysis & Design of Analog Integrated Circuits*, Wiley 2001, page 335

Gm-Cell Offset Induced Error

Voltage source representing DC offset



•Effect of Gm-cell DC offset:

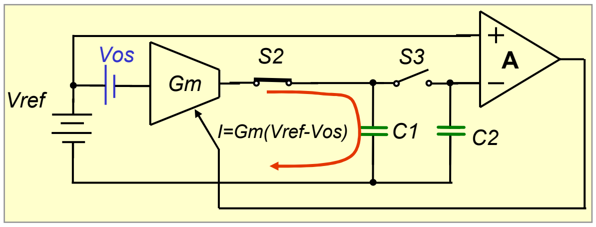
$$V_{C1} = V_{C2} = Vref$$

$$Ideal: V_{C1} = Gm \times V_{ref} \times T2 / C1$$

$$with\ offset: V_{C1} = Gm \times (V_{ref} - V_{os}) \times T2 / C1$$

$$or: C1/Gm = T2 \left(1 - \frac{V_{os}}{V_{ref}} \right)$$

Gm-Cell Offset Induced Error



- Example:

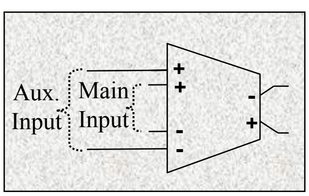
$$C1/_{Gm} = T2\left(1 - \frac{V_{os}}{V_{ref}}\right) \quad \& \quad f_{critical} \propto Gm/_{C1}$$

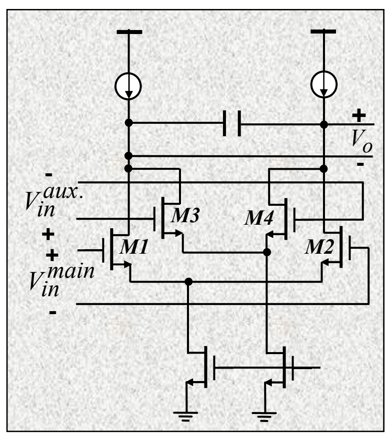
$$for\ \frac{V_{os}}{V_{ref}} = 1/10 \quad \rightarrow \quad C1/_{Gm} = 0.9T2 = 0.9\frac{N}{fclk}$$

10% error in tuning!

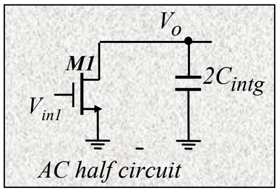
Gm-Cell Tuning Offset Induced Error Solution

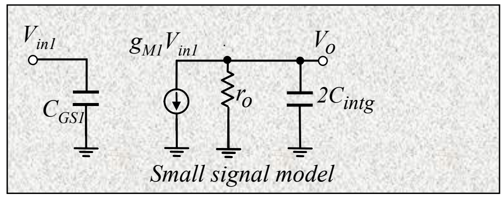
- Assuming differential integrator
- Add a pair of auxiliary inputs to the input stage for offset cancellation purposes





Simple Gm-Cell
AC Small Signal Model



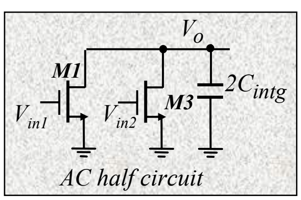


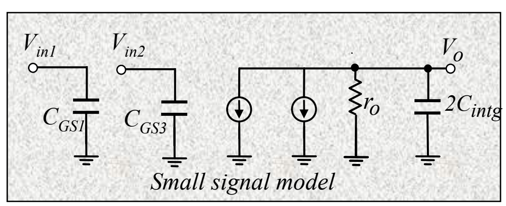
$V_o = \left(g_m^{M1} V_{in1}\right)\left(r_o \,||\, 1/s\times 2C_{intg}\right)$ *r_o is parallel combination of r_o of M1 & load*

$V_o = \frac{-g_m^{M1} r_o}{1+s\times 2C_{intg} r_o} V_{in1}$ *& $g_m^{M1} r_o = a1 \rightarrow$ Integrator finite DC gain*

$V_o = \frac{-a1}{1+\frac{a1\times s\times 2C_{intg}}{g_m^{M1}}} V_{in1}$ *Note: $a1 \rightarrow \infty$,* $V_o = \frac{-g_m^{M1}}{s\times 2C_{intg}} V_{in1}$

Simple Gm-Cell + Auxiliary Inputs
AC Small Signal Model



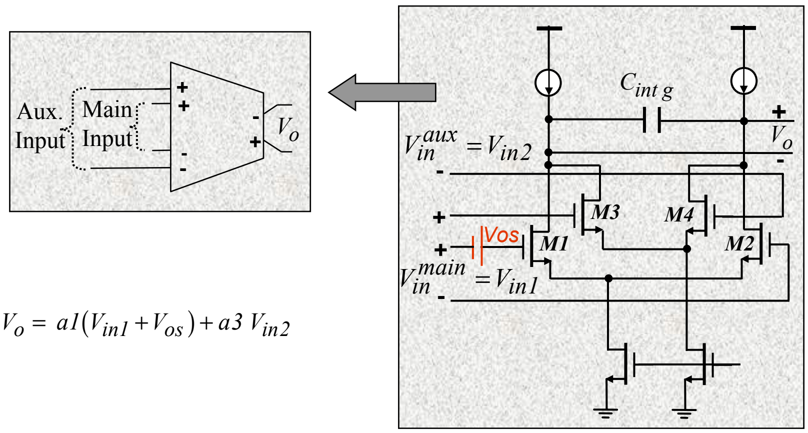


$V_o = \left(g_m^{M1} V_{in1} + g_m^{M3} V_{in2}\right)\left(r_o \,||\, 1/s\times 2C_{intg}\right)$ *r_o parallel combination of r_o of M1, M3, & current source*

$V_o = \frac{-g_m^{M1} r_o}{1+s\times 2C_{intg} r_o} V_{in1} - \frac{g_m^{M3} r_o}{1+s\times 2C_{intg} r_o} V_{in2}$

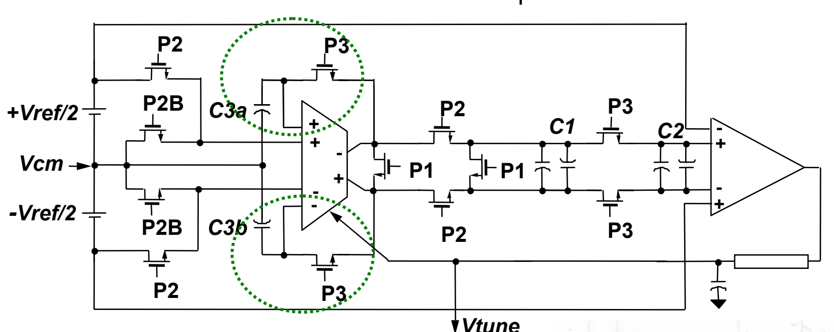
$V_o = \frac{-a1}{1+\frac{a1\times s\times 2C_{intg}}{g_m^{M1}}} V_{in1} - \frac{a3}{1+\frac{a3\times s\times 2C_{intg}}{g_m^{M3}}} V_{in2}$

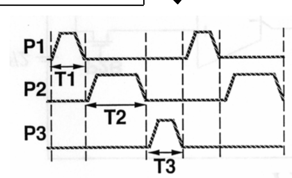
Gm-Cell
DC Model



$$V_o = a1(V_{in1} + V_{os}) + a3\,V_{in2}$$

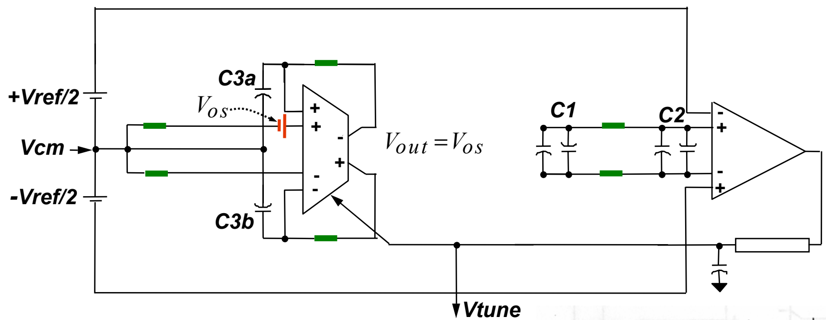
Reference Integrator Locked to Reference Frequency
Offset Cancellation Incorporated

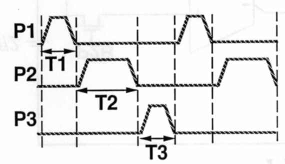




Gm-cell → two sets of input pairs
Aux. input pair + *C3a,b* → Offset cancellation
Same clock signals

Reference Integrator Locked to Reference Frequency
P3 High (Update & Store offset)





Gm-cell → Unity gain configuration via aux. inputs
Main inputs shorted
C1, C2 → Charge sharing

Reference Integrator During Offset Cancellation Phase

$$V_o = a1(V_{in1} + V_{os}) + a3\,V_{in2} \quad (V_{in1} \rightarrow 0)$$

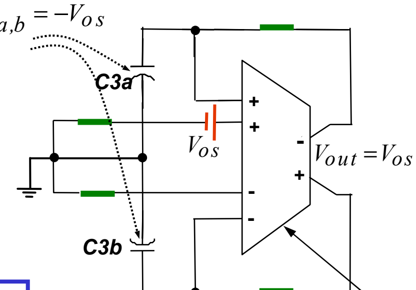
$$V_{in2} = -V_o$$

$$V_o = a1 \times V_{os} - a3 \times V_o$$

$$\rightarrow V_o = \frac{a1}{1 + a3} \times V_{os}$$

Assuming $a1 = a3 >> 1$

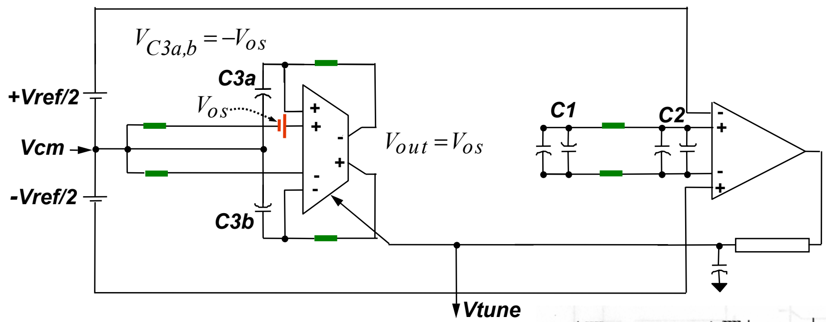
$V_{C3a,b} = -V_{os}$

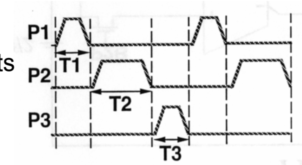


$V_o = V_{os}$ & $V_{in2} = -V_{os}$

C3a,b → Store main Gm-cell offset

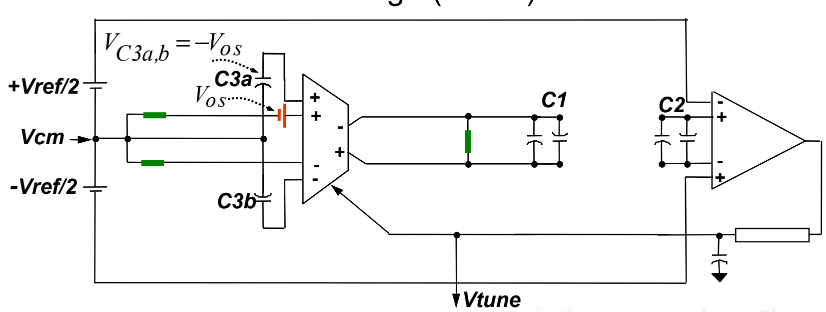
Reference Integrator Locked to Reference Frequency
P3 High (Update & Store offset)

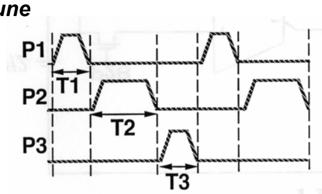




Gm-cell → Unity gain configuration via aux. inputs
Main input shorted
C3a,b → Store Gm-cell offset
C1, C2 → Charge sharing

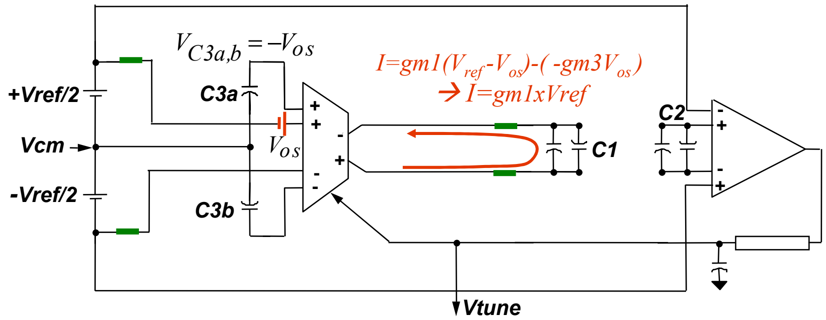
Reference Integrator Locked to Reference Frequency
P1 High (Reset)





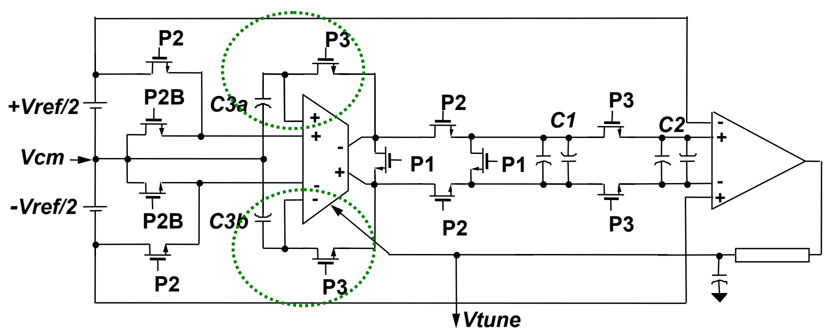
Gm-cell → Reset.
C1 → Discharge
C2 → Hold Charge
C3a,b → Hold Charge
→Offset previously stored on C3a,b cancels gm-cell offset

Reference Integrator Locked to Reference Frequency P2 High (Charge)



Gm-cell → Charging C1
C3a,b → Store/hold Gm-cell offset
C2 → Hold charge

Reference Integrator Locked to Reference Frequency



Key point: Tuning error due to Gm-cell offset cancelled
*Note: Same offset compensation technique can be used in many other applications

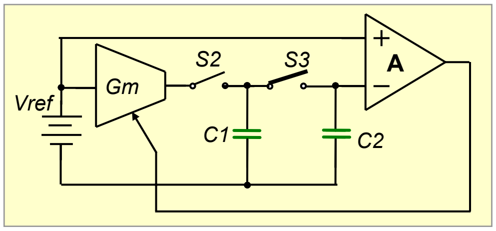
Summary
Reference Integrator Locked to Reference Frequency

Tuning error due to gm-cell offset voltage resolved

Advantage over previous schemes:

→ f_{clk} can be chosen to be at much higher frequencies compared to filter bandwidth $(N > 1)$

→ Feedthrough of clock falls out of band and thus attenuated by filter



Feedback forces Gm to vary so that :

$$\tau_{intg} = C1/Gm = N/fclk$$

or

$$\omega_0^{intg} = Gm/C1 = fclk/N$$

DC Tuning of Resistive Timing Element

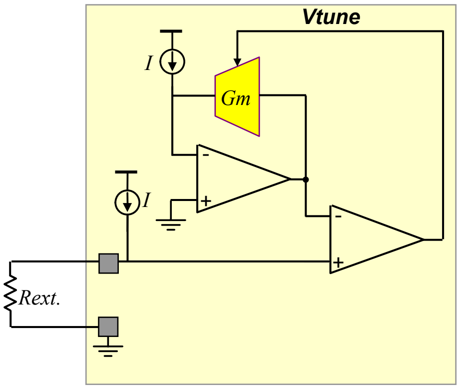
Tuning circuit Gm → replica of Gm used in filter

Rext used to lock Gm to accurate off-chip R

Feedback forces:
Gm=1/Rext

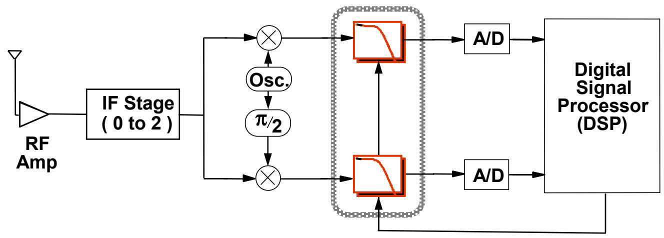
Issues with DC offset

Account for capacitor variations in this gm-C implementation by trimming in the factory



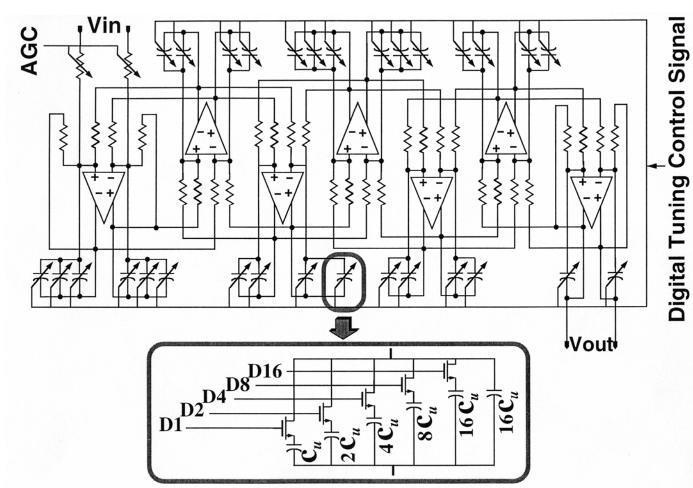
Ref: C. Laber and P.R. Gray, "A 20MHz 6th Order BiCMOS Parasitic Insensitive Continuous-time Filter and Second Order Equalizer Optimized for Disk Drive Read Channels," *IEEE Journal of Solid State Circuits,* Vol. 28, pp. 462-470, April 1993

Digitally Assisted Frequency Tuning Example:Wireless Receiver Baseband Filters



- Systems where filter is followed by ADC & DSP
  - Take advantage of existing digital signal processor capabilities to periodically test & if needed update the filter critical frequency
  - Filter tuned only at the outset of each data transmission session (off-line/periodic tuning) – can be fine tuned during times data is not transmitted or received

Example: Seventh Order Tunable Low-Pass OpAmp-RC Filter



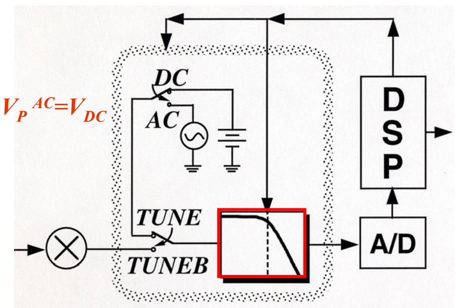
Digitally Assisted Filter Tuning Concept

Assumptions:

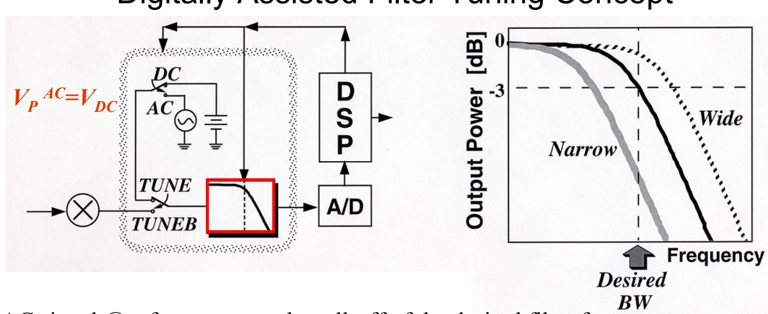
– System allows a period of time for the filter to undergo tuning (e.g. for a wireless transceiver during idle periods)

– An AC (e.g. a sinusoid) signal can be generated on-chip whose amplitude is a function of an on-chip DC voltage

- AC signal generator outputs a sinusoid with peak voltage equal to the DC signal source
- AC Signal Power =1/2 DC signal power @ the input of the filter



Digitally Assisted Filter Tuning Concept



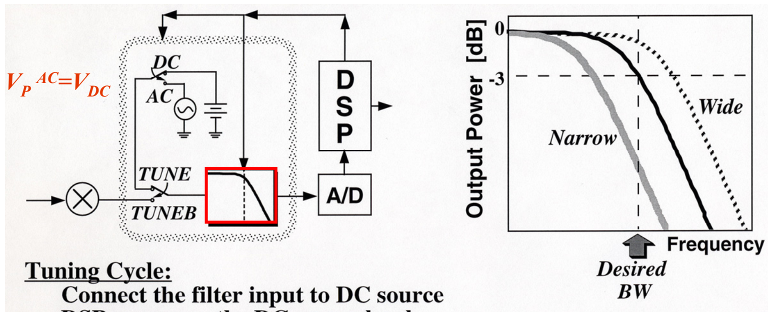
AC signal @ a frequency on the roll-off of the desired filter frequency response (e.g. -3dB frequency) $V_{AC} = V_{DC} \times sin\left(2\pi f_{-3dB}^{desired}\ t\right)$

Provision can be made → during the tuning cycle, the input of the filter is disconnected from the previous stage (e.g. mixer) and connected to:

1. DC source
2. AC source

under the control of the DSP

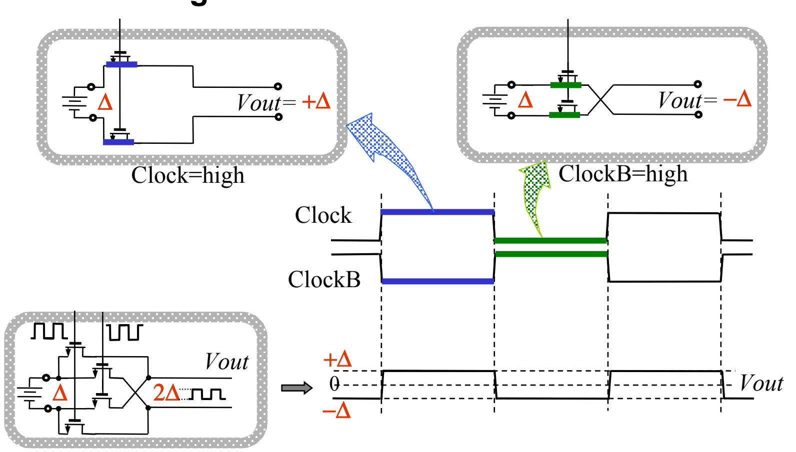
Digitally Assisted Filter Tuning Concept



Tuning Cycle:

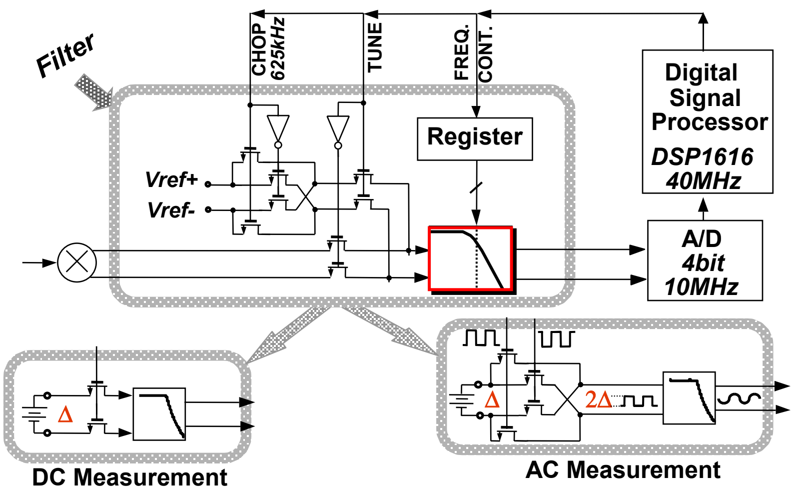
Connect the filter input to DC source
DSP measures the DC power level
Connect the filter input to AC souce (freq. -> desired -3dB freq.)
DSP measures the AC signal power level
If DC = 4*AC
Then filter is tuned
Else If DC > 4*AC
Then widen the filter bandwidth & repeat
Else narrow the filter bandwidth & repeat

Practical Implementation of Frequency Tuning AC Signal Generation From DC Source

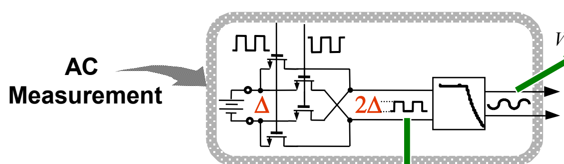


Square waveform generated → 2Δ peak to peak magnitude and @ frequency=f_{clock}

Practical Implementation of Frequency Tuning



Practical Implementation of Frequency Tuning
Effect of Using a Square Waveform



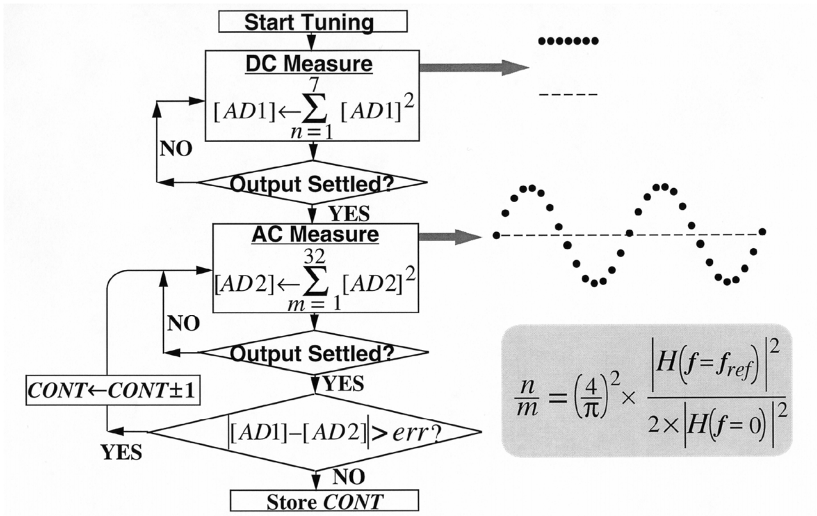
$$Vout(t) = \frac{4\Delta}{\pi} sin(\omega t) \times \frac{1}{\sqrt{2}}$$

$$Vin(t) = \frac{4}{\pi} \sum_{n=1,3,5,..}^{\infty} \frac{\Delta}{n} sin(n\omega t)$$

- Input signal chosen to be a square wave due to ease of generation
- Filter input signal comprises a sinusoidal waveform @ the fundamental frequency + its odd harmonics:

Key Point: The filter itself attenuates unwanted odd harmonics
→ Inaccuracy incurred by the harmonics negligible

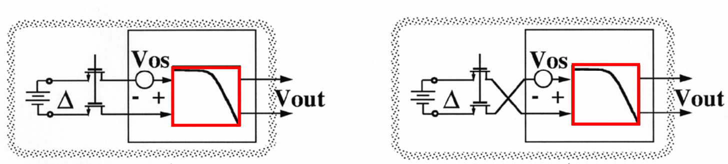
Simplified Frequency Tuning Flowchart



Digitally Assisted Offset Compensation

In cases where the filter DC offset cause significant error in tuning (i.e. high passband gain)

- **Offset compensation needed:**
  - ➪**DC measurement performed in two steps:**



Vout1 = A (Δ + Vos) **Vout2 = A (- Δ + Vos)**

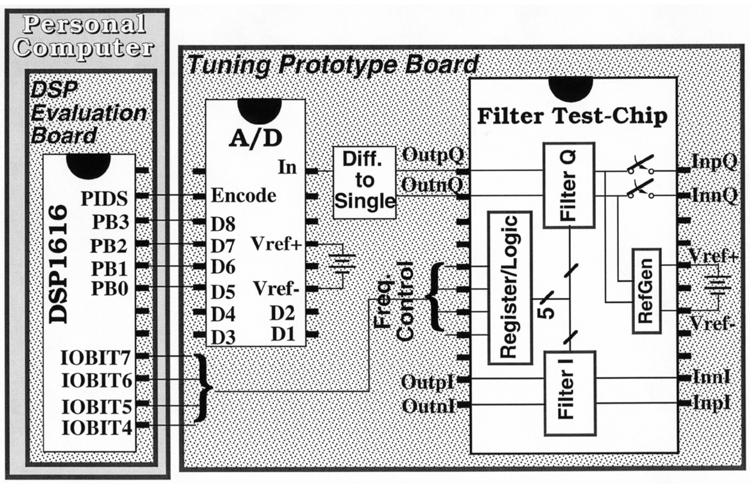
Passband Gain

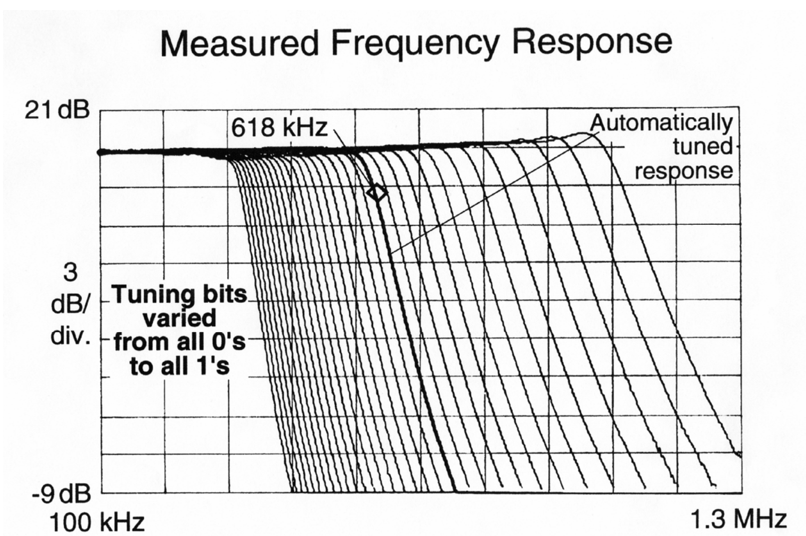
➪**DSP extracts: Offset component ➜ 1/2(Vout1 + Vout2) = A . Vos**

DC component ➜ 1/2(Vout1 - Vout2) = A . Δ

➪**DSP substracts Vos from all subsequent AC measurement**

Filter Tuning Prototype Diagram





Chip Photo

Measured Tuning Characteristics

Tunable frequency range (nom. process)		**370kHz to 1.1MI**
Variations due to process		**±50%**
I/Q bandwidth imbalance		**0.1%**
Tuning resolution	***Measured***	**3.8%**
(620kHz frequency range)	***Expected***	**2-5%**
Tuning time	***Coarse+Fine***	**max. 800µsec**
	Fine only	**min. 50µsec**
Memory space required for tuning routine		**250 byte**

Off-line Digitally Assisted Tuning

- Advantages:
  - No reference signal feedthrough since tuning does not take place during data transmission (off-line)
  - Minimal additional hardware
  - Small amount of programming
- Disadvantages:
  - If acute temperature change during data transmission, filter may slip out of tune!
    - Can add fine tuning cycles during periods of data is not transmitted or received

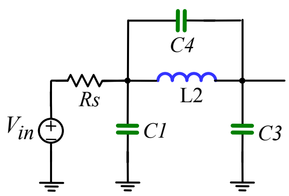
Ref: H. Khorramabadi, M. Tarsia and N.Woo, "Baseband Filters for IS-95 CDMA Receiver Applications Featuring Digital Automatic Frequency Tuning," *1996 International Solid State Circuits Conference*, pp. 172-173.

Summary: Continuous-Time Filter Frequency Tuning

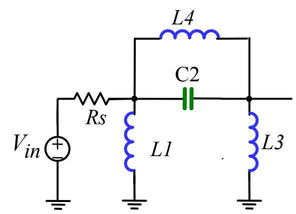
- Trimming
  - Expensive & does not account for temperature and supply etc… variations
- Automatic frequency tuning
  - Continuous tuning
    - Master VCF used in tuning loop, same tuning signal used to tune the slave (main) filter
      - Tuning quite accurate
      - Issue → reference signal feedthrough to the filter output
    - Master VCO used in tuning loop
      - Design of reliable & stable VCO challenging
      - Issue → reference signal feedthrough
    - Single integrator in negative feedback loop forces time-constant to be a function of accurate clock frequency
      - More flexibility in choice of reference frequency → less feedthrough issues
    - DC locking of a replica of the integrator to an external resistor
      - DC offset issues & does not account for integrating capacitor variations
  - Periodic digitally assisted tuning
    - Requires digital capability + minimal additional hardware
    - Advantage of no reference signal feedthrough since tuning performed off-line

RLC Highpass Filters

- Any RLC lowpass can be converted to highpass by:
  - Replacing all Cs by Ls and $L_{Norm}^{HP} = 1/C_{Norm}^{LP}$
  - Replacing all Ls by Cs and $C_{Norm}^{HP} = 1/L_{Norm}^{LP}$
  - $L^{HP}=L_r/C_{Norm}^{LP}$, $C^{HP}=C_r/L_{Norm}^{LP}$ where $L_r=R_r/\omega_r$ and $C_r=1/(R_r\omega_r)$



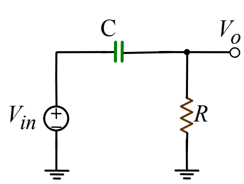
Lowpass



Highpass

Integrator Based High-Pass Filters
1st Order

- Conversion of simple high-pass RC filter to integrator-based type by using signal flowgraph technique



$$\frac{V_o}{V_{in}} = \frac{sRC}{1+sRC}$$

1^{st} Order Integrator Based High-Pass Filter Signal Flowgraph

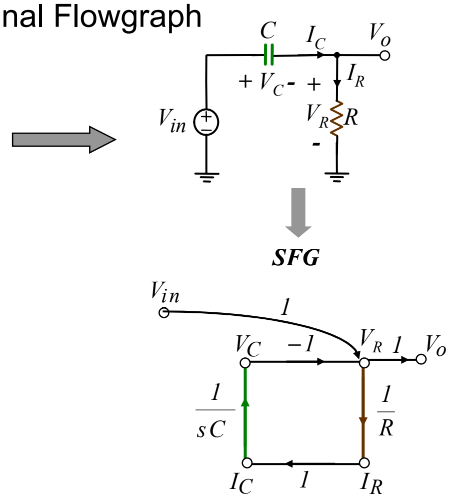
$V_R = V_{in} - V_C$

$V_C = I_C \times \frac{1}{sC}$

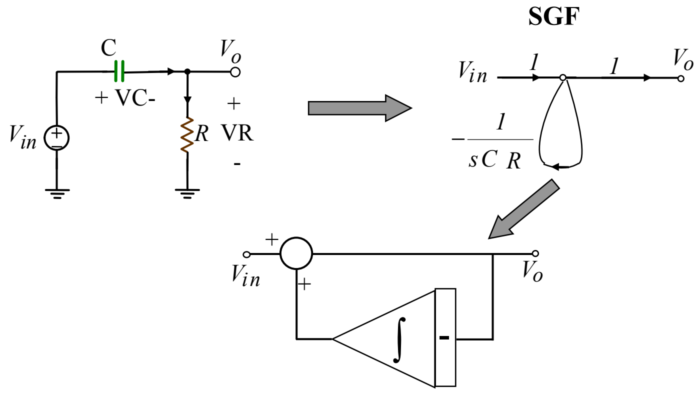
$V_o = V_R$

$I_R = V_R \times \frac{1}{R}$

$I_C = I_R$



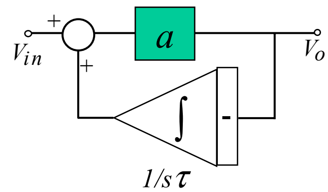
1^{st} Order Integrator Based High-Pass Filter SGF



Note: Addition of an integrator in the feedback path → High pass frequency shaping

Addition of Integrator in Feedback Path

Let us assume flat gain in forward path (a)
Effect of addition of an integrator in the feedback path:



$$\frac{V_o}{V_{in}} = \frac{a}{1+af}$$

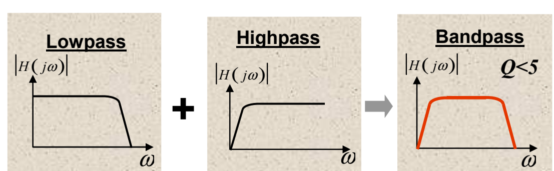
$$\frac{V_o}{V_{in}} = \frac{a}{1+a/s\tau} = \frac{s\tau}{1+s\tau/a}$$

$$\rightarrow zero@DC \quad \& \quad pole@ \quad \omega_{pole} = -\frac{a}{\tau} = -a\times\omega_0^{intg}$$

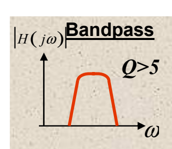
Note: For large forward path gain, a, can implement high pass function with high corner frequency
Addition of an integrator in the feedback path → zero @ DC + pole @ $a\times\omega_0^{intg}$
This technique used for offset cancellation in systems where the low frequency content is not important and thus disposable

Bandpass Filters

- Bandpass filters → two cases:
  1- Low Q or wideband ($Q < 5$)
  → Combination of lowpass & highpass



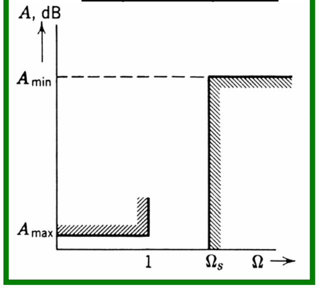
  2- High Q or narrow-band ($Q > 5$)
  → Direct implementation



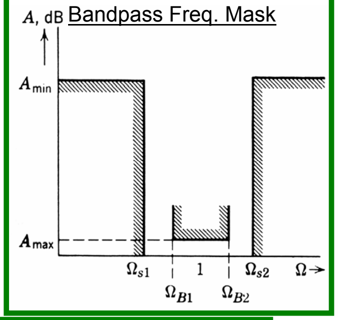
Narrow-Band Bandpass Filters
Direct Implementation

- Narrow-band BP filters → Design based on lowpass prototype
- Same tables used for LPFs are also used for BPFs

Lowpass Freq. Mask



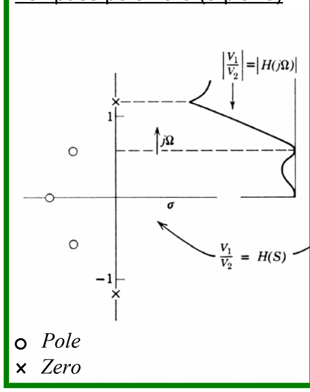
Bandpass Freq. Mask



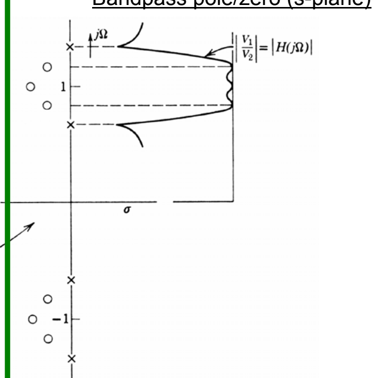
$$s \Rightarrow Q \times \left[\frac{s}{\omega_c} + \frac{\omega_c}{s} \right] \qquad \frac{\Omega_s}{\Omega_c} \Rightarrow \frac{\Omega_{s2} - \Omega_{s1}}{\Omega_{B2} - \Omega_{B1}}$$

Lowpass to Bandpass Transformation

Lowpass pole/zero (s-plane)



Bandpass pole/zero (s-plane)

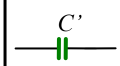
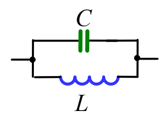
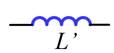
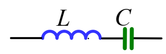


From: Zverev, *Handbook of filter synthesis*, Wiley, 1967- p.156.

Lowpass to Bandpass Transformation Table

Lowpass RLC filter structures & tables used to derive bandpass filters

$$Q = Q_{filter}$$

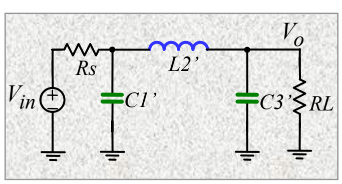
LP	BP	BP Values
		$C = QC' \times \frac{1}{R_r \omega_r}$, $L = \frac{1}{QC'} \times \frac{R_r}{\omega_r}$
		$L = QL' \times \frac{R_r}{\omega_r}$, $C = \frac{1}{QC'} \times \frac{1}{R_r \omega_r}$

C' & L' are normilzed LP values

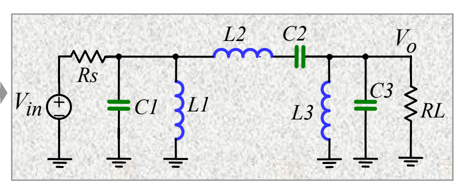
From:
Zverev,
Handbook of filter synthesis,
Wiley, 1967- p.157.

Lowpass to Bandpass Transformation Example: 3rd Order LPF → 6th Order BPF

Lowpass



Bandpass



- Each capacitor replaced by parallel L& C
- Each inductor replaced by series L&C

Lowpass to Bandpass Transformation
Example: 3rd Order LPF → 6th Order BPF

$$C_1 = QC_1' \times \frac{1}{R\omega_0}$$

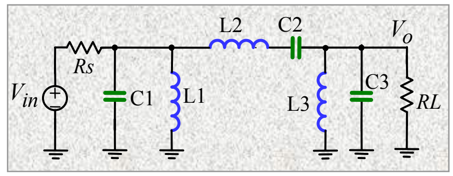
$$L_1 = \frac{1}{QC_1'} \times \frac{R}{\omega_0}$$

$$C_2 = \frac{1}{QL_2'} \times \frac{1}{R\omega_0}$$

$$L_2 = QL_2' \times \frac{R}{\omega_0}$$

$$C_3 = QC_3' \times \frac{1}{R\omega_0}$$

$$L_3 = \frac{1}{QC_3'} \times \frac{R}{\omega_0}$$



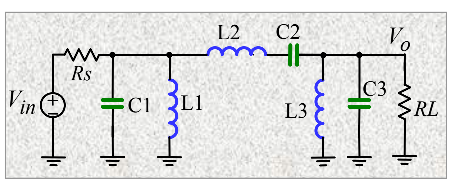
Where:

C_1' , L_2' , C_3' → Normalized lowpass values

Q → Bandpass filter quality factor

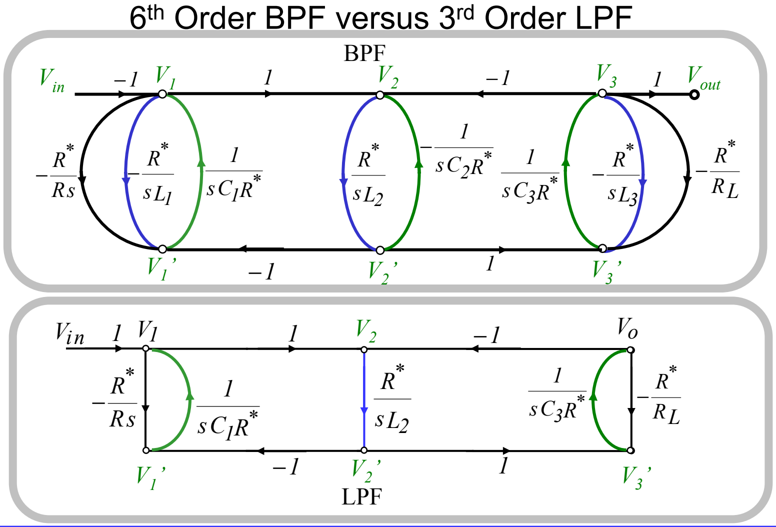
ω_0 → Filter center frequency

Lowpass to Bandpass Transformation
Signal Flowgraph

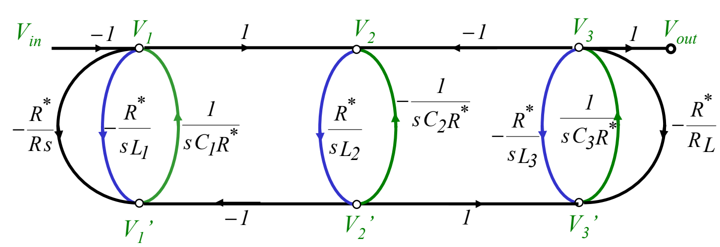


1- Voltages & currents named for all components
2- Use KCL & KVL to derive state space description
3- To have BMFs in the integrator form
   Cap. voltage expressed as function of its current $V_C=f(I_C)$
   Ind. current as a function of its voltage $I_L=f(V_L)$
4- Use state space description to draw SFG
5- Convert all current nodes to voltage

Signal Flowgraph
6^{th} Order BPF versus 3^{rd} Order LPF

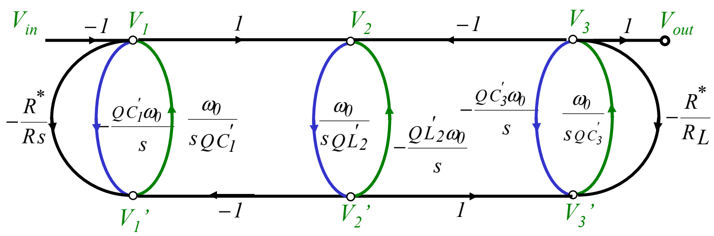


Signal Flowgraph
6^{th} Order Bandpass Filter



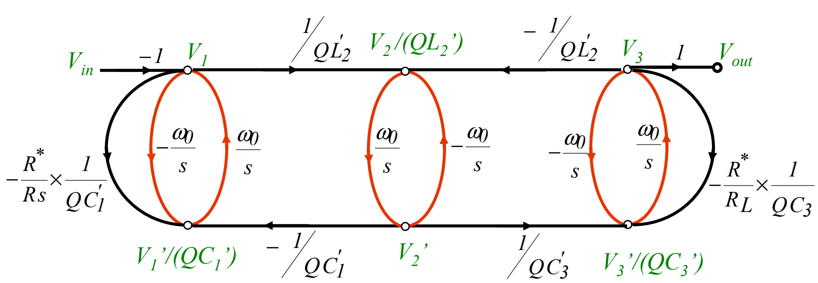
Note: each *C & L* in the original lowpass prototype → replaced by a *resonator*
Substituting the bandpass *L1, C1,.....* by their normalized lowpass equivalent from page 30
The resulting SFG is:

Signal Flowgraph
6^{th} Order Bandpass Filter



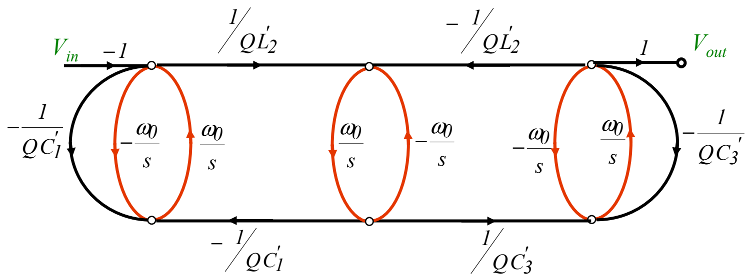
- Note the integrators → different time constants
  - Ratio of time constants for two integrator in each resonator ~ Q^2
    → Typically, requires high component ratios
    → Poor matching
- Desirable to modify SFG so that all integrators have equal time constants for optimum matching.
  - To obtain equal integrator time constant → use node scaling

Signal Flowgraph
6^{th} Order Bandpass Filter



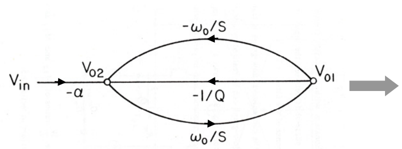
- All integrator time-constants → equal
- To simplify implementation → choose $RL=Rs=R^*$

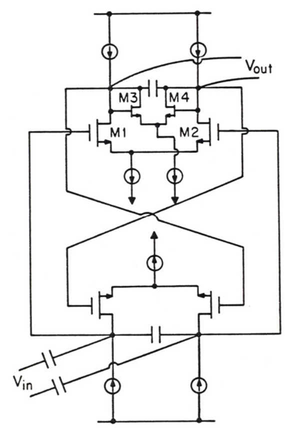
Signal Flowgraph
6^{th} Order Bandpass Filter



Let us try to build this bandpass filter using the simple Gm-C structure

Second Order Gm-C Filter
Using Simple Source-Couple Pair Gm-Cell





- Center frequency:

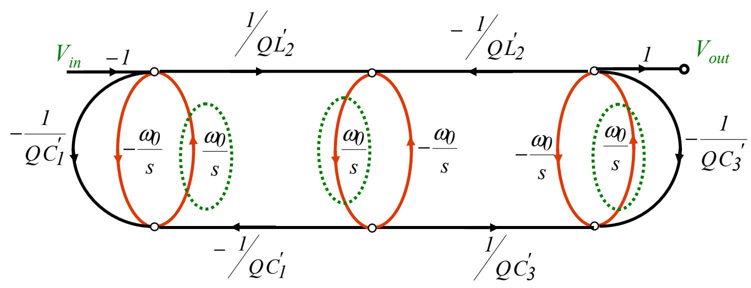
$$\omega_o = \frac{g_m^{M1,2}}{2 \times C_{intg}}$$

- Q function of:

$$Q = \frac{g_m^{M1,2}}{g_m^{M3,4}}$$

Use this structure for the 1st and the 3rd resonator
Use similar structure w/o M3, M4 for the 2nd resonator
How to couple the resonators?

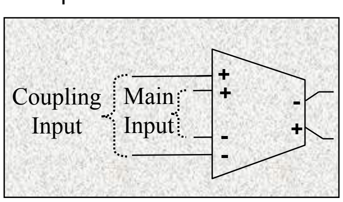
Coupling of the Resonators
1- Additional Set of Input Devices

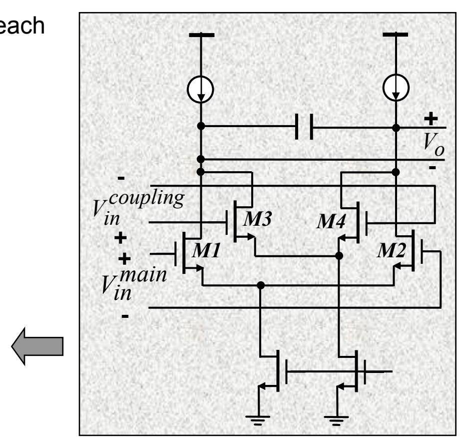


Coupling of resonators:
Use additional input source coupled pairs for the highlighted integrators
For example, the middle integrator requires 3 sets of inputs

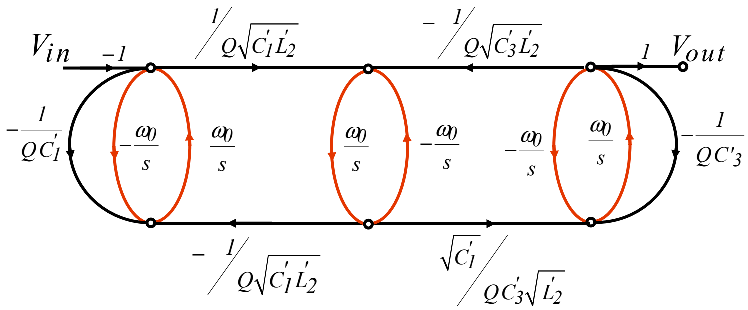
Example: Coupling of the Resonators
1- Additional Set of Input Devices

- Add one source couple pair for each additional input
- Coupling level → ratio of device widths
- Disadvantage → extra power dissipation





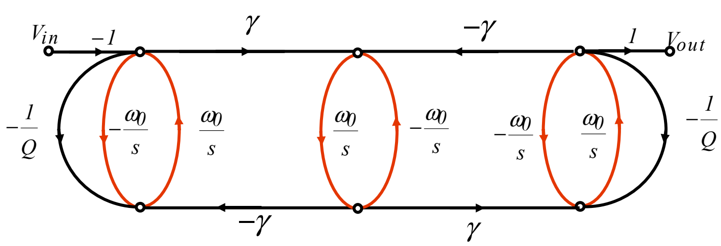
Coupling of the Resonators
2- Modify SFG → Bidirectional Coupling Paths



Modified signal flowgraph to have equal coupling between resonators

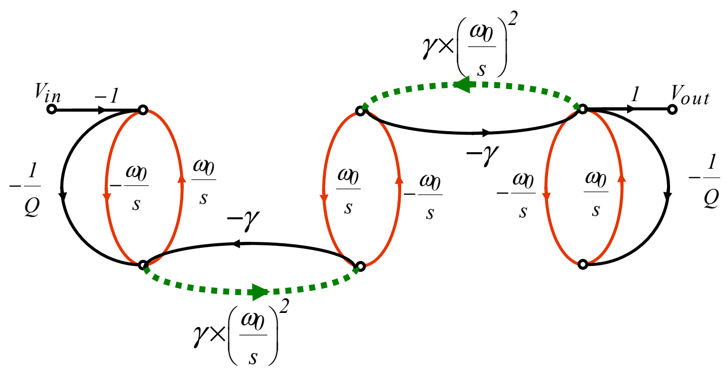
- In most filter cases $C_1' = C_3'$
- Example: For a butterworth lowpass filter $C_1' = C_3' = 1$ & $L_2' = 2$
- Assume desired overall bandpass filter $Q=10$

Sixth Order Bandpass Filter Signal Flowgraph



- Where for a Butterworth shape $\gamma = \frac{1}{Q\sqrt{2}}$
- Since in this example $Q=10$ then: $\gamma \approx \frac{1}{14}$

Sixth Order Bandpass Filter Signal Flowgraph
SFG Modification



Sixth Order Bandpass Filter Signal Flowgraph
SFG Modification

For narrow band filters (high Q) where frequencies within the passband are close to ω_0 *narrow-band approximation* can be used:

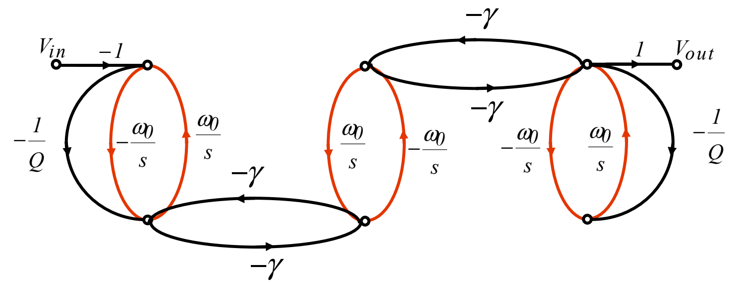
Within filter passband:

$$\left(\frac{\omega_0}{\omega}\right)^2 \approx 1$$

$$\gamma \times \left(\frac{\omega_0}{s}\right)^2 = \gamma \times \left(\frac{\omega_0}{j\omega}\right)^2 \approx -\gamma$$

The resulting SFG:

Sixth Order Bandpass Filter Signal Flowgraph
SFG Modification



Bidirectional coupling paths, can easily be implemented with coupling capacitors → no extra power dissipation

Sixth Order Gm-C Bandpass Filter
Utilizing Simple Source-Coupled Pair Gm-Cell

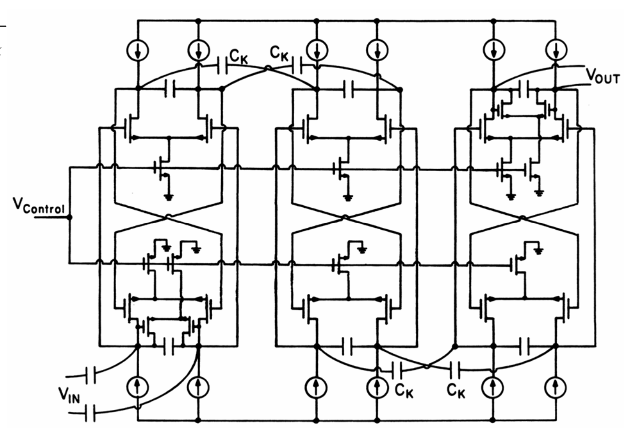
$$\gamma = \frac{C_k}{2\times C_{int\,g}+C_k}$$

$$C_k = \frac{2\times C_{int\,g}}{\frac{1}{\gamma}-1}$$

$$\gamma = 1/14$$

$$\rightarrow C_k = \frac{2}{13} C_{int\,g}$$

Parasitic cap. at integrator output, if unaccounted for, will result in inaccuracy in γ



Sixth Order Gm-C Bandpass Filter
Narrow-Band versus Exact
Frequency Response Simulation