EE247
Lecture 26

- Administrative
  - Project submission:
    - Project reports due Dec. 5th
    - Please make an appointment with the instructor for a 15minute meeting on Monday Dec. 8th
    - Prepare to give a 3 to 7 minute presentation regarding the project during the class period on Dec. 9th
      - Highlight the important aspects of your approach towards the implementation of the ADC
      - If the project is joint effort, one or both could present

EE247
Lecture 26

- Homework for oversampled data converters
  - Due to the time consuming nature of the project, homework covering oversampled converters will not be given. Please review relevant previous year homeworks & solutions e.g.
  - http://www-inst.eecs.berkeley.edu/~ee247/fa07/files07/homework/HW9_2_07.pdf
  - http://www-inst.eecs.berkeley.edu/~ee247/fa07/files07/homework/HW9_sol_Lynn_Wang.pdf

EE247
Lecture 26

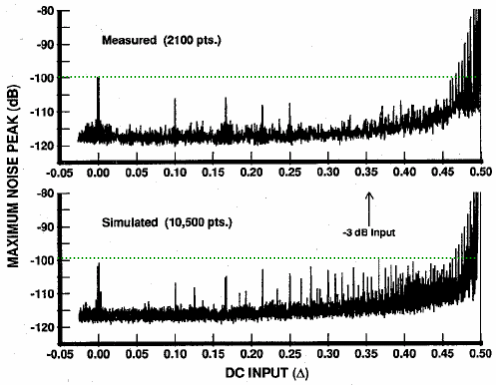
- Final course grading
  - Homeworks (7) 30%
  - Project 20%
  - Midterm exam 20%
  - Final exam 30%

EE247
Lecture 26

Oversampled ADCs (continued)

- 2^{nd} order $\Sigma\Delta$ modulator
  - Implementation example
- Higher order $\Sigma\Delta$ modulators
  - Cascaded modulators (multi-stage)
  - Single-loop single-quantizer modulators with multi-order filtering in the forward path
- Bandpass $\Sigma\Delta$ modulators
- Testing of $\Sigma\Delta$ modulator front-end

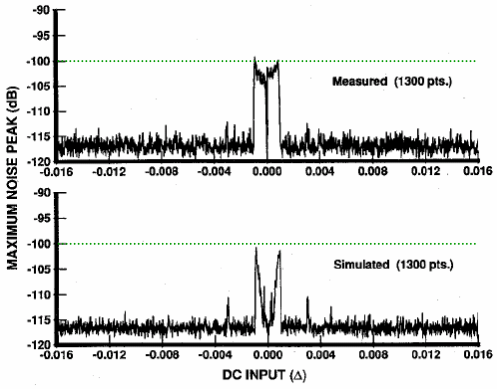
2nd Order ΣΔ
Implementation Example: Digital Audio Applications



→ Measured & simulated spurious tones performance as a function of DC input signal
→ Sampling rate=12.8MHz, M=256

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Digital Audio Applications



Sampling rate=12.8MHz, M=256

→ Measured & simulated noise tone performance for near zero DC worst case input → 0.00088Δ

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

Higher Order ΣΔ Modulator Dynamic Range

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)^{L} E(z) \quad , \quad L \rightarrow \Sigma\Delta \text{ order}$$

$$\overline{S_X} = \frac{1}{2}\left(\frac{\Delta}{2}\right)^2 \qquad \text{sinusoidal input,} \quad STF = 1$$

$$\overline{S_Q} = \frac{\pi^{2L}}{2L+1}\frac{1}{M^{2L+1}}\frac{\Delta^2}{12}$$

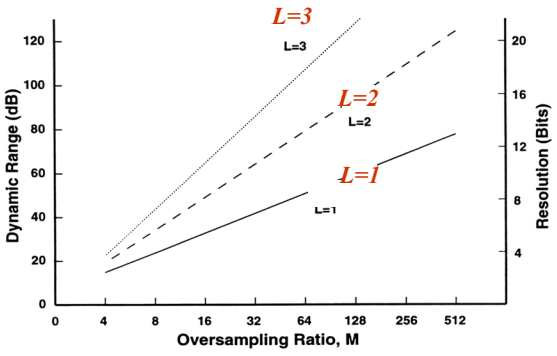
$$\frac{\overline{S_X}}{\overline{S_Q}} = \frac{3(2L+1)}{2\pi^{2L}} M^{2L+1}$$

$$DR = 10\log\left[\frac{3(2L+1)}{2\pi^{2L}} M^{2L+1}\right]$$

$$DR = 10\log\left[\frac{3(2L+1)}{2\pi^{2L}}\right] + (2L+1)\times 10\times \log M$$

2X increase in M→(*6L+3*)dB or (*L+0.5*)-bit increase in DR

ΣΔ Modulator Dynamic Range As a Function of Modulator Order



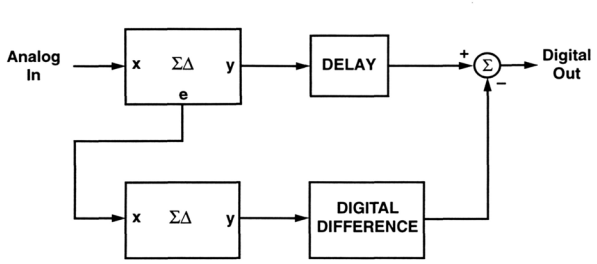
- Potential stability issues for L >2

Higher Order ΣΔ Modulators

- Extending ΣΔ Modulators to higher orders by adding integrators in the forward path (similar to 2nd order)
  → Issues with stability

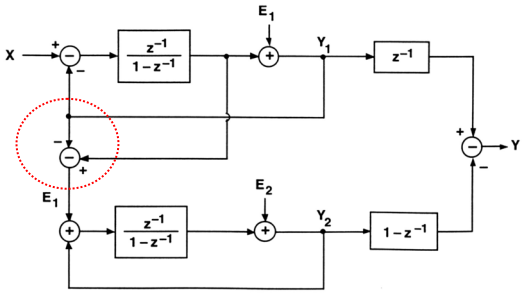
- Two different architectural approaches used to implement ΣΔ modulators of order >2
  1. Cascade of lower order modulators (multi-stage)
  2. Single-loop single-quantizer modulators with multi-order filtering in the forward path

Higher Order ΣΔ Modulators
(1) Cascade of 2-Stages ΣΔ Modulator



- Main ΣΔ quantizes the signal
- The 1st stage quantization error is then quantized by the 2nd quantizer
- The quantized error is then subtracted from the results in the digital domain

2nd Order (1-1) Cascaded ΣΔ Modulators



$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})E_1(z)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})Y_2(z)$$

$$= z^{-2}X(z) + z^{-1}(1 - z^{-1})E_1(z) - z^{-1}(1 - z^{-1})E_1(z) - (1 - z^{-1})^2E_2(z)$$

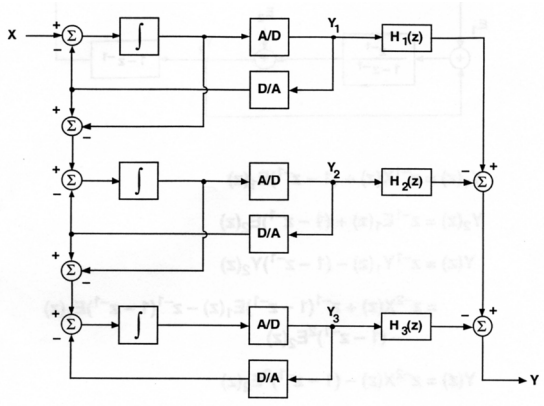
$$\boxed{Y(z) = z^{-2}X(z) - (1 - z^{-1})^2E_2(z)}$$

2nd order noise shaping

– **Cascade of two 1st order ΣΔs → 2nd order ΣΔ**

3rd Order Cascaded ΣΔ Modulators
(a) Cascade of 1-1-1 ΣΔs

- Can implement 3rd order noise shaping with 1-1-1
- This is also called MASH (multi-stage noise shaping)

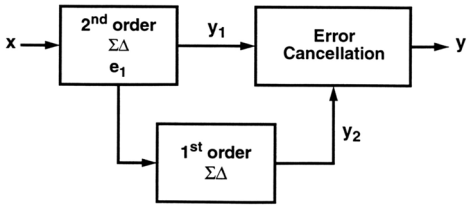


– **Cascade of two 1st order ΣΔs → 3rd order ΣΔ**

3rd Order Cascaded ΣΔ Modulators
(b) Cascade of 2-1 ΣΔs

Advantages of 2-1 cascade:

- Low sensitivity to precision matching of analog/digital paths
- Low spurious limit cycle tone levels
- No potential instability



$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_1(z)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

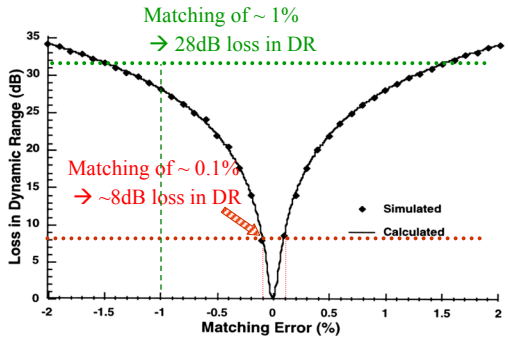
$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})^2 Y_2(z)$$

$$= z^{-3}X(z) + z^{-1}(1 - z^{-1})^2 E_1(z) - z^{-1}(1 - z^{-1})^2 E_1(z) - (1 - z^{-1})^3 E_2(z)$$

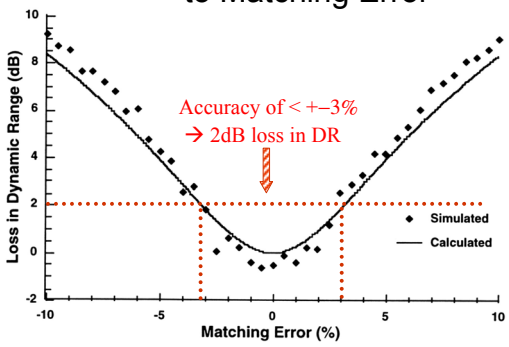
3rd order noise shaping ⇒

$$\boxed{Y(z) = z^{-3}X(z) - (1 - z^{-1})^3 E_2(z)}$$

Sensitivity of Cascade of (1-1-1) ΣΔ Modulators to Matching of Analog & Digital Paths



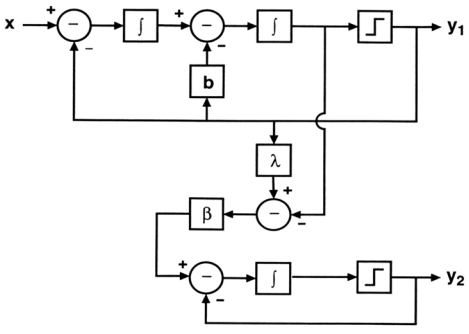
Sensitivity of Cascade of (2-1) ΣΔ Modulators to Matching Error



Main advantage of 2-1 cascade compared to 1-1-1 topology:

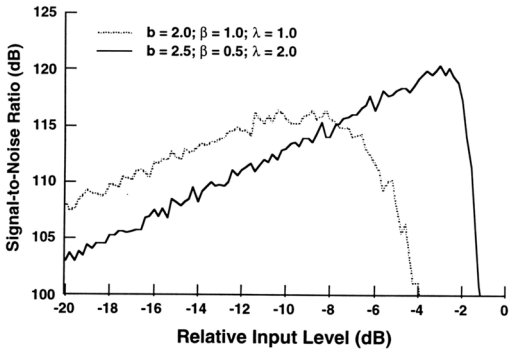
- Low sensitivity to matching of analog/digital paths (in excess of one order of magnitude less sensitive compared to (1-1-1)!)

2-1 Cascaded ΣΔ Modulators



Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits,* vol. 29, pp. 193 - 202, March 1994.

2-1 Cascaded ΣΔ Modulators

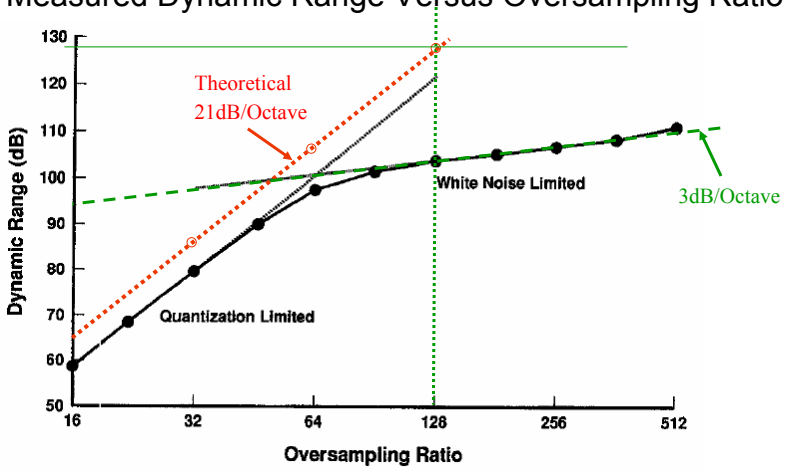


Effect of gain parameters on signal-to-noise ratio

Comparison of 2nd order & Cascaded (2-1) ΣΔ Modulator

Digital Audio Application, f_N =50kHz *(Does not include Decimator)*		
Reference	Brandt ,JSSC 4/91	Williams, JSSC 3/94
Architecture	*2nd order*	*(2+1) Order*
Dynamic Range	*98dB (16-bits)*	*104dB (17-bits)*
Peak SNDR	*94dB*	*98dB*
Oversampling rate	*256 (theoretical → SNR=109dB)*	*128 (theoretical → SNR=128dB)*
Differential input range	*4Vppd* *5V supply*	*8Vppd* *5V supply*
Power Dissipation	*13.8mW*	*47.2mW*
Active Area	*0.39mm²* (1μ tech.)	*5.2mm²* (1μ tech.)

2-1 Cascaded ΣΔ Modulators
Measured Dynamic Range Versus Oversampling Ratio

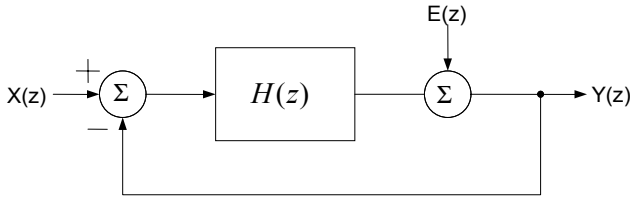


Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits,* vol. 29, pp. 193 - 202, March 1994.

Higher Order ΣΔ Modulators
(1) Cascaded Modulators Summary

- Cascade two or more stable ΣΔ stages
- Quantization error of each stage is quantized by the succeeding stage and subtracted digitally
- Order of noise shaping equals sum of the orders of the stages
- Quantization noise cancellation depends on the precision of analog/digital signal paths
- Quantization noise further randomized → less limit cycle oscillation problems
- Typically, no potential instability

Higher Order ΣΔ Modulators
(2) Multi-Order Filter



$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z)$$

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

- Zeros of NTF (poles of H(z)) can be strategically positioned to suppress in-band noise spectrum
- Approach: Design NTF first and solve for H(z)

Example: Modulator Specification

- Example: Audio ADC

– Dynamic range	DR	18 Bits
– Signal bandwidth	B	20 kHz
– Nyquist frequency	f_N	44.1 kHz
– Modulator order	L	5
– Oversampling ratio	$M = f_s/f_N$	64
– Sampling frequency	f_s	2.822 MHz

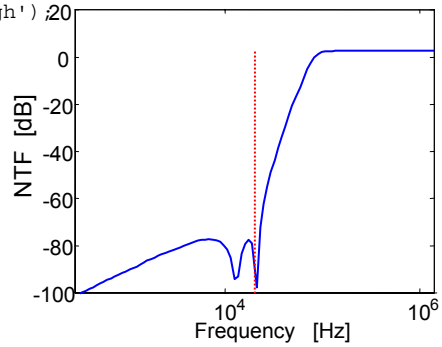
- The order L and oversampling ratio M are chosen based on
  - SQNR > 120dB

Noise Transfer Function, NTF(z)

```
% stop-band attenuation Rstop=80dB, L=5,
bandwidth-20kHz ...
L=5;
Rstop = 80;
B=20000;
[b,a] = cheby2(L, Rstop, B,'high');

NTF = filt(b, a, ...);
```

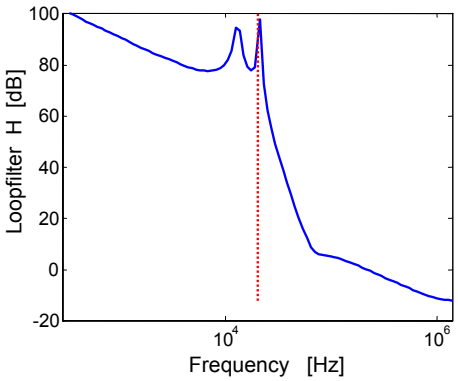
Chebychev II filter chosen
→ zeros in stop-band



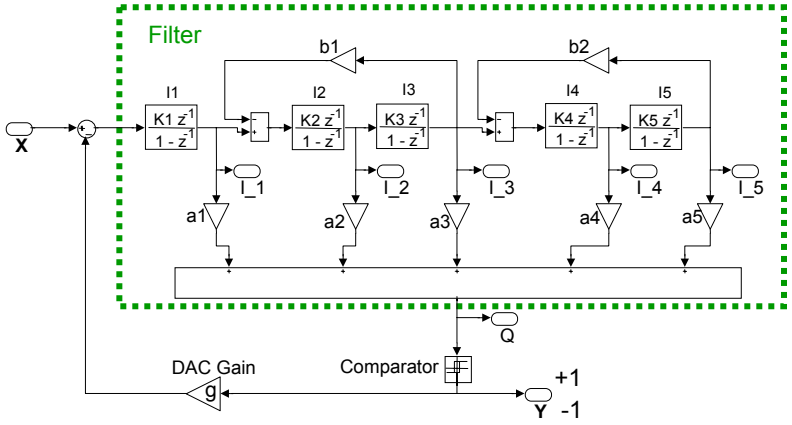
Loop-Filter Characteristics H(z)

$$\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

$$\rightarrow H(z) = \frac{1}{NFT} - 1$$



Modulator Topology
Simulation Model

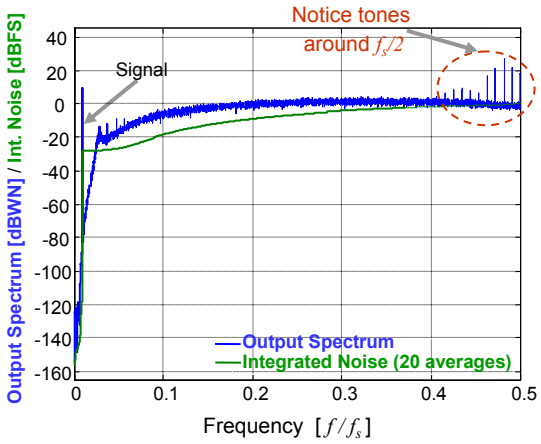


Filter Coefficients

```
a1=1;          k1=1;          b1=1/1024;
a2=1/2;        k2=1;          b2=1/16-1/64;
a3=1/4;        k3=1/2;
a4=1/8;        k4=1/4;
a5=1/8;        k5=1/8;        g =1;
```

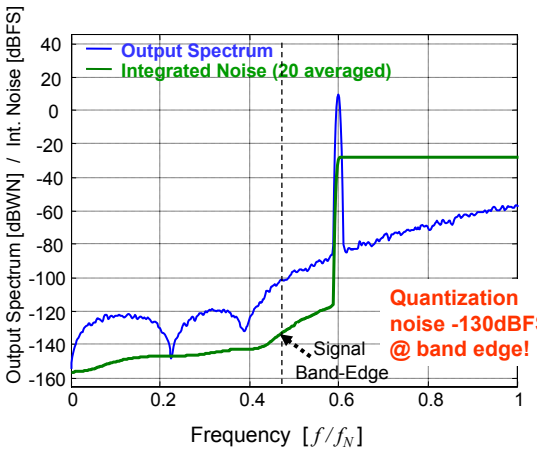
Ref: Nav Sooch, Don Kerth, Eric Swanson, and Tetsuro Sugimoto, “Phase Equalization System for a Digital-to-Analog Converter Using Separate Digital and Analog Sections”, U.S. Patent 5061925, 1990, figure 3 and table 1

5th Order Noise Shaping Simulation Results



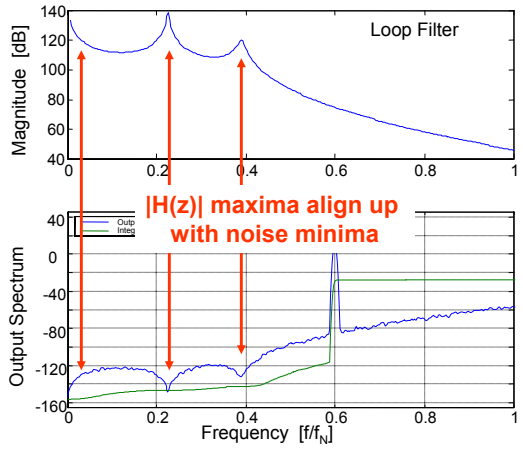
- Mostly quantization noise, except at low frequencies
- Let's zoom into the baseband portion…

5th Order Noise Shaping



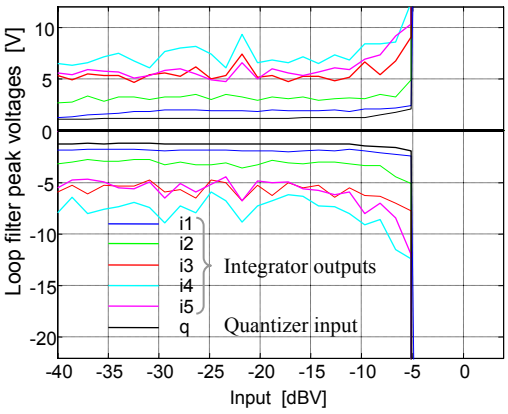
- SQNR > 120dB
- Sigma-delta modulators are usually designed for negligible quantization noise
- Other error sources dominate, e.g. thermal noise are allowed to dominate & thus provide dithering to eliminate limit cycle oscillations

In-Band Noise Shaping



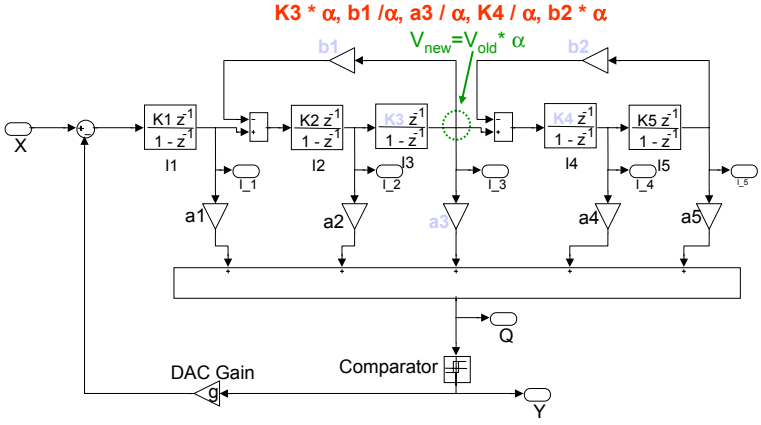
- Lot's of gain in the loop filter pass-band
- Forward path filter not necessarily stable!
- Remember that:
  - ✓NTF ~ 1/H→ small within passband since H is large
  - ✓STF=H/(1+H) → ~1 within passband

Internal Node Voltages

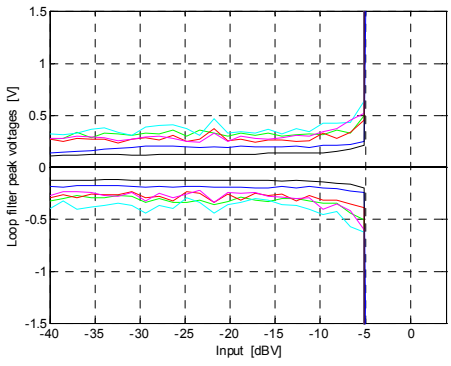


- Internal signal peak amplitudes are weak function of input level (except near overload)
- Maximum peak-to-peak voltage swing approach +-10V! Exceed supply voltage!
- Solutions:
  - Reduce V_{ref} ??
  - Node scaling

Node Scaling Example:
3rd Integrator Output Voltage Scaled by α



Node Voltage Scaling



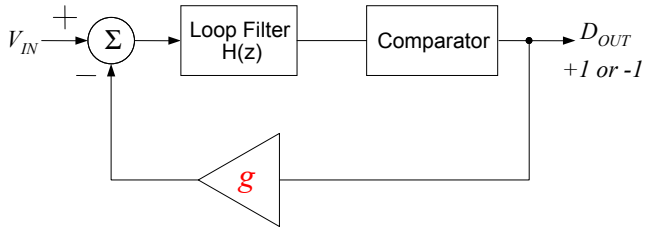
α=1/10
→
k1=1/10;
k2=1;
k3=1/4;
k4=1/4;
k5=1/8;
a1= 1;
a2=1/2;
a3=1/2;
a4=1/4;
a5=1/4;
b1=1/512;
b2=1/16-1/64;
g =1;

- Integrator output range reasonable for new parameters
- But: maximum input signal limited to -5dB (-7dB with safety) – fix?

Input Range Scaling

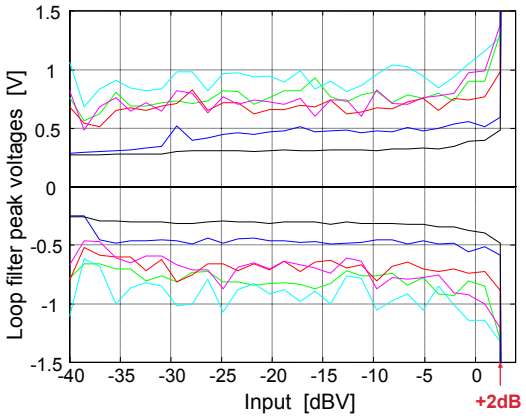
Increasing the DAC levels by using higher value for g reduces the analog to digital conversion gain:

$$\frac{D_{OUT}(z)}{V_{IN}(z)} = \frac{H(z)}{1+gH(z)} \cong \frac{1}{g}$$



Increasing V_{IN} & g by the same factor leaves 1-Bit data unchanged

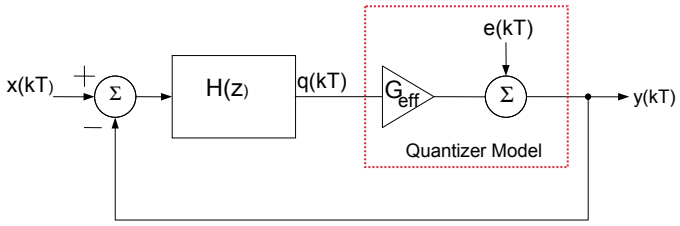
Scaled Stage 1 Model



g modified:
From 1 to 2.5;

→Overload input level shifted up by 8dB

Stability Analysis



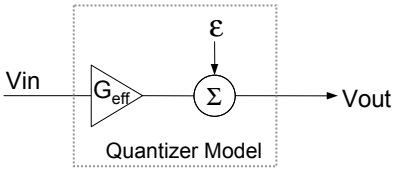
- Approach: linearize quantizer and use linear system theory!
- One way of performing stability analysis→ use RLocus in Matlab with H(z) as argument and Geff as variable
- Effective quantizer gain

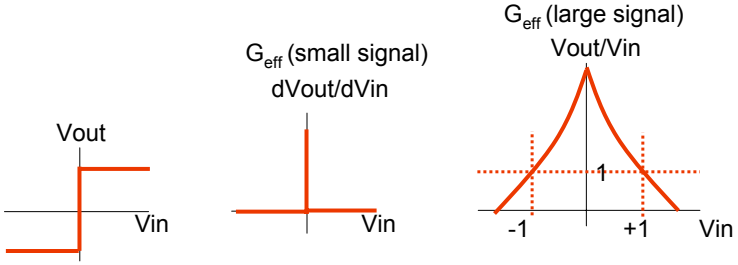
$$G_{eff}^2 = \overline{y^2} / \overline{q^2}$$

- Can obtain G_{eff} from simulation

Ref: R. W. Adams and R. Schreier, "Stability Theory for ΔΣ Modulators," in Delta-Sigma Data Converters- S. Norsworthy et al. (eds), IEEE Press, 1997

Quantizer Gain (G_{eff})





Stability Analysis

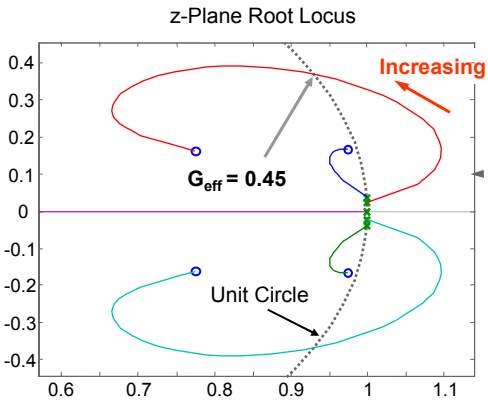
$$STF = \frac{G \cdot H(z)}{1 + G \cdot H(z)}$$

$$H(z) = \frac{N(z)}{D(z)}$$

$$\rightarrow STF = \frac{G \cdot N(z)}{D(z) + G \cdot N(z)}$$

- Zeros of STF same as zeros of H(z)
- Poles of STF vary with G
- For G=0 (no feedback) poles of the STF same as poles of H(z)
- For G=large, poles of STF move towards zeros of H(z)
- Draw root-locus: for G values for which poles move to LHP (s-plane) or inside unit circle (z-plane) → system is stable

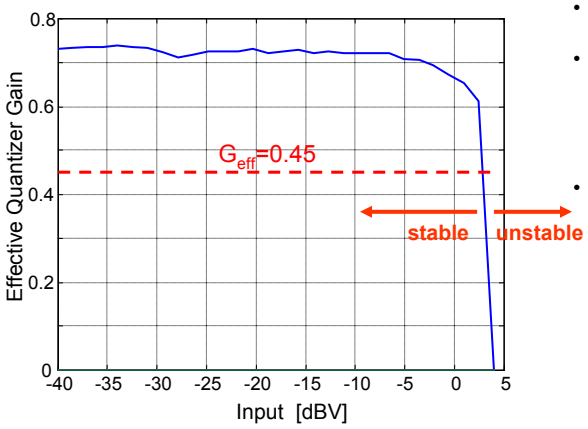
Modulator z-Plane Root-Locus



- As G_{eff} increases, poles of STF move from
  - poles of H(z) (G_{eff} = 0) to
  - zeros of H(z) (G_{eff} = ∞)
- Pole-locations inside unit-circle correspond to stable STF and NTF
- Need G_{eff} > 0.45 for stability

– Note: Final exam does NOT include Root Locus

Effective Quantizer Gain, Geff

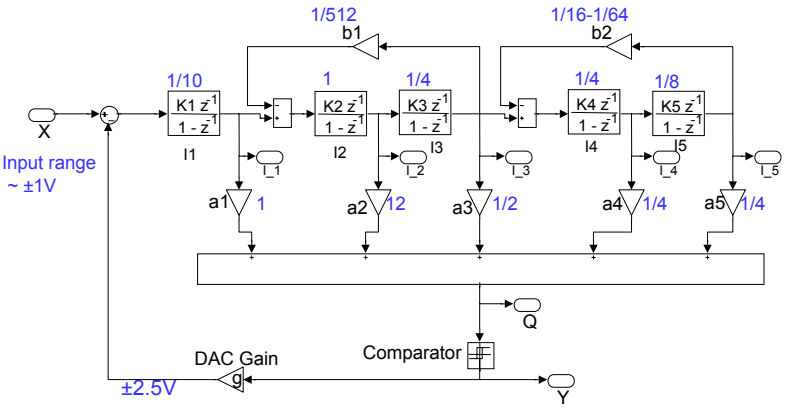


- Large inputs → comparator input grows
- Output is fixed (±1)
  → G_{eff} drops
  → modulator unstable for large inputs

- Solution:
  - Limit input amplitude
  - Detect instability (long sequence of +1 or -1) and reset integrators

  - Be ware that signals grow slowly for nearly stable systems → use long simulations

5th Order Modulator Final Parameter Values

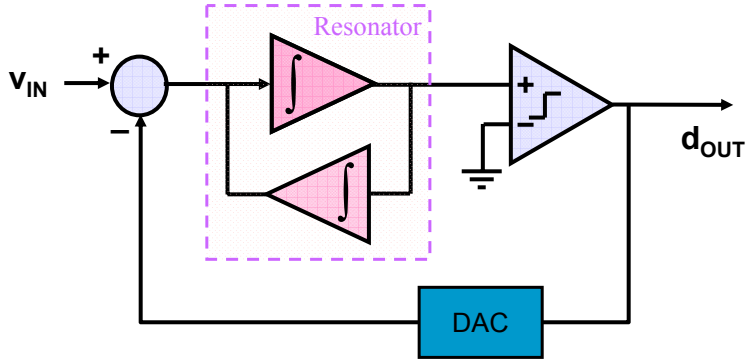


Stable input range with margin ~ ±1V

Summary

- Oversampled ADCs to 1st order, decouple SQNR from circuit complexity and accuracy
- If a 1-Bit DAC is used, the converter is to 1st order, inherently linear—independent of component matching
- Typically, used for high resolution & low frequency applications – e.g. digital audio
- 2nd order ΣΔ used extensively due to lower levels of limit cycle related spurious tones compared to 1st order
- ΣΔ modulators of order greater than 2:
  - Cascaded (multi-stage) modulators
  - Single-loop, single-quantizer modulators with multi-order filtering in the forward path

Bandpass ΔΣ Modulator



- Replace the integrator in 1st order lowpass ΣΔ with a resonator

  → 2nd order bandpass ΣΔ

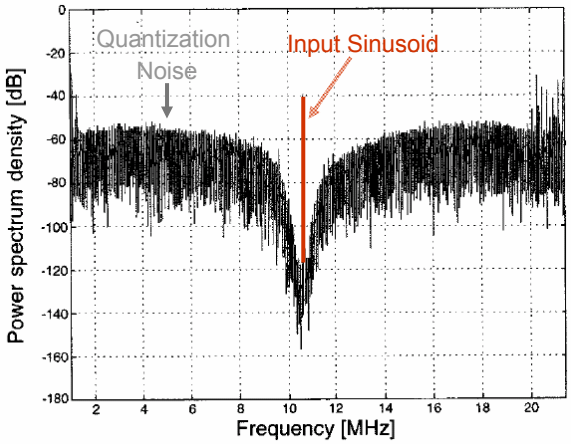
Bandpass ΔΣ Modulator Example: 6th Order

Measured output for a bandpass ΣΔ (prior to digital filtering)

Key Point:

NTF→ notch type shape

STF→ bandpass shape



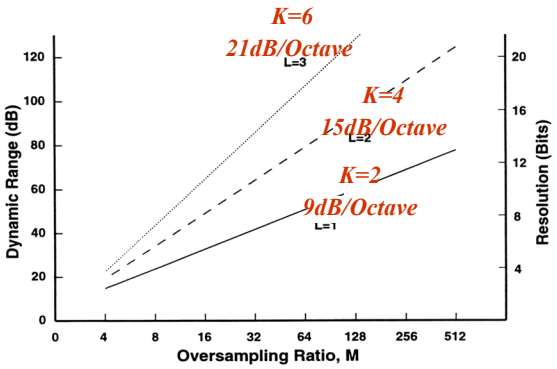
Ref:

Paolo Cusinato, et. al, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range ", IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001

Bandpass ΣΔ Characteristics

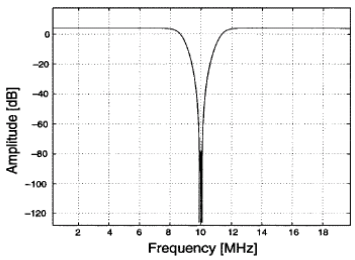
- Oversampling ratio defined as $f_s/2B$ where B = signal bandwidth
- Typically, sampling frequency is chosen to be $f_s=4xf_{center}$ where f_{center}→ bandpass filter center frequency
- STF has a bandpass shape while NTF has a notch shape
- To achieve same resolution as lowpass, need twice as many integrators

Bandpass ΣΔ Modulator Dynamic Range As a Function of Modulator Order (K)

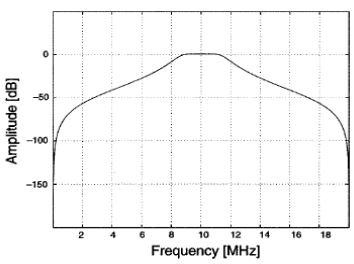


- Bandpass ΣΔ resolution for order K is the same as lowpass ΣΔ resolution with order L= K/2

Example: Sixth-Order Bandpass ΣΔ Modulator



Simulated noise transfer function



Simulated signal transfer function

Ref:

Paolo Cusinato, et. al, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range ", IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001

Example: Sixth-Order Bandpass ΣΔ Modulator

Features & Measured Performance

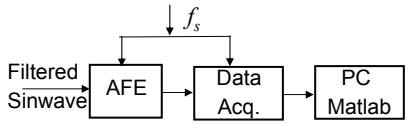
Analog input full-scale	4.4V (differential)
Sampling frequency (F_S)	42.8MHz ← $f_s=4xf_{center}$
Center frequency (f_0)	10.7MHz
Signal bandwidth	200kHz ← B
OSR	107 ← $OSR=f_s/2B$
Dynamic range	74dB (200kHz band)
	88dB (9kHz band)
Peak SNDR	61dB
IMD (@-15dB)	71dBc
Active die area	$1mm^2$
Power supply	3.3V
Power consumption	76mW (adaptive biasing)
	126mW (standard biasing)
Technology	0.35µm CMOS

Ref:

Paolo Cusinato, et. al, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range ", IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001

Modulator Front-End Testing

- Should make provisions for testing the modulator (AFE) separate from the decimator (digital back-end)
- Data acquisition board used to collect 1-bit digital output at f_s rate
- Analyze data in a PC environment or dedicated test equipment in manufacturing environments can be used
- Need to run DFT on the collected data and also make provisions to perform the function of digital decimation filter in software
- Typically, at this stage, parts of the design phase behavioral modeling effort can be utilized
- Good testing strategy vital for debugging/improving challenging designs



Summary
Oversampled ADCs

- Noise shaping utilized to reduce baseband quantization noise power
- Reduced precision requirement for analog building blocks compared to Nyquist rate converters
- Relaxed transition band requirements for analog anti-aliasing filters due to oversampling
- Takes advantage of low cost, low power digital filtering
- Speed is traded for resolution
- Typically used for lower frequency applications compared to Nyquist rate ADCs