EE247
Lecture 25

- Administrative
  - EE247 Final exam:
    - Date: Sat. Dec.13th
    - Time: 5 to 8pm
    - Location: 203 MCL (same as class)
    - Closed course notes/books
    - No calculators/cell phones/PDAs/computers
    - Bring two 8x11 paper with your own notes
    - Final exam covers the entire course material unless specified otherwise

---

EE247
Lecture 25

Oversampled ADCs (continued)
- 2nd order $\Sigma\Delta$ modulator
  - Practical implementation
    - Effect of various building block nonidealities on the $\Sigma\Delta$ performance
      - Integrator maximum signal handling capability
      - Integrator finite DC gain
      - Comparator hysteresis
      - Integrator non-linearity
      - Effect of KT/C noise
      - Finite opamp bandwidth
      - Opamp slew limited settling
    - Implementation example
- Higher order $\Sigma\Delta$ modulators
  - Cascaded modulators (multi-stage)
  - Single-loop single-quantizer modulators with multi-order filtering in the forward path

2nd Order ΣΔ Modulator Example

- Digital audio application
  - Signal bandwidth *20kHz*
  - Desired resolution *16-bit*

$$16-bit \rightarrow 98\,dB \quad \text{Dynamic Range}$$

$$DR_{2nd\,order\,\Sigma\Delta} = -11.1dB + 50\log M$$

$$M_{min} = 153$$

M → 256=2^8 *(→ DR=109dB)* two reasons:
  1. Allow some margin so that thermal noise dominate & provides dithering to minimize level of in-band limit cycle oscillation
  2. Choice of *M* power of *2* → ease of digital filter implementation

→ Sampling rate *(2x20kHz + 5kHz)M = 12MHz* (quite reasonable!)

Limit Cycle Tones in 1st Order & 2nd Order ΣΔ Modulator

- Higher oversampling ratio → lower tones

- 2nd order tones much lower compared to 1st

- 2X increase in M decreases the tones by 6dB for 1st order loop and 12dB for 2nd order loop
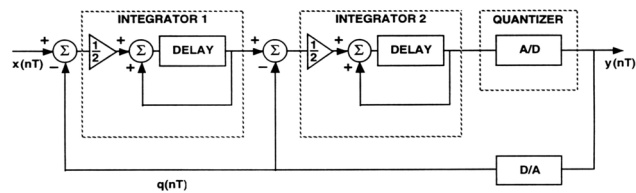

Ref: B. P. Brandt, et al., "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.
    R. Gray, "Spectral analysis of quantization noise in a single-loop sigma–delta modulator with dc input," *IEEE Trans. Commun.,* vol. 37, pp. 588–599, June 1989.

$\Sigma\Delta$ Implementation
Practical Design Considerations

• Internal node scaling & clipping

• Effect of finite opamp gain & linearity

• KT/C noise

• Opamp noise

• Effect of comparator nonidealities
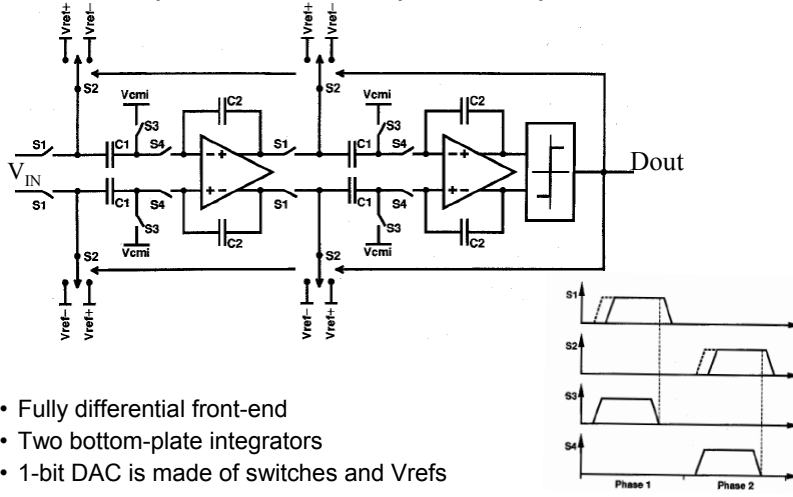
• Power dissipation considerations

Switched-Capacitor Implementation 2nd Order $\Sigma\Delta$
Nodes Scaled for Maximum Dynamic Range

• Modification (gain of ½ in front of integrators) reduce & optimize required signal range at the integrator outputs ~ 1.7x input full-scale (Δ)
• Note: Non-idealities associated with 2nd integrator and quantizer when referred to the $\Sigma\Delta$ input is attenuated by 1st integrator high gain
  → The only building block requiring low-noise and high accuracy is the 1st integrator
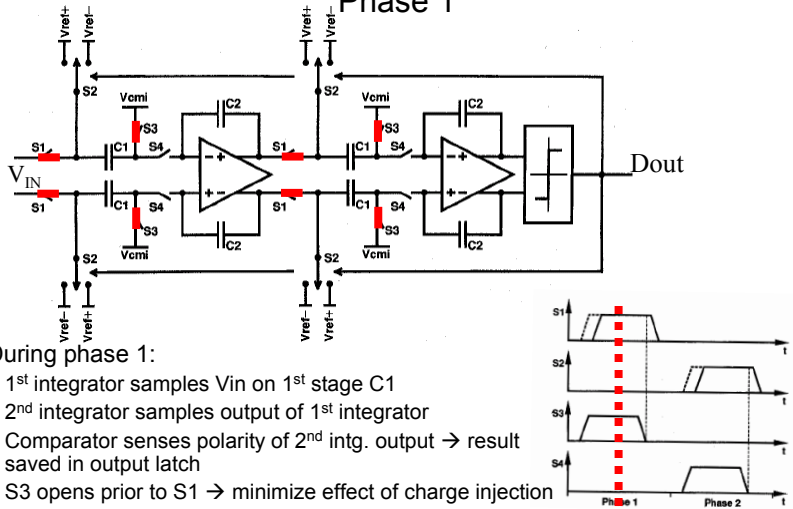
Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ Modulator
Example: Switched-Capacitor Implementation

- Fully differential front-end
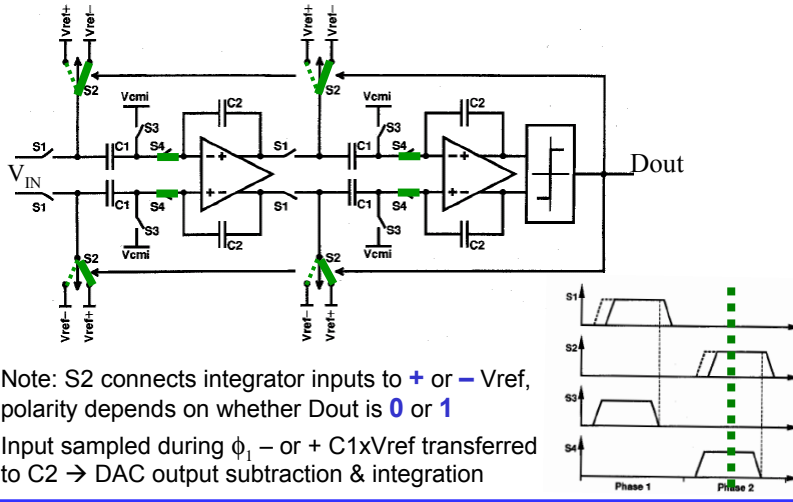- Two bottom-plate integrators
- 1-bit DAC is made of switches and Vrefs

Switched-Capacitor Implementation 2nd Order ΣΔ
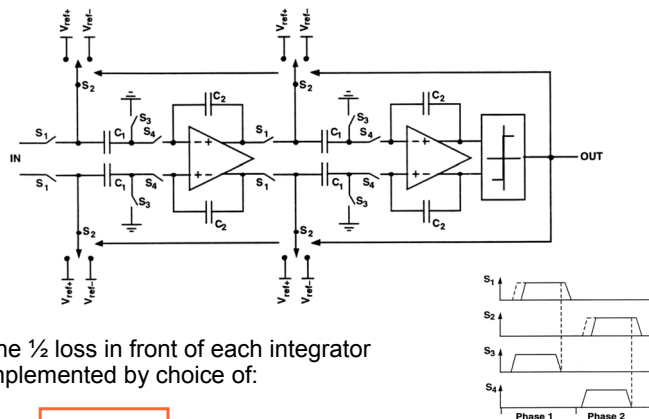## Phase 1

During phase 1:
- 1st integrator samples Vin on 1st stage C1
- 2nd integrator samples output of 1st integrator
- Comparator senses polarity of 2nd intg. output → result saved in output latch
- S3 opens prior to S1 → minimize effect of charge injection

Switched-Capacitor Implementation 2nd Order ΣΔ Phase 2

- Note: S2 connects integrator inputs to **+** or **−** Vref, polarity depends on whether Dout is **0** or **1**
- Input sampled during ϕ_1 – or + C1xVref transferred to C2 → DAC output subtraction & integration

2nd Order ΣΔ Modulator Switched-Capacitor Implementation

- The ½ loss in front of each integrator implemented by choice of:

$$C_2=2C_1 \qquad \rightarrow f_0^{intg}=f_s/(4\pi)$$
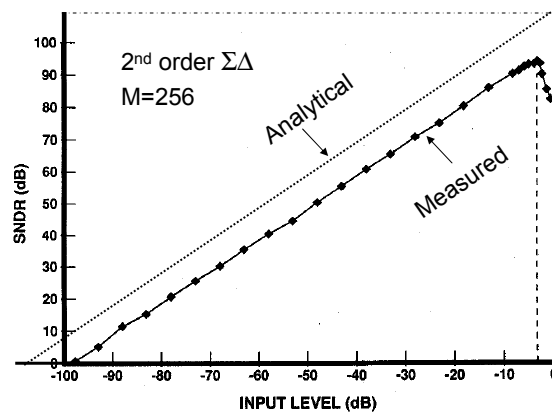
Design Phase Simulations

- Design of oversampled ADCs requires simulation of extremely long data traces due to the oversampled nature of the system
- SPICE type simulators:
  - Normally used to test for gross circuit errors only
  - Too slow for detailed performance verification
- Typically, behavioral modeling is used in MATLAB-like environments
- Circuit non-idealities either computed or found by using SPICE at subcircuit level
- Non-idealities introduced in the behavioral model one-by-one first to fully understand the effect of each individually
- Next step is to add as many of the non-idealities simultaneously as possible to verify whether there are interaction among non-idealities

Example: Testing $\Sigma\Delta$ ADC

Note:

The Nyquist ADC tests such as INL and DNL test do not apply to $\Sigma\Delta$ modulator type ADCS
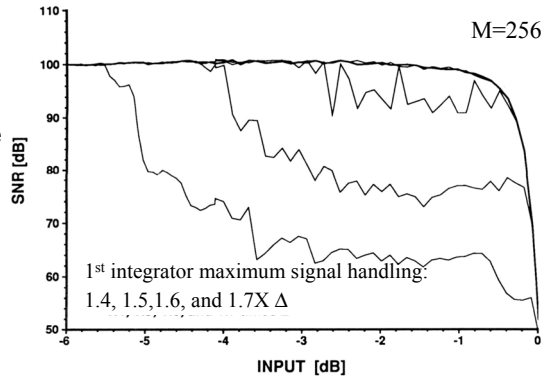
$\Sigma\Delta$ testing is performed via SNDR as a function of input signal level

2nd Order ΣΔ

Effect of 1st Integrator Maximum Signal Handling Capability on SNR

M=256

– Behavioral model
– Non-idealities tested one by one

1st integrator maximum signal handling:
1.4, 1.5,1.6, and 1.7X Δ

SNR [dB] (vertical axis, 50–110)
INPUT [dB] (horizontal axis, -6 to 0)
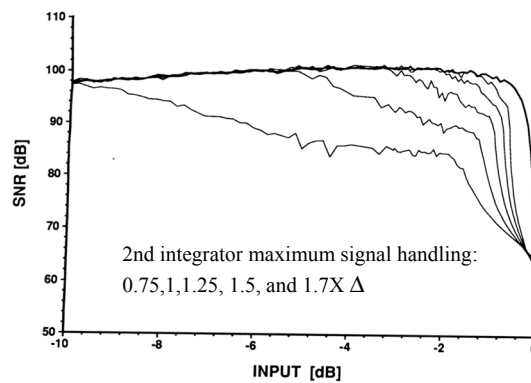
• Effect of 1st Integrator maximum signal handling capability on converter SNR
→ No SNR loss for max. sig. handling >1.7Δ

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.
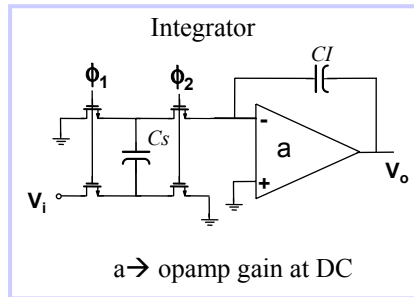

2nd Order ΣΔ

Effect of 2nd Integrator Maximum Signal Handling Capability on SNR

2nd integrator maximum signal handling:
0.75,1,1.25, 1.5, and 1.7X Δ

SNR [dB] (vertical axis, 50–110)
INPUT [dB] (horizontal axis, -10 to 0)

• Effect of 2nd Integrator maximum signal handling capability on SNR
→ No SNR loss for max. sig. handling >1.7 Δ

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2nd Order ΣΔ
Effect of Integrator Finite DC Gain
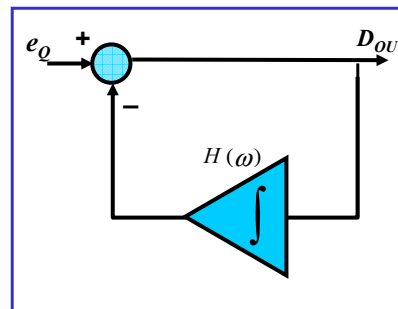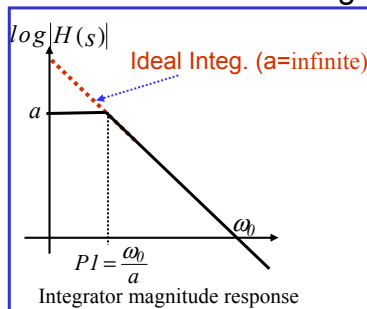
Integrator

$a \rightarrow$ opamp gain at DC

$$H(z)_{ideal} = \frac{Cs}{CI} \times \frac{z^{-1}}{1 - z^{-1}}$$

$$H(z)_{Finit\,DC\,Gain} = \frac{Cs}{CI} \times \frac{\left(\dfrac{a}{1+a+\dfrac{Cs}{CI}}\right) z^{-1}}{1 - \left(\dfrac{1+a}{1+a+\dfrac{Cs}{CI}}\right) z^{-1}}$$

$$\rightarrow H(DC) = a$$

2nd Order ΣΔ
Effect of Integrator Finite DC Gain

Ideal Integ. (a=infinite)

$log|H(s)|$

a

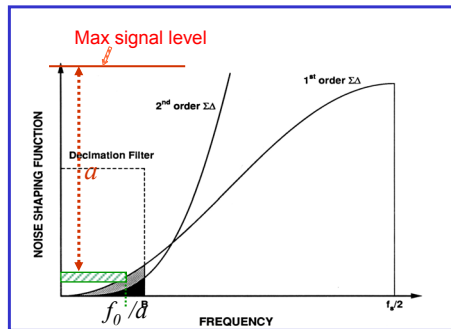$P1 = \dfrac{\omega_0}{a}$

ω_0

Integrator magnitude response

• Note: Quantization transfer function wrt output has integrator in the feedback path:

$$\frac{Dout}{e_Q} = \frac{1}{1 + H(\omega)}$$

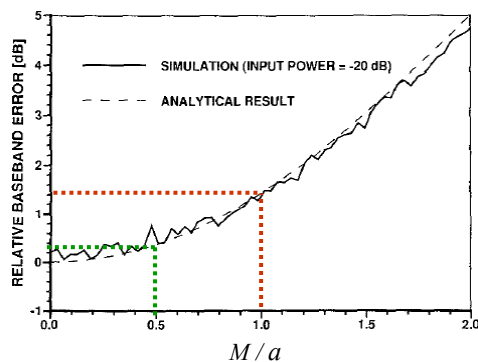$$\rightarrow @\ DC\ for\ ideal\ integ: \frac{Dout}{e_Q} = 0$$

$$\rightarrow @\ DC\ for\ real\ integ: \frac{Dout}{e_Q} \approx \frac{1}{a}$$

1st & 2nd Order ΣΔ
Effect of Integrator Finite DC Gain

- Low integrator DC gain → Increase in total in-band quantization noise
- Can be shown: If $a > M$ (oversampling ratio) → Insignificant degradation in SNR
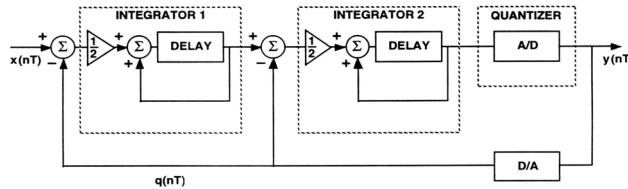- Normally DC gain designed to be >> M in order to suppress nonlinearities

---

2nd Order ΣΔ
Effect of Integrator Finite DC Gain

- *Example:* $a = 2M$ → 0.4dB degradation in SNR
  $a = M$ → 1.4dB degradation in SNR

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.
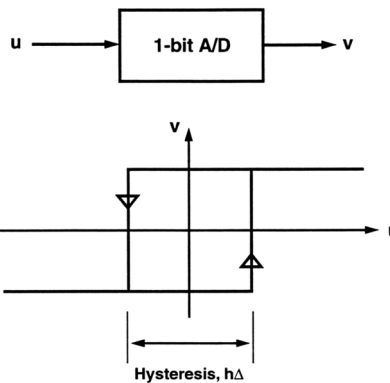
2nd Order $\Sigma\Delta$
Effect of Comparator Non-Idealities on $\Sigma\Delta$ Performance

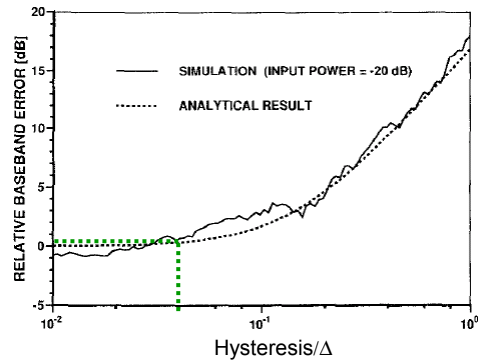1-bit A/D $\rightarrow$ Single comparator
- Speed must be adequate for the operating sampling rate
- Input referred offset- feedback loop & high DC intg. gain suppresses the effect
    - $\rightarrow$ $\Sigma\Delta$ performance quite insensitive to comparator offset
- Input referred comparator noise- same as offset
- Hysteresis= Minimum overdrive required to change the output

2nd Order $\Sigma\Delta$
Comparator Hysteresis

Hysteresis= Minimum overdrive required to change the output

2nd Order ΣΔ
Comparator Hysteresis
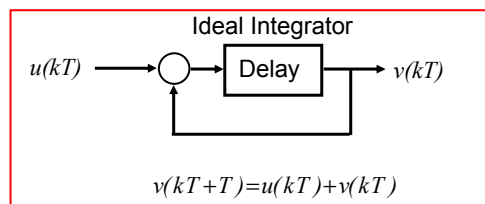

→ Comparator hysteresis < Δ/25 does not affect SNR
→ E.g. Δ=1V, comparator hysteresis up to 40mV tolerable
Key Point: One of the main advantages of ΣΔ ADCS → Highly tolerant of comparator and in general building-block non-idealities

---

2nd Order ΣΔ
Effect of Integrator Nonlinearities

Ideal Integrator

$u(kT) \longrightarrow \bigcirc \longrightarrow \boxed{\text{Delay}} \longrightarrow v(kT)$

$$v(kT+T)=u(kT)+v(kT)$$

With non-linearity added:

$$v(kT+T)= u(kT)+\alpha_2\left[u(kT)\right]^2+\alpha_3\left[u(kT)\right]^3\ldots..$$
$$+v(kT)+\beta_2\left[v(kT)\right]^2+\beta_3\left[v(kT)\right]^3+\ldots.$$

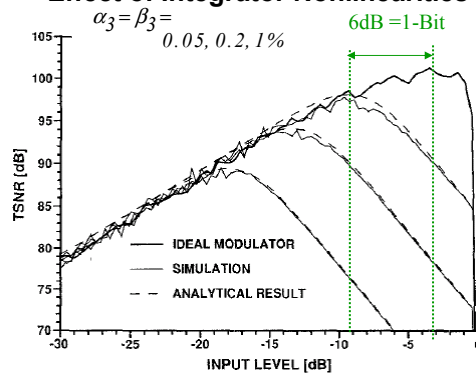Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2ⁿᵈ Order ΣΔ
Effect of Integrator Nonlinearities (Single-Ended)

$\alpha_2 = \beta_2 = 0.01, 0.02, 0.05, 0.1\%$

- Simulation for single-ended topology
- Even order nonlinearities can be significantly attenuated by using differential circuit topologies

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2ⁿᵈ Order ΣΔ
Effect of Integrator Nonlinearities

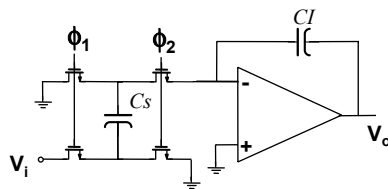$\alpha_3 = \beta_3 = 0.05, 0.2, 1\%$

6dB = 1-Bit

- Simulation for single-ended topology
- Odd order nonlinearities (3ʳᵈ in this case)

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2nd Order $\Sigma\Delta$
Effect of Integrator Nonlinearities

- Odd order nonlinearities (usually 3rd) could case significant loss of SNR for high resolution oversampled ADCs
- Two significant source of non-linearities:
  - Non-linearities associated with opamp used to build integrators
    - Opamp open-loop non-linearities are suppressed by the loopgain since there is feedback around the opamp
      - Class A opamps tend to have lower open loop gain but more linear output versus input transfer characteristic
      - Class A/B opamps typically have higher open loop gain but non-linear transfer function. At times this type is preferred for $\Sigma\Delta$ AFE due to its superior slew rate compared to class A type
  - Integrator capacitor non-linearites
    - Poly-Sio2-Poly capacitors$\rightarrow$non-linearity in the order of 10ppm/V
    - Metal-Sio2-Metal capacitors ~ 1ppm/V

2nd Order $\Sigma\Delta$
Effect of Integrator KT/C noise

$$\overline{v_n^2} = \frac{2KT}{Cs}$$

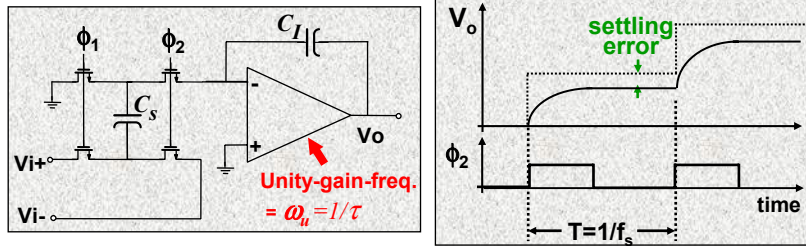$$\overline{v_n^2}/f = 2\frac{kT}{Cs} \times \frac{1}{fs/2} = 4\frac{kT}{Cs \times fs}$$

Total in-band noise:

$$\overline{v_n^2}_{input-referred} = 4\frac{kT}{Cs \times fs} \times f_B$$

$$= \frac{2kT}{Cs \times M}$$

- For the example of digital audio with *16-bit (96dB)* & *M=256* (*110dB SQNR*)
  - $\rightarrow$ *Cs=1pF* $\rightarrow$ *7µVrms* noise
  - $\rightarrow$ If *$V_{FS}=2V_{p-p-d}$* then thermal noise @ *-101dB* $\rightarrow$ degrades overall *SNR* by *~10dB*
  - $\rightarrow$ *Cs=1pF, CI=2pF* $\rightarrow$**much smaller capacitor area (~*1/M*) compared to Nyquist ADC**
  - $\rightarrow$Since thermal noise provides some level of dithering $\rightarrow$ better not choose much larger capacitors!
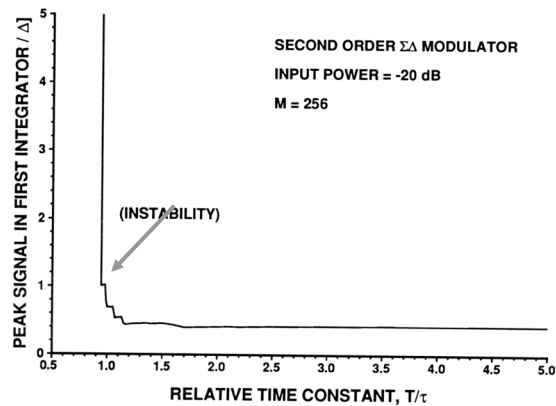
2nd Order ΣΔ
Effect of Finite Opamp Bandwidth

Assumptions:
  Opamp → does not slew
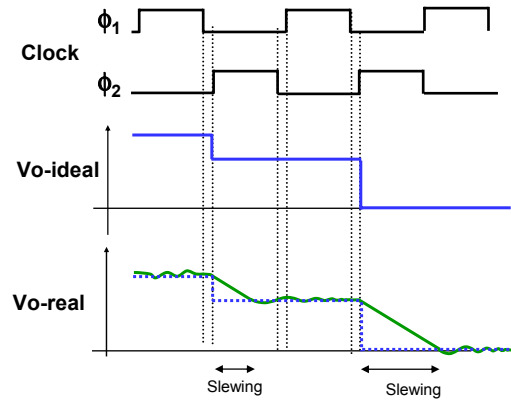 Opamp has only one pole → exponential settling

2nd Order ΣΔ
Effect of Finite Opamp Bandwidth

SECOND ORDER ΣΔ MODULATOR
INPUT POWER = -20 dB
M = 256

(INSTABILITY)

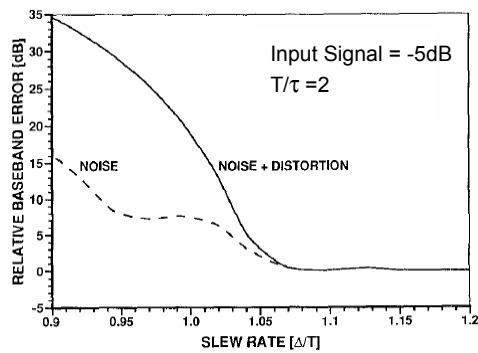→ ΣΔ does not require high opamp bandwidth $T/\tau > 2$ or $f_u > 2f_s$ adequate
Note: Bandwidth requirements significantly more relaxed compared to Nyquist rate ADCs
Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2nd Order ΣΔ
Effect of Slew Limited Settling

Clock — ϕ_1, ϕ_2

Vo-ideal

Vo-real

Slewing   Slewing

2nd Order ΣΔ
Effect of Slew Limited Settling
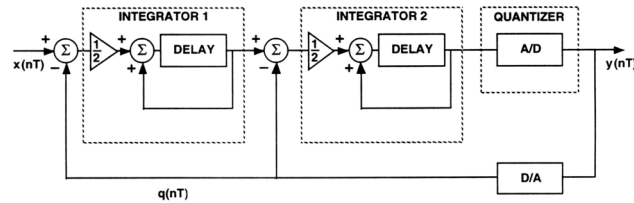

Input Signal = -5dB
$T/\tau = 2$

NOISE   NOISE + DISTORTION

Assumption:

Opamp settling → includes a single-pole setting of $\tau = 1/2f_s$ + slewing

→ Low slew rate degrades SNR rapidly- increases quantization noise and also causes signal distortion

→ Minimum slew rate of $S_R^{min} \sim 1.2 \ (\Delta \times f_s)$ required

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2nd Order $\Sigma\Delta$
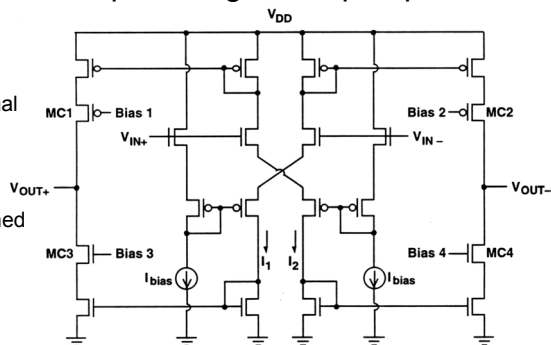## Implementation Example: Digital Audio Application

- In Ref.: 5V supply, $\Delta = 4$Vp-p-d, f_s=12.8MHz$\rightarrow$ M=256 $\rightarrow$ theoretical quantization noise @-110dB
- Minimum capacitor values computed based on -104dB noise wrt maximum signal
  - $\rightarrow$ Max. inband KT/C noise = $7\mu Vrms$ (thermal noise dominates $\rightarrow$ provide dithering & reduce limit cycle oscillations)
  - $\rightarrow$ $C1=(2kT)/(M\,v_n^2)=1pF$ $C2=2C1$

  Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order $\Sigma\Delta$
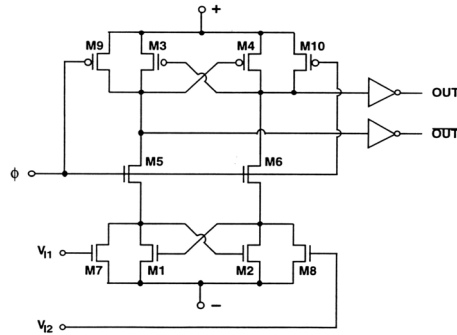## Implementation Example: Integrator Opamp

- Class A/B type opamp $\rightarrow$ High slew-rate
- S.C. common-mode feedback
- Input referred noise (both thermal and 1/f) important for high resolution performance
- Minimum required DC gain> M=256 , usually DC gain designed to be much higher to suppress nonlinearities (particularly, for class A/B amps)
- Minimum required slew rate of 1.2($\Delta.f_s$) $\rightarrow$ 65V/usec
- Minimum opamp settling time constant $\rightarrow$ 1/2fs~30nsec

  Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Comparator

- Comparator → simple design

- Minimum acceptable hysteresis or offset (based on analysis) → $\Delta/25 \sim 160mV$

→ Since offset requirement not stringent → No preamp needed, basically a latch with reset

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Subcircuit Performance

Subcircuit Performance		Our computed minimum required	Over-Design Factor
Operational Amplifier			
DC gain	67 dB	DC Gain 48dB (compensates non-linear open-loop gain)	x8
Unity-gain frequency	50 MHz	Unity-gain freq =2fs=25MHz	x2
Slew rate	350 V/μsec	Slew rate = 65V/usec	x5
Linear output range	6 V	Output range 1.7Δ=6.8V!	X0.9
Sampling rate	12.8 MHz		
Integrator			
Settling time constant	7.25 nsec	Settling time constant= 30nsec	x4
Comparator			
Offset	13 mV	Comparator offset 160mV	x12

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
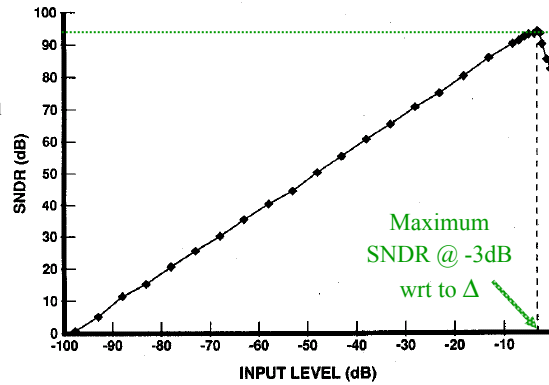### Implementation Example: Digital Audio Applications

Measured SNDR

M=256, 0dB=4V$_{p-p-d}$

f$_{sampling}$: 12.8MHz

Test signal frequency: 2.8kHz

Maximum SNDR @ -3dB wrt to Δ

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
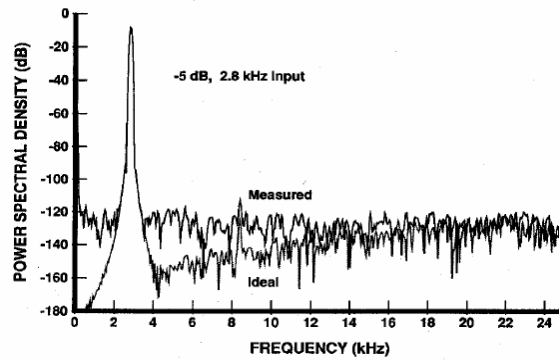### Implementation Example: Digital Audio Applications

Measured Performance Summary
(Does Not Include Decimator)

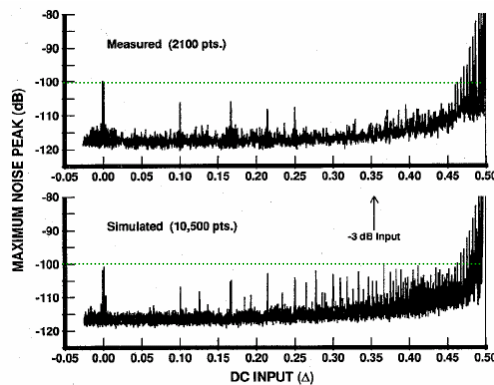|	
Dynamic Range	98 dB (16 b)
Peak SNDR	94 dB
Sampling Rate	12.8 MHz
Oversampling Ratio	256
Output Rate	50 kHz
Signal Band	23 kHz
Differential Input Range	4 V
Supply Voltage	5 V
Power Supply Rejection	60 dB
Power Dissipation	13.8 mW
Area	0.39 mm^2
Technology	1-μm CMOS

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Digital Audio Applications

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Digital Audio Applications

→ Measured & simulated spurious tones performance as a function of DC input signal
→ Sampling rate=12.8MHz, M=256

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.
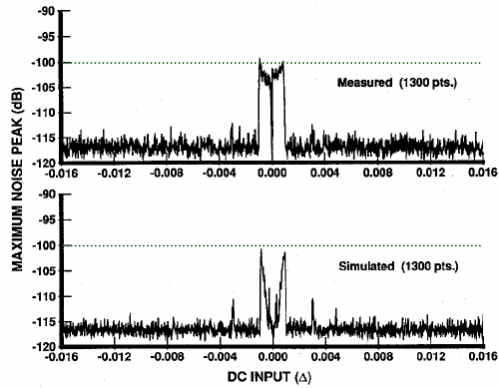
2nd Order ΣΔ
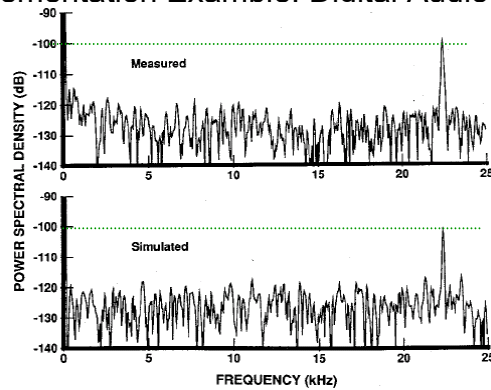## Implementation Example: Digital Audio Applications

Sampling rate=12.8MHz, M=256

→ Measured & simulated noise tone performance for near zero DC worst case input → 0.00088Δ

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Digital Audio Applications

→ Measured & simulated worst-case noise tone @ DC input of 0.00088Δ
→ Both indicate maximum tone @ 22.5kHz around -100dB level

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

Higher Order ΣΔ Modulator Dynamic Range

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)^L E(z) \quad , \quad L \rightarrow \Sigma\Delta \text{ order}$$

$$\overline{S_X} = \frac{1}{2}\left(\frac{\Delta}{2}\right)^2 \qquad \text{sinusoidal input,} \quad STF = 1$$

$$\overline{S_Q} = \frac{\pi^{2L}}{2L+1}\frac{1}{M^{2L+1}}\frac{\Delta^2}{12}$$
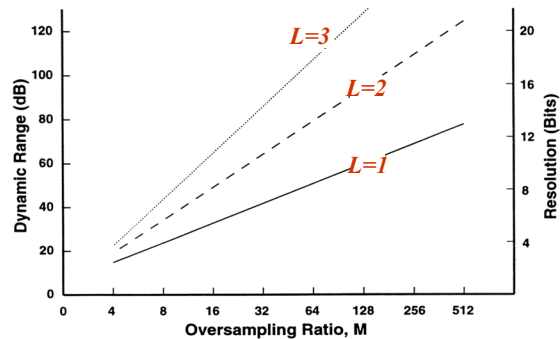
$$\frac{\overline{S_X}}{\overline{S_Q}} = \frac{3(2L+1)}{2\pi^{2L}}M^{2L+1}$$

$$DR = 10\log\left[\frac{3(2L+1)}{2\pi^{2L}}M^{2L+1}\right]$$

$$DR = 10\log\left[\frac{3(2L+1)}{2\pi^{2L}}\right] + (2L+1)\times 10 \times \log M$$

2X increase in M➔(*6L+3*)dB or (*L+0.5*)-bit increase in DR

ΣΔ Modulator Dynamic Range
As a Function of Modulator Order

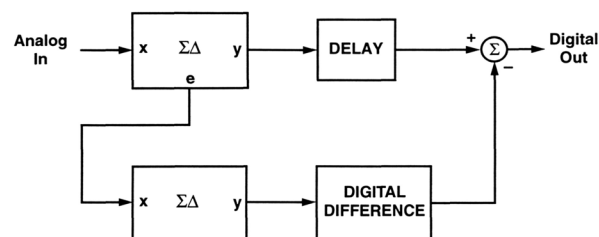• Potential stability issues for L >2

Higher Order $\Sigma\Delta$ Modulators

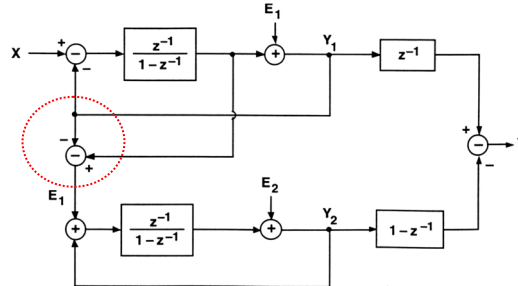- Extending $\Sigma\Delta$ Modulators to higher orders by adding integrators in the forward path (similar to 2nd order)

    $\rightarrow$ Issues with stability

- Two different architectural approaches used to implement $\Sigma\Delta$ modulators with order >2

    1. Cascade of lower order modulators (multi-stage)
    2. Single-loop single-quantizer modulators with multi-order filtering in the forward path

---

Higher Order $\Sigma\Delta$ Modulators
(1) Cascade of 2-Stages $\Sigma\Delta$ Modulators

- Main $\Sigma\Delta$ quantizes the signal
- The 1st stage quantization error is then quantized by the 2nd quantizer
- The quantized error is then subtracted from the results in the digital domain

2nd Order (1-1) Cascaded $\Sigma\Delta$ Modulators

$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})E_1(z)$
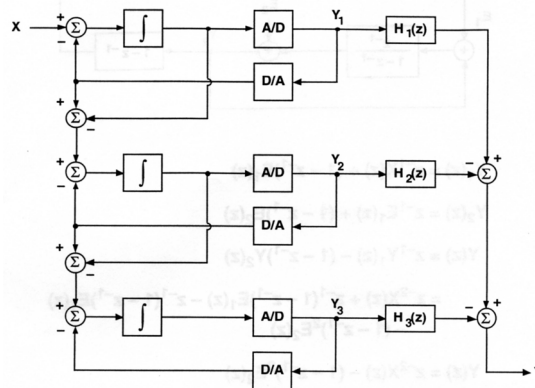
$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$

$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})Y_2(z)$

$\quad = z^{-2}X(z) + z^{-1}(1 - z^{-1})E_1(z) - z^{-1}(1 - z^{-1})E_1(z)$
$\quad\quad - (1 - z^{-1})^2E_2(z)$

$\boxed{Y(z) = z^{-2}X(z) - (1 - z^{-1})^2E_2(z)}$ ⟸ 2nd order noise shaping

3rd Order Cascaded $\Sigma\Delta$ Modulators
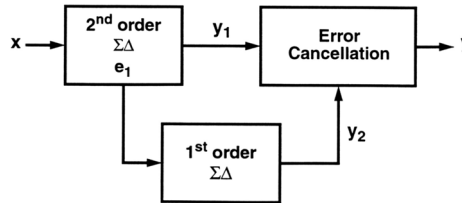## (a) Cascade of 1-1-1 $\Sigma\Delta$s

- Can implement 3rd order noise shaping with 1-1-1

- This is also called MASH (multi-stage noise shaping)

3rd Order Cascaded $\Sigma\Delta$ Modulators
(b) Cascade of 2-1 $\Sigma\Delta$s

Advantages of 2-1 cascade:

- Low sensitivity to precision matching of analog/digital paths

- Low spurious limit cycle tone levels

- No potential instability

$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_1(z)$$
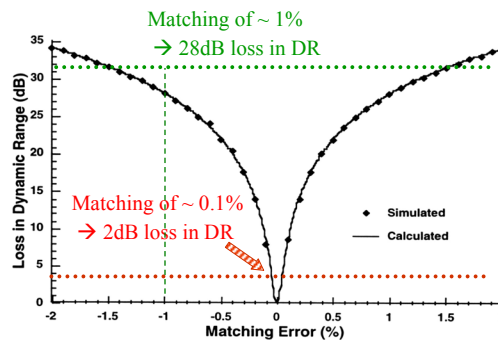
$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})^2 Y_2(z)$$

$$= z^{-3}X(z) + z^{-1}(1 - z^{-1})^2 E_1(z) - z^{-1}(1 - z^{-1})^2 E_1(z)$$

$$- (1 - z^{-1})^3 E_2(z)$$

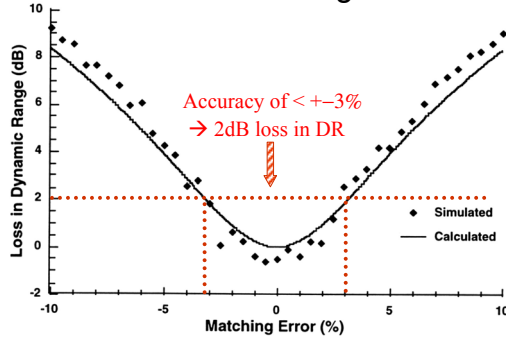3rd order noise shaping ⋙

$$Y(z) = z^{-3}X(z) - (1 - z^{-1})^3 E_2(z)$$

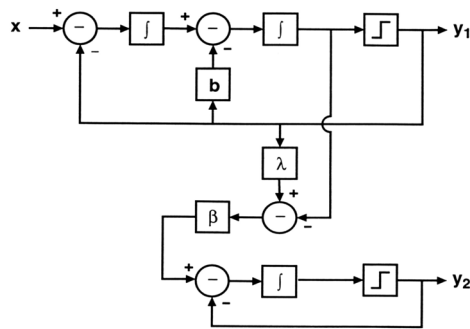## Sensitivity of Cascade of (1-1-1) $\Sigma\Delta$ Modulators to Matching of Analog & Digital Paths

Matching of ~ 1%
→ 28dB loss in DR

Matching of ~ 0.1%
→ 2dB loss in DR

Sensitivity of Cascade of (2-1) $\Sigma\Delta$ Modulators to Matching Error

Accuracy of $< +-3\%$
$\rightarrow$ 2dB loss in DR

(Simulated, Calculated)

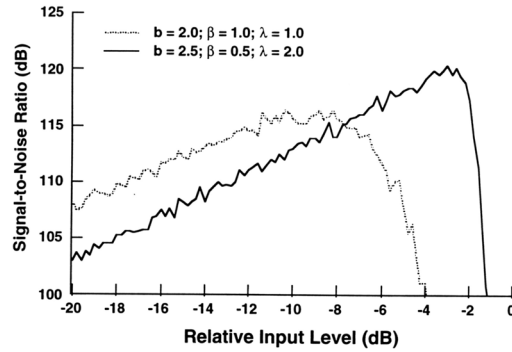Main advantage of 2-1 cascade compared to 1-1-1 topology:

• Low sensitivity to matching of analog/digital paths (in excess of one order of magnitude less sensitive compared to (1-1-1)!)

2-1 Cascaded $\Sigma\Delta$ Modulators

Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits,* vol. 29, pp. 193 - 202, March 1994.
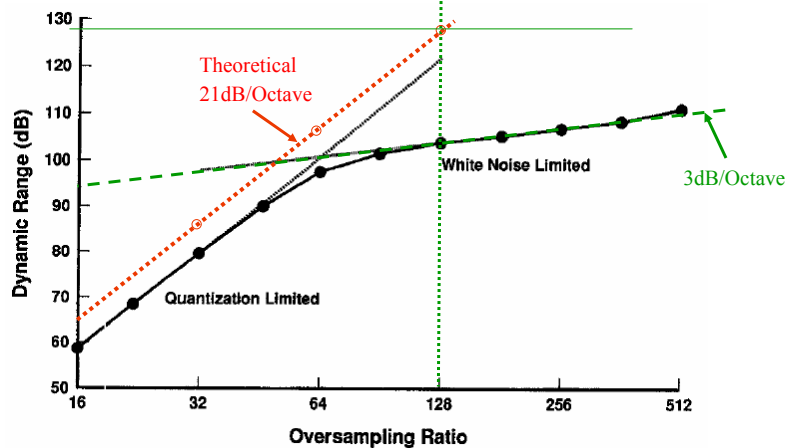
2-1 Cascaded ΣΔ Modulators

Effect of gain parameters on signal-to-noise ratio

Comparison of 2nd order & Cascaded (2-1) ΣΔ Modulator

Digital Audio Application, $f_N = 50kHz$		
(Does not include Decimator)		
Reference	Brandt ,JSSC 4/91	Williams, JSSC 3/94
Architecture	*2nd order*	*(2+1) Order*
Dynamic Range	*98dB (16-bits)*	*104dB (17-bits)*
Peak SNDR	*94dB*	*98dB*
Oversampling rate	*256 (theoretical →* *SNR=109dB)*	*128 (theoretical →* *SNR=128dB)*
Differential input range	*4Vppd* *5V supply*	*8Vppd* *5V supply*
Power Dissipation	*13.8mW*	*47.2mW*
Active Area	*0.39mm² (1μ tech.)*	*5.2mm² (1μ tech.)*

2-1 Cascaded ΣΔ Modulators
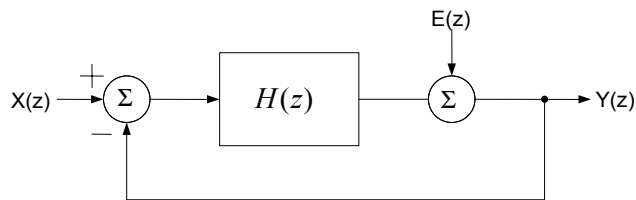## Measured Dynamic Range Versus Oversampling Ratio

Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits,* vol. 29, pp. 193 - 202, March 1994.

Higher Order ΣΔ Modulators
(1) Cascaded Modulators Summary

- Cascade two or more stable ΣΔ stages

- Quantization error of each stage is quantized by the succeeding stage and subtracted digitally

- Order of noise shaping equals sum of the orders of the stages

- Quantization noise cancellation depends on the precision of analog/digital signal paths

- Quantization noise further randomized → less limit cycle oscillation problems

- Typically, no potential instability

Higher Order $\Sigma\Delta$ Modulators
(2) Multi-Order Filter

E(z)

X(z) → Σ (+ / −) → $H(z)$ → Σ → Y(z)

$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z)$$

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

• Zeros of NTF (poles of H(z)) can be strategically positioned to suppress in-band noise spectrum
• Approach: Design NTF first and solve for H(z)

Example: Modulator Specification

• Example: Audio ADC
   – Dynamic range   DR   18 Bits
   – Signal bandwidth   B   20 kHz
   – Nyquist frequency f_N 44.1 kHz
   – Modulator order   L   5
   – Oversampling ratio $M = f_s/f_N$ 64
   – Sampling frequency f_s 2.822 MHz

• The order L and oversampling ratio M are chosen based on
   – SQNR > 120dB