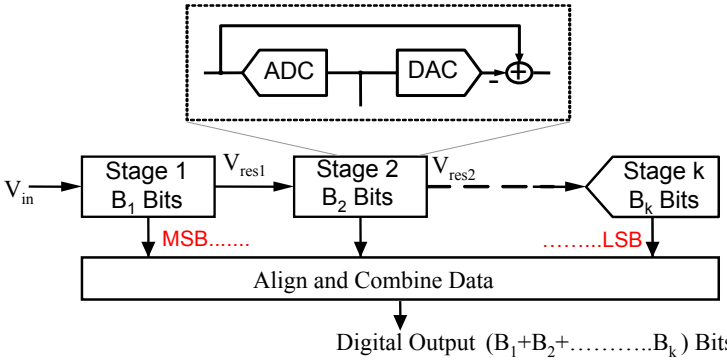
EE247
Lecture 23

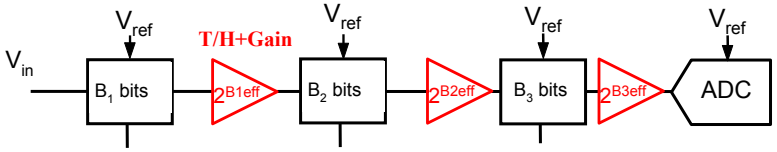
Pipelined ADCs (continued)
- Effect gain stage, sub-DAC non-idealities on overall ADC performance
  - Digital calibration (continued)
  - Correction for inter-stage gain nonlinearity
- Implementation
  - Practical circuits
  - Stage scaling
  - Combining the bits
  - Stage implementation
    - Circuits
    - Noise budgeting
  - How many bits per stage?
- Algorithmic ADCs utilizing pipeline structure
- Advanced background calibration techniques

Pipeline ADC Block Diagram



- Idea: Cascade several low resolution stages to obtain high overall resolution (e.g. 10bit ADC can be built with series of 10 ADCs each 1-bit only!)
- Each stage performs coarse A/D conversion and computes its quantization error, or "residue"

Summary So Far
Pipelined A/D Converters



- Cascade of low resolution stages
  - By adding inter-stage gain= 2^{Beff}
    - No need to scale down Vref for stages down the pipe
    - Reduced accuracy requirement for stages coming after stage 1
  - Addition of Track & Hold function to interstage-gain →
    - stages can operate concurrently→
    - Throughput increased to as high as one sample per clock cycle
    - Latency function of number of stages & conversion-per-stage
  - Correction for circuit non-idealities
    - Built-in redundancy compensate for sub-ADC inaccuracies such as comparator offset (interstage gain: $G=2^{Bneff}$, $B_{neff} < B_n$)

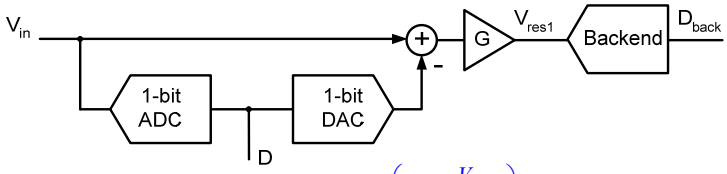
Pipeline ADC
Error Compensation

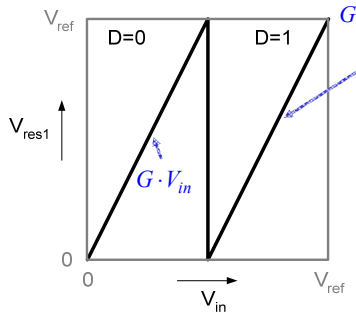
- Non-idealities associated with sub-ADCs, sub-DACs and gain stages → error in overall pipeline ADC performance
- Need to find means to tolerate/correct errors
- Important sources of error
  - Sub-ADC errors- comparator offset
  - Gain stage offset
  - Gain stage error
  - Sub-DAC error

Gain Stage Gain Inaccuracy

- Gain error can be compensated in digital domain – "Digital Calibration"
- Problem: Need to measure/calibrate digital correction coefficient
- Example: Calibrate 1-bit first stage
- Objective: Measure G in digital domain

ADC Model





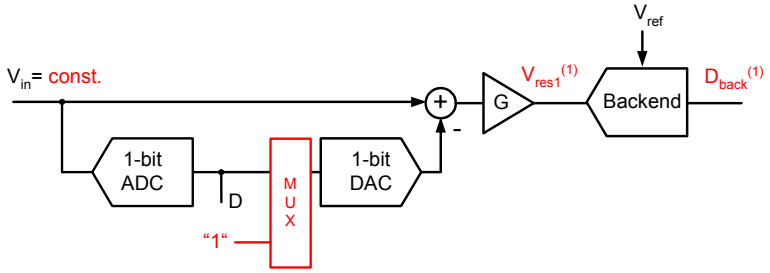
$$G \cdot \left(V_{in} - \frac{V_{ref}}{2} \right)$$

$$V_{res1} = G \cdot (V_{in} - V_{DAC})$$

$$V_{DAC}(D=0) = 0$$

$$V_{DAC}(D=1) = V_{ref}/2$$

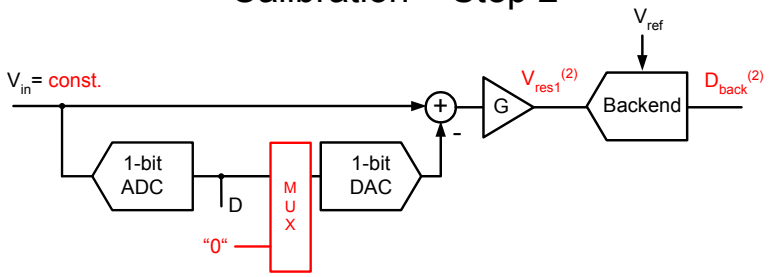
Gain Stage Inacurracy Calibration – Step 1



$$V_{res1}^{(1)} = G \cdot \left(V_{in} - V_{ref}/2\right)$$

$$D_{back}^{(1)} = G \cdot \frac{\left(V_{in} - V_{ref}/2\right)}{V_{ref}} \rightarrow store$$

Gain Stage Inacurracy Calibration – Step 2



$$V_{res1}^{(2)} = G \cdot \left(V_{in} - 0\right)$$

$$D_{back}^{(2)} = G \cdot \frac{\left(V_{in} - 0\right)}{V_{ref}} \rightarrow store$$

Gain Stage Inacurracy Calibration – Evaluate

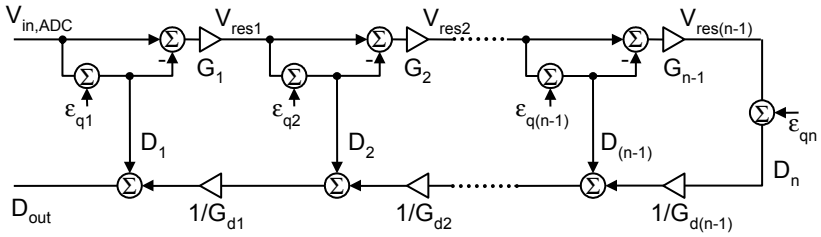
$$D_{back}^{(1)} = G \cdot \frac{\left(V_{in} - V_{ref}/2\right)}{V_{ref}}$$

$$-D_{back}^{(2)} = G \cdot \frac{\left(V_{in} - 0\right)}{V_{ref}}$$

$$D_{back}^{(1)} - D_{back}^{(2)} = \frac{1}{2} \cdot G$$

- To minimize the effect of backend ADC noise → perform measurement several times and take the average

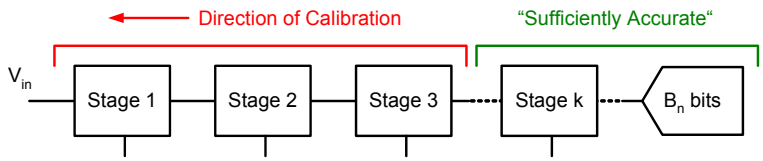
Accuracy Bootstrapping



$$D_{out} = V_{in,ADC} + \varepsilon_{q1}\left(1 - \frac{G_1}{G_{d1}}\right) + \frac{\varepsilon_{q2}}{G_{d1}}\left(1 - \frac{G_2}{G_{d2}}\right) + \ldots + \frac{\varepsilon_{q(n-1)}}{\prod_{j=1}^{n-2} G_{dj}}\left(1 - \frac{G_{(n-1)}}{G_{d(n-1)}}\right) + \frac{\varepsilon_{qn}}{\prod_{j=1}^{n-1} G_{dj}}$$

- Highest sensitivity to gain errors in front-end stages

"Accuracy Bootstrapping"



Ref:

A. N. Karanicolas et al. "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE J. Of Solid-State Circuits*, pp. 1207-15, Dec. 1993

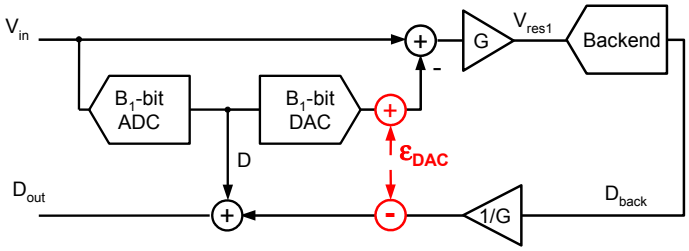
E. G. Soenen et al., "An architecture and an algorithm for fully digital correction of monolithic pipelined ADCs," TCAS II, pp. 143-153, March 1995

L. Singer et al., "A 12 b 65 MSample/s CMOS ADC with 82 dB SFDR at 120 MHz," *ISSCC 2000, Digest of Tech. Papers.*, pp. 38-9 (calibration in opposite direction!)

Pipeline ADC Errors

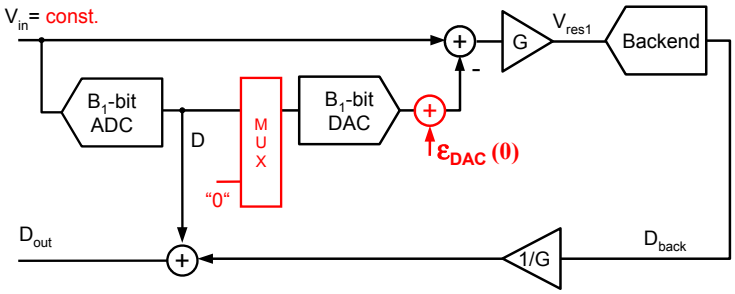
- Non-idealities associated with sub-ADCs, sub-DACs and gain stages → error in overall pipeline ADC performance
- Need to find means to tolerate/correct errors
- Important sources of error
  - Sub-ADC errors- comparator offset
  - Gain stage offset
  - Gain stage error
  - Sub-DAC error

DAC Errors



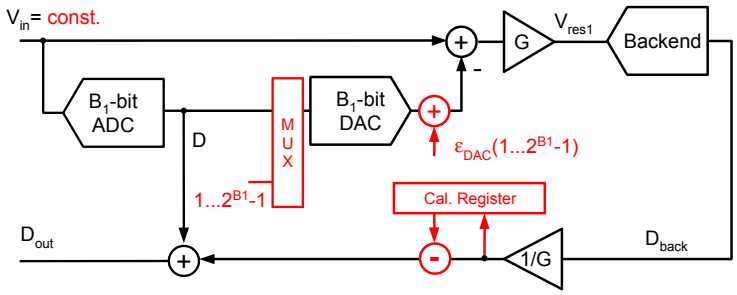
- Can be corrected digitally as well
- Same calibration concept as gain errors
  → Vary DAC codes & measure errors via backend ADC

DAC Calibration – Step 1



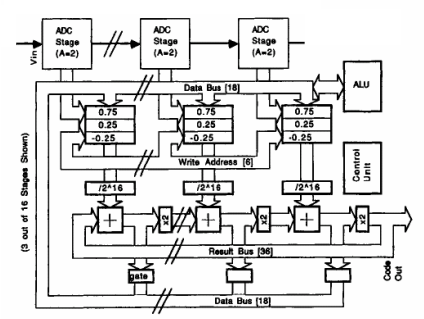
- $\varepsilon_{DAC}(0)$ equivalent to offset - ignore

DAC Calibration – Step 2...2^{B1}



- Stepping through DAC codes 1...2^{B1}-1 yields all incremental correction values
- Measurements repeated and averages to account for variance associated with noise

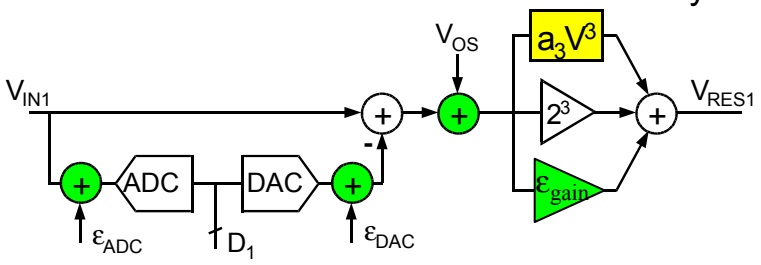
Pipeline ADC
Example: Calibration Hardware



- Above block diagram may seem extensive however, in current fine-line CMOS technologies digital portion of a pipeline ADCs consume insignificant power and area compared to the analog sections

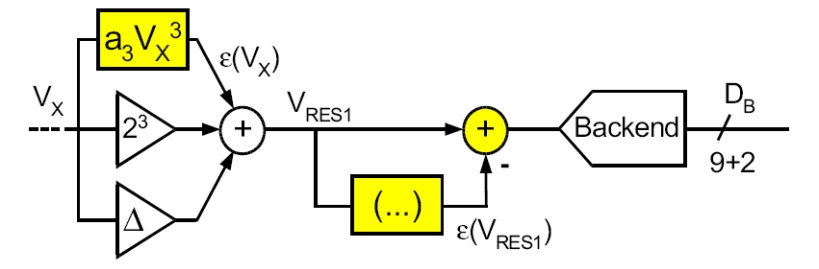
Ref: E. G. Soenen et al., "An architecture and an algorithm for fully digital correction of monolithic pipelined ADCs," TCAS II, pp. 143-153, March 1995

Pipelined ADC
Error Correction/Calibration Summary



Error	Correction/Calibration
ε_{ADC}, V_{os}	Redundancy either same stage or next stage
ε_{gain}	Digital adjustment
ε_{DAC}	Either sufficient component matching or digital calibration
Inter-stage amplifier non-linearity	?

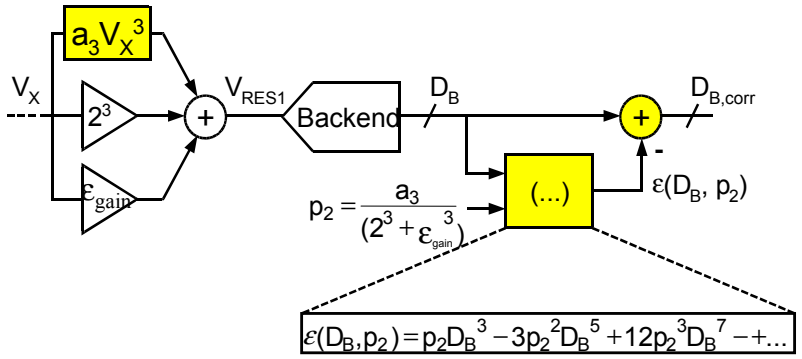
Inter-stage Gain Nonlinearity



- Invert gain stage non-linear polynomial
- Express error as function of V_{RES1}
- Push error into digital domain through backend

Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," *ISSCC Dig. Techn. Papers*, pp. 328-329, 2003

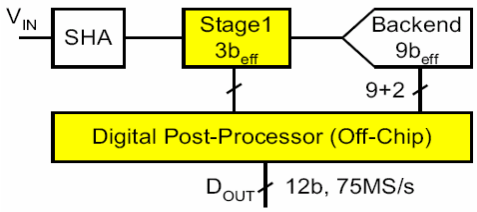
Inter-stage Gain Nonlinearity



- Pre-computed table look-up
- p_2 continuously estimated & updated (account for temp. & other variations)

Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," *ISSCC Dig. Techn. Papers*, pp. 328-329, 2003

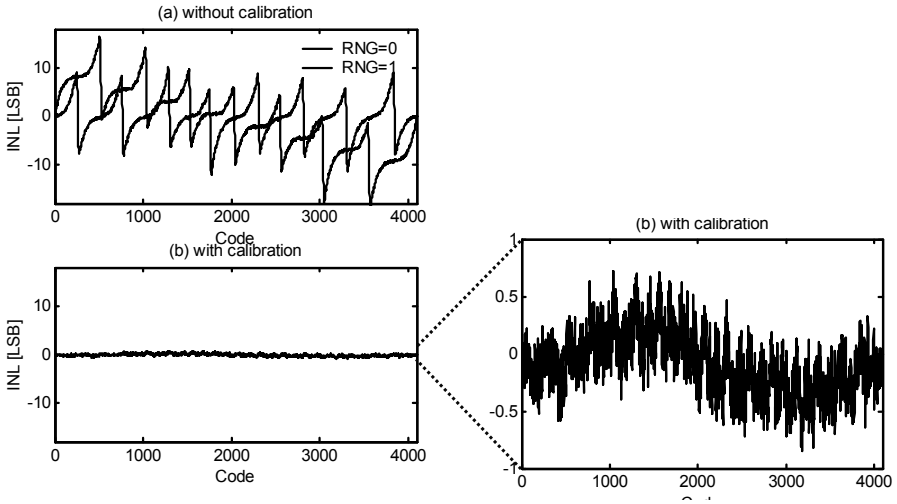
Inter-stage Gain Nonlinearity Compensation Proof of Concept Evaluation Prototype



- Re-used 14-bit ADC in 0.35µm from Analog Devices [Kelly, ISSCC 2001]
- Modified only 1st stage with 3-b_{eff} → open-loop amplifier built with simple diff-pair + resistive load instead of the conventional feedback around high-gain amp
- Conventional 9-b_{eff} backend, 2-bit redundancy in 1st stage
- Real-time post-processor off-chip (FPGA)

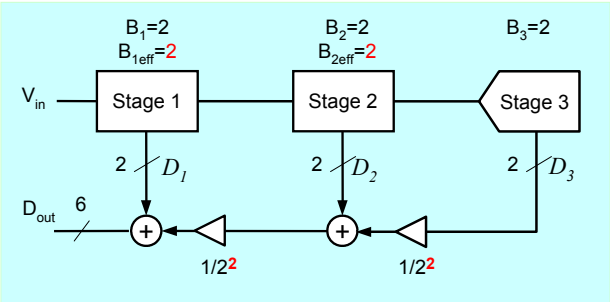
Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," *ISSCC Dig. Techn. Papers*, pp. 328-329, 2003

Measurement Results
12-bit ADC w Extra 2-bits for Calibration



Combining the Bits

- Example: Three 2-bit stages, no redundancy



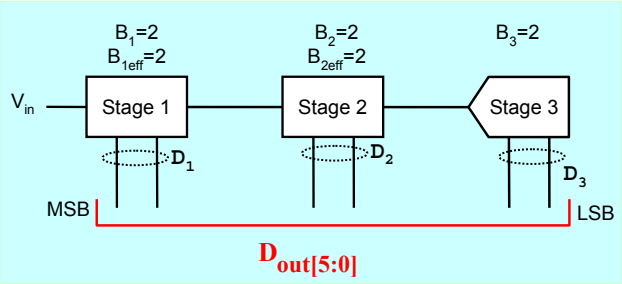
$$D_{out} = D_1 + \frac{1}{2^{B1eff}} D_2 + \frac{1}{2^{B1eff} \cdot 2^{B2eff}} D_3$$

$$D_{out} = D_1 + \frac{1}{4} D_2 + \frac{1}{16} D_3$$

Combining the Bits

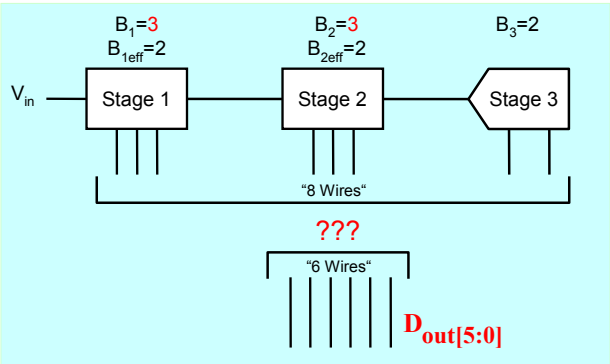
```
D1    XX
D2      XX
D3        XX
------------
Dout  DDDDDD
```

- Only bit shifts
- No arithmetic circuits needed



Combining the Bits Including Redundancy

- Example: Three 2-bit stages, incorporating 1- bit redundancy in stages 1 and 2

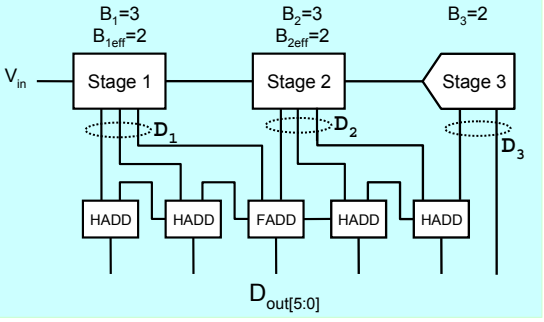


Combining the Bits

$$D_{out} = D_1 + \frac{1}{2^{B1eff}} D_2 + \frac{1}{2^{B1eff} \cdot 2^{B2eff}} D_3$$

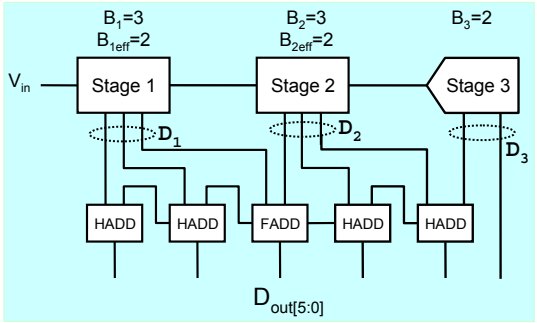
$$D_{out} = D_1 + \frac{1}{4} D_2 + \frac{1}{16} D_3$$

- Bits overlap
- Need adders



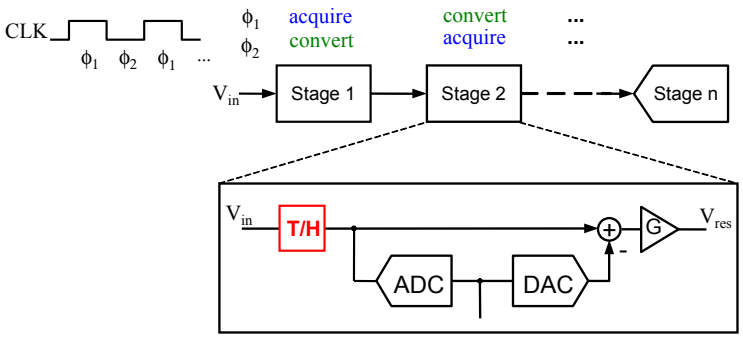

```
D1     XXX
D2       XXX
D3         XX
------------
Dout   DDDDDD
```


Combining the Bits Example



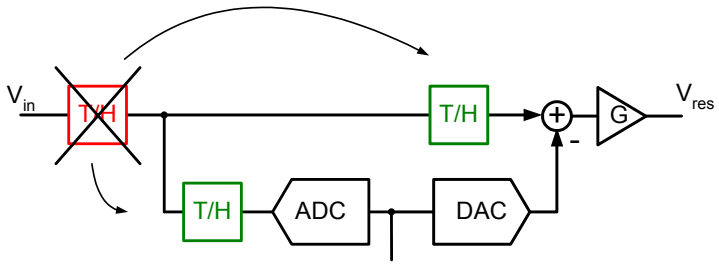

```
D1     001
D2       111
D3         10
------------
Dout   011000
```

Stage Implementation



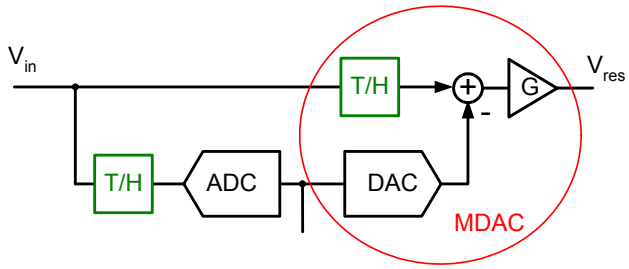
- Each stage needs T/H hold function
- Track phase: Acquire input/residue from previous stage
- Hold phase: sub-ADC decision, compute residue

Stage Implementation



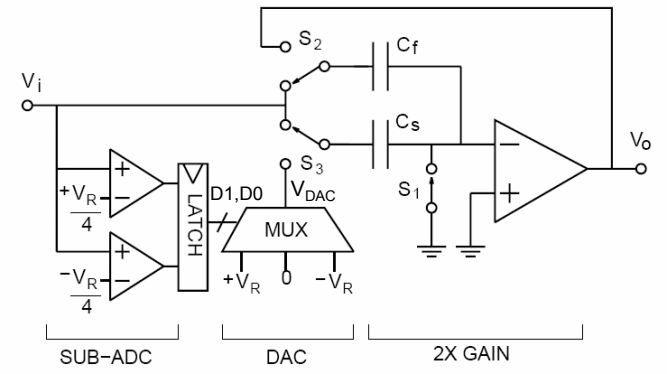
- Usually no dedicated T/H amplifier in each stage (Except first stage in some cases – why?)
- T/H implicitely contained in stage building blocks

Stage Implementation



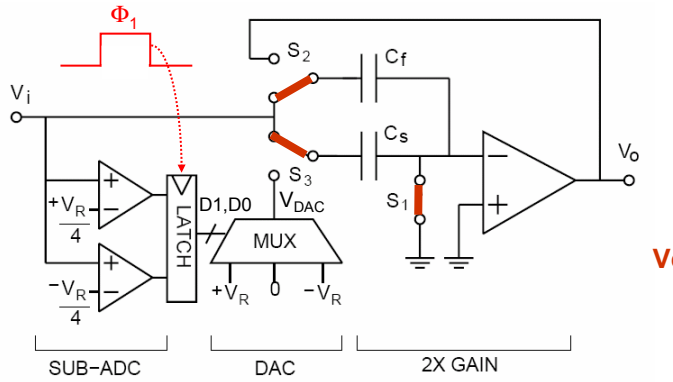
- DAC-subtract-gain function can be lumped into a single switched capacitor circuit
- "MDAC"

1.5-Bit Stage Implementation Example



Ref: A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

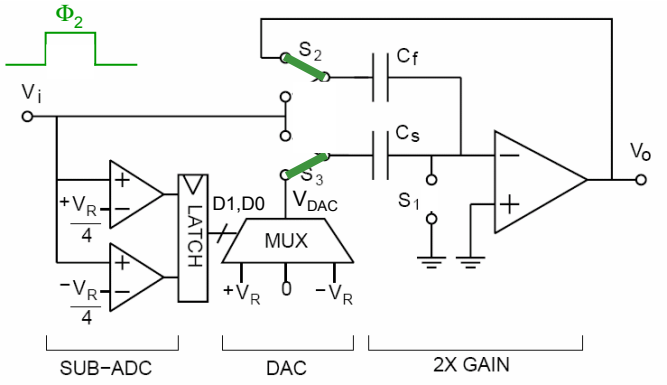
1.5-Bit Stage Implementation
Acquisition Cycle



$Vc_f=Vc_s=V_i$

Ref: A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

1.5-Bit Stage Implementation
Conversion Cycle

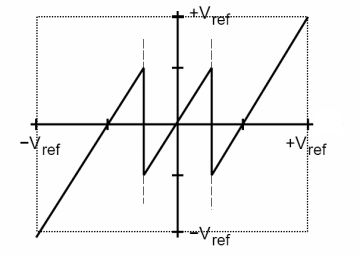


Ref: A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

1.5 Bit Stage Implementation Example

$$V_o = \begin{cases} \left(1+\frac{C_s}{C_f}\right)V_i - \frac{C_s}{C_f}V_{ref} & \text{if } V_i > V_{ref}/4 \\ \left(1+\frac{C_s}{C_f}\right)V_i & \text{if } -V_{ref}/4 \le V_i \le +V_{ref}/4 \\ \left(1+\frac{C_s}{C_f}\right)V_i + \frac{C_s}{C_f}V_{ref} & \text{if } V_i < -V_{ref}/4 \end{cases}$$

Note: Interstage gain set by C ratios
- → Accuracy better than 0.1%
- →Up to 10bit level no need for gain calibration



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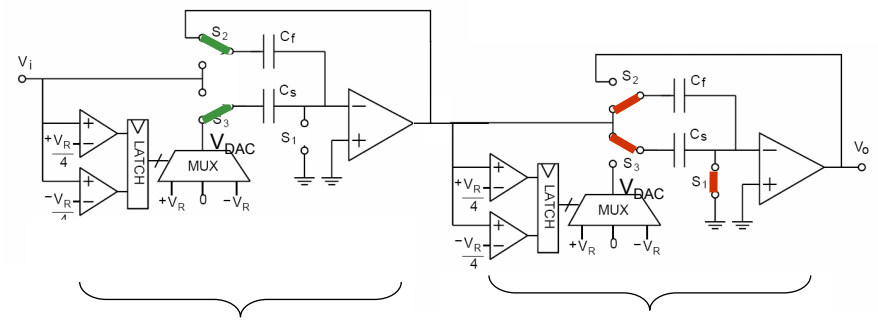
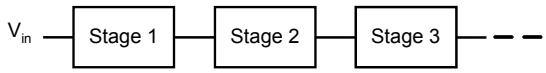
1.5-Bit Stage Implementation Timing of Stages

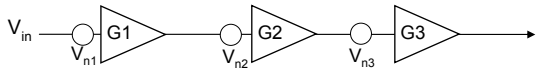


Conversion *Acquisition*

Pipelined ADC Stage Power Dissipation & Noise

- Typically pipeline ADC noise dominated by inter- stage gain blocks
- Sub-ADC comparator noise translates into comparator threshold uncertainty and is compensated for by redundancy

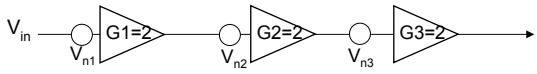


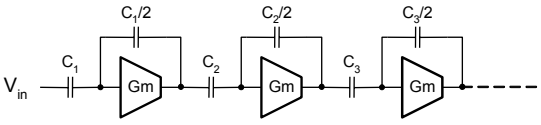


$$V_{noise}^{in} = \sqrt{V_{n1}^2 + \frac{V_{n2}^2}{G1^2} + \frac{V_{n3}^2}{G1^2 G2^2} + \ldots}$$

Pipelined ADC Stage Scaling

- Example: Pipeline using 1-bit$_{eff}$ stages



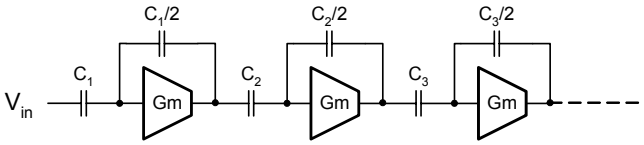


- Total input referred noise power:

$$N_{tot} \propto kT\left[\frac{1}{C_1} + \frac{1}{G1^2 C_2} + \frac{1}{G1^2 G2^2 C_3} + \ldots\right]$$

$$N_{tot} \propto kT\left[\frac{1}{C_1} + \frac{1}{4C_2} + \frac{1}{16C_3} + \ldots\right]$$

Pipelined ADC Stage Scaling

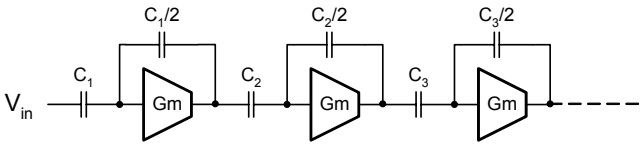


$$N_{tot} \propto kT\left[\frac{1}{C_1}+\frac{1}{4C_2}+\frac{1}{16C_3}+...\right]$$

- If all caps made the same size, backend stages contribute very little noise
- Wasteful power-wise, because:
  - ❑ Power ~ Gm
  - ❑ Speed ~ Gm/C

    Fixed speed → Gm/C filxed → Power ~ C

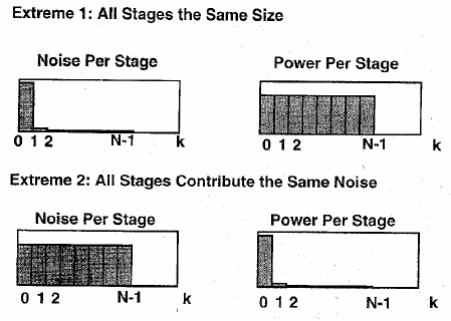
Pipelined ADC Stage Scaling



$$N_{tot} \propto kT\left[\frac{1}{C_1}+\frac{1}{4C_2}+\frac{1}{16C_3}+...\right]$$

- How about scaling caps down by $G^2=2^2=4x$ per stage?
  - – Same amount of noise from every stage
  - – All stages contribute significant noise
  - – To keep overall noise the same → noise/stage must be reduced
  - – Power ~ Gm ~ C goes up!

Stage Scaling
Example: 2-bit$_{eff}$/stage

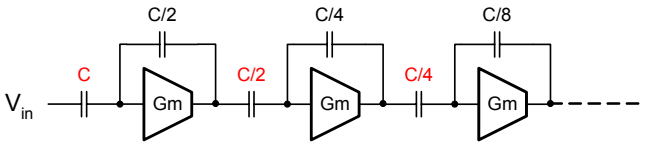


- Optimum capacitior scaling lies approximately midway between these two extremes

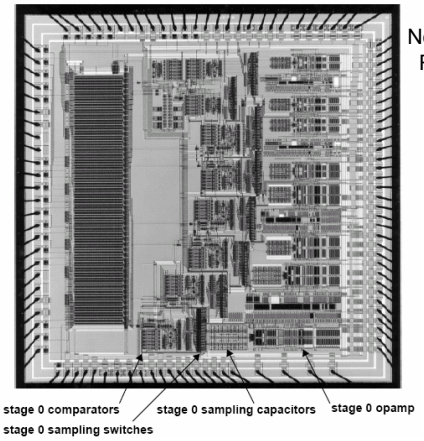
Ref: D. W. Cline, P.R. Gray "A power optimized 13-b 5MSamples/s pipelined analog-to-digital converter in 1.2um CMOS," JSSC 3/1996

Pipeline ADC
Stage Scaling

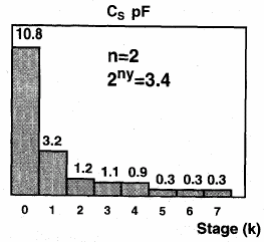
- Power minimum is "shallow“
- Near optimum solution in practice: Scale capacitors by stage gain
- E.g. for effective stage resolution of 1bit (Gain=2):

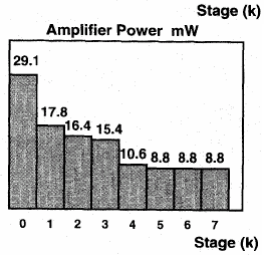


Stage Scaling Example



Note:
Resolution per stage:
→2bits
→A=4





Ref: D. W. Cline, P.R Gray "A power optimized 13-b 5 MSamples/s pipelined analog-to-digital converter in 1.2um CMOS," JSSC 3/1996

How Many Bits Per Stage?

- Many possible architectures
  - E.g. B_{1eff}=3, B_{2eff}=1, ...
    vs. B_{1eff}=1, B_{2eff}=1, B_{3eff}=1, ...
- Complex optimization problem, fortunately optimum tends to be shallow...
- Qualitative answer:
  - Maximum speed for given technology
    - Use small resolution-per-stage (large feedback factor)
  - Maximum power efficiency for fixed, "low" speed
    - Try higher resolution stages
    - Can help alleviate matching & noise requirements in stages following the 1st stage
      Ref: Singer VLSI 96, Yang, JSSC 12/01

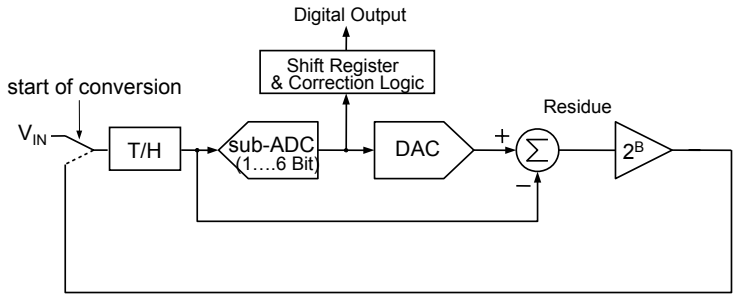
14 & 12-Bit State-of-the-Art Implementations

Reference	Yang (JSSC 12/2001) 0.35μ/3V	Loloee (ESSIRC 2002) 0.18μ/3V
Bits	14	12
Architecture	3-1-1-1-1-1-1-1-1-3	1-1-1-1-1-1-1-1-1-1-2
SNR/SFDR	~73dB/88dB	~66dB/75dB
Speed	75MS/s	80MS/s
Power	340mW	260mW

10 & 8-Bit State-of-the-Art Implementations

Reference	Yoshioko et al (ISSCC 2005) 0.18μ/1.8V	Kim et al (ISSCC 2005) 0.18μ/1.8V
Bits	10	8
Architecture	1.5bit/stage	2.8 -2.8 - 4
SNR/SFDR	~55dB/66dB	~48dB/56dB
Speed	125MS/s	200MS/s
Power	40mW	30mW

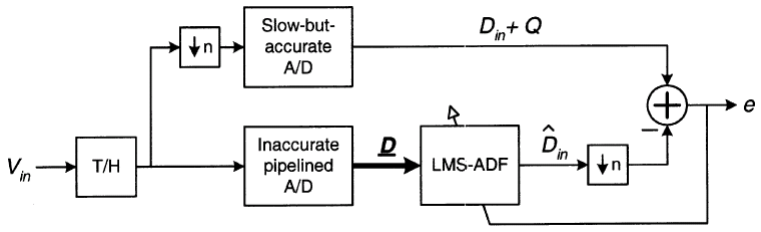
Algorithmic ADC



- Essentially same as pipeline, but a single stage is reused for all partial conversions
- For overall $B_{overall}$ bits → need $B_{overall}/B_{stage}$ clock cycles per conversion

  → Small area, slow

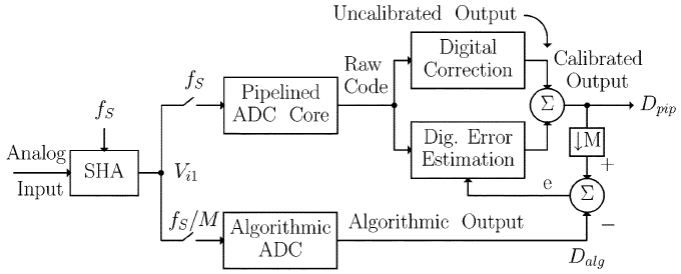
Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters



- Slow, but accurate ADC operates in parallel with pipelined (main) ADC
- Slow ADC samples input signal at a lower sampling rate (f_s/n)
- Difference between corresponding samples for two ADCs (e) used to correct fast ADC digital output via an adaptive digital filter (ADF) based on minimizing the Least-Mean-Squared error

Ref: Y. Chiu, *et al,* "Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters," IEEE TRANS. CAS, VOL. 51, NO. 1, JANUARY 2004

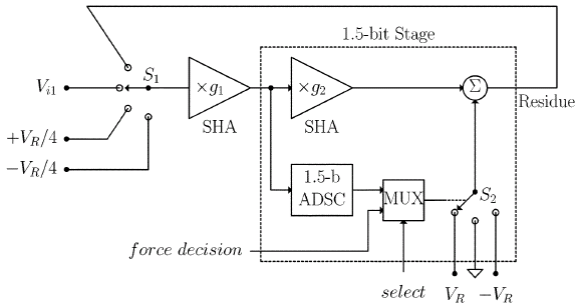
Example: "A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration"



- Pipelined ADC operates at 20Ms/s @ has 1.5bit/stage
- Slow ADC → Algorithmic type operating at 20Ms/32=625ks/s
- Digital correction accounts for bit redundancy
- Digital error estimator → minimizes the mean-squared-error

Ref: X. Wang, P. J. Hurst, S. H. Lewis, " A 12-bit 20-Msample/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

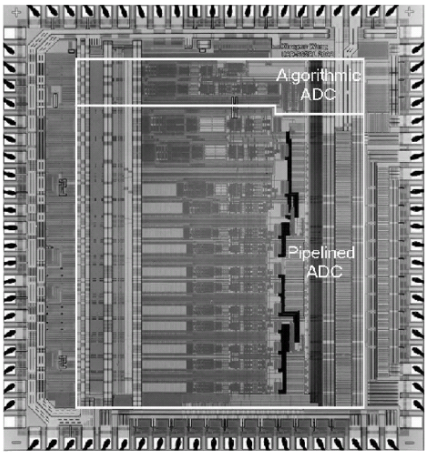
Algorithmic ADC Used for Calibration of Pipelined ADC (continued from previous page)



- Uses replica of pipelined ADC stage
- Requires extra SHA in front to hold residue
- Undergoes a calibration cycle periodically prior to being used to calibrate pipelined ADC

Ref: X. Wang, P. J. Hurst, S. H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

12-bit 20-MS/s Pipelined ADC with Digital Background Calibration

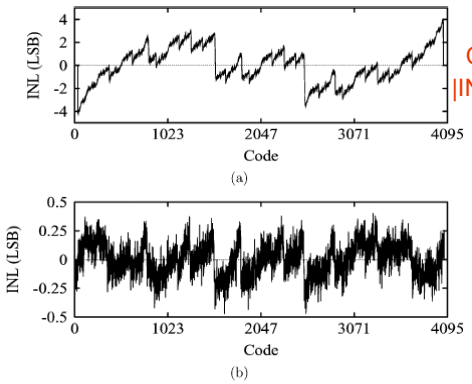


Sampling capacitors scaled:
- Input SHA: 6pF
- Pipelined ADC: 2pF,0.9,0.4,0.2, 0.1,0.1…
- Algorithmic ADC: 0.2pF

Chip area: 13.2mm^2
- Area of Algorithmic ADC <20%
- Does not include digital calibration circuitry estimated ~1.7mm^2

Ref: X. Wang, P. J. Hurst, S. H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Measurement Results
12-bit 20-MS/s Pipelined ADC with Digital Background Calibration

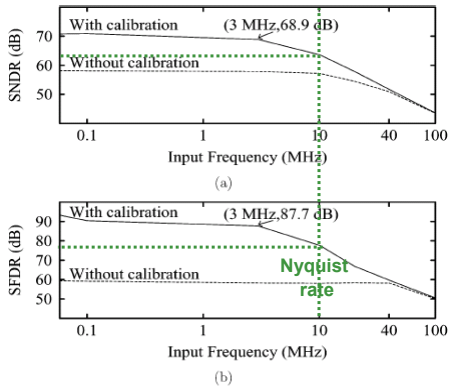


Without Calibration |INL|<4.2LSB

With Calibration |INL|<0.5LSB

Ref: X. Wang, P. J. Hurst, S. H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Measurement Results
12-bit 20-MS/s Pipelined ADC with Digital Background Calibration



Ref: X. Wang, P. J. Hurst, S. H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Measurement Results
12-bit 20-MS/s Pipelined ADC with Digital Background Calibration

PERFORMANCE SUMMARY (3.3 V, 25 °C)

Process	0.35μm 2P4M CMOS	
Sampling rate	20 Msample/s	
Active area	7.5 mm^2	
Full-Scale Input	1.6 Vp-p	
	Without Cal.	With Cal.
Analog Power Diss.	190 mW	226 mW
Total Power Diss.	217 mW	254 mW
Max. |INL| (Pip. ADC)*	4.21 LSB	0.47 LSB
Max. |DNL| (Pip. ADC)*	0.60 LSB	0.41 LSB
SNDR (Alg. ADC)*	49.6 dB	59.6 dB
SNDR (Pip. ADC)*	58.2 dB	70.8 dB
SFDR (Pip. ADC)*	59.4 dB	93.3 dB
THD (Pip. ADC) *	–59.4 dB	–92.9 dB
PSRR*	65.0 dB	64.8 dB
CMRR*	73.6 dB	73.4 dB

*f_{in}=58 kHz

Does not include digital calibration circuitry estimated ~1.7mm^2

Alg. ADC SNDR dominated by noise

Ref: X. Wang, P. J. Hurst, S. H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004